Problem Set #6

Assigned: October 15, 2008
Due: October 22, 2008 at Recitation

Reading Assignments:	10/14/08	Sections 5.3 - 5.4 of Howe & Sodini
	10/16/08	Sections 5.5-5.6 of Howe & Sodini
	10/21/08	Sections 6.1–6.3 of Howe & Sodini

PLEASE WRITE YOUR RECITATION SESSION TIME ON YOUR PROBLEM SET SOLUTION

MOS Device Data for Problem 1.

$$\mu_N C_{ox} = 50\,\mu A/V^2, \quad \mu_P C_{ox} = 25\,\mu A/V^2, \quad V_{Ton} = 1V, \quad V_{Top} = -1V$$
$$-2\phi_p = 0.84V, \quad 2\phi_n = 0.84V, \quad \gamma_n = 0.6V^{1/2}, \quad \gamma_p = 0.6V^{1/2}$$
$$\lambda_n = \frac{0.1}{L}V^{-1}, \quad \lambda_p = \frac{0.1\,\mu m}{L}V^{-1} \quad [L \text{ in } \mu m]; \quad \phi_p = -0.42V, \quad \phi_n = 0.42V$$

1. [25 points] Problem E4-19 of Howe and Sodini (***note comment in p. 246 of Howe & Sodini under "Exercises" heading***). Use the approximation that the overlap capacitance per unit area is the same as the oxide capacitance per unit area i.e. $C_{ov} \approx C_{ox} \bullet L_D$

   The n-channel MOSFET shown in layout in Figure PS6-1.1 is biased at the operating point $V_{GS} = 3V; V_{DS} = 5V; V_{BS} = -1V$. For this problem, include $L_D = 0.1$ μm in finding the channel length L from the layout and let $C_{ox} = 1.42$ fF/μm^2.

   a) Find the small signal parameters g_m, g_{mb} and r_o at this operating point.
   b) Find the capacitances C_{gs}, C_{gd}, C_{db} and C_{sb}. In calculating the overlap capacitances, only consider the underdiffusion of the drain and source diffusions by L_D. Also you can neglect the sidewall capacitance and use a substrate doping Na = 10^{17} cm^{-3}.

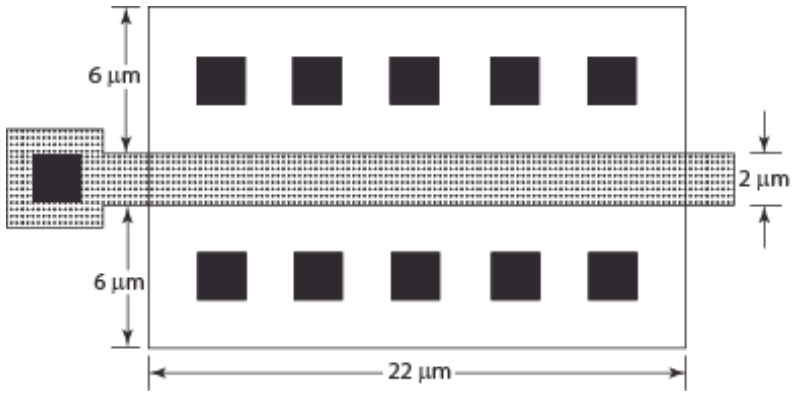

Figure PS6-1.1:

MOS Device Data for Problems 2.

$$\mu_N C_{ox} = 50\,\mu A/V^2 \quad \mu_P C_{ox} = 25\,\mu A/V^2 \quad V_{Tn} = 1V \quad V_{Tp} = -1V$$
$$-2\phi_p = 0.8V \quad 2\phi_n = 0.8V \quad \gamma_n = 0.6V^{1/2} \quad \gamma_p = 0.6V^{1/2}$$
$$\lambda_n = 0.067\frac{1.5\,\mu m}{L}V^{-1} \quad \lambda_p = 0.067\frac{1.5\,\mu m}{L}V^{-1}$$
$$C_{ox} = 2.3\ fF/\mu m^2 \quad C_{jn} = 0.1\ fF/\mu m^2 \quad C_{jp} = 0.3\ fF/\mu m^2$$
$$C_{JSWn} = 0.5\ fF/\mu m \quad C_{JSWp} = 0.35\ fF/\mu m \quad L_{diffn} = 6\,\mu m \quad L_{diffp} = 6\,\mu m$$

2. [25 points] Given an PMOS inverter shown in Figure PS6-2-01with a pull down resistor of 10 kΩ and V_{DD}=5.0 V.
   (a) Sketch the voltage transfer characteristics and label V_{IL}, V_{IH}, V_M, V_{OH} and V_{OL} for a PMOS transistor (W/L) = (20 μm / 1 μm)?
   (b) For the PMOS inverter in (a) calculate NM_H and NM_L using the simplified hand calculation presented in lecture.
   (c) If a 100 fF load capacitor is connected to the output of the inverter, calculate t_{PLH} and t_{PHL} for the inverter. [**Include the influence of C_{DB} in your calculations and use the diagram in Lecture 10 for calculating relevant capacitances. Assume that $C_{ov} = 0$].**

   (d) What is the static power dissipation?

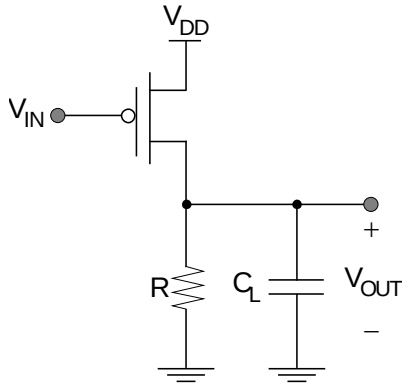

Figure PS6-2-01

3. [25 points] Problem P5.10 of Howe and Sodini:
In this problem you will size a CMOS inverter with process parameters:

$V_{Tn} = 0.7 \quad V_{Tp} = -0.9$

$\mu_n = 500\ cm^2/Vs \quad \mu_p = 200\ cm^2/Vs \quad t_{ox} = 20\ nm \quad \lambda_n = \lambda_p = 0.05\ V^{-1}$

$C_{jn} = 0.1\ fF/\mu m^2 \quad C_{jp} = 0.3\ fF/\mu m^2$

$C_{JSWn} = 0.5\ fF/\mu m \quad C_{JSWp} = 0.35\ fF/\mu m \quad L_{diffn} = 6\ \mu m \quad L_{diffp} = 6\ \mu m$

Assume equal channel lengths, V_{DD} = 5 V and all other process parameters are as given on Page 319 of H& S.

(a) Calculate the ratio of W_n/W_p, such that V_M=2.5 V.

(b) When $V_{IN}=V_M$, we want the current through the inverter to be 1 mA. What is W_n and W_p assuming the channel length of both devices is 2 μm?

The CMOS Inverter you have just sized above must drive two identical inverters connected in parallel as shown in Figure PS6-1.1 [Figure 5.24 (b) of H & S].

(c) What is the component of the load capacitance that could be ascribed to the drain-bulk capacitance of your inverter?

(d) What is the component of the load capacitance that could be ascribed to the two additional inverters your inverter is driving?

(e) Calculate t_{PHL} and t_{PLH}.

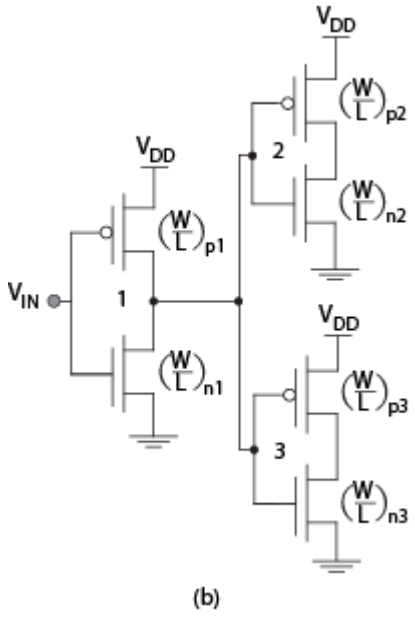

Figure PS6-1.1: A CMOS inverter driving two identical CMOS inverters as load. [Figure 5.24 (b) of H & S].

4. [25 points] **DC SPICE parameter extraction of an n-channel MOSFET (Contd.)**

This is a continuation of the exercise in which you used the ***Web-based Microelectronic Device Characterization*** system to characterize a MOSFET (http://iLab.mit.edu). From the measurements in problem Set #5, you extracted a model and a few DC SPICE parameters of the transistor in this problem set. The remaining DC SPICE parameters will be extracted in this Problem Set. The User Manual is available on the ***iLab*** homepage.

[**If you still have your measurements from Problem Set #5, please skip the measurement part of this problem.]**

In this problem, you will characterize an n-channel MOSFET. Select one of the devices labeled "**3μm nMOSFET**" under the "**Devices**" Menu. Take the measurements specified below and download the data to your local machine for additional graphing and further analysis. *Only download the data when you have satisfactory results*.

For the following measurements, hold V_{GS} between 0 and 3 V, and V_{DS} between 0 and 3 V. When relevant, vary V_{BS} between 0 and -3.0 V. For the SPICE parameter determination you will need the following structural information about the transistor. The gate length of this transistor is L = 3 μm, and the gate width is W = 20 μm. In this exercise, we do not distinguish between L and L_{eff} (see Section 4.6.1 in Howe & Sodini).

Below is the characterization assignment.

a. (5 points) Measure the ***output characteristics*** of the transistor. These are I_D vs. V_{DS} measurements with V_{GS} as the stepping parameter and V_{BS} = 0 V. Download the data to your local machine and plot the ***output characteristics*** using your favorite software tool. Turn in a printout of this graph.
b. (10 points) From the ***output characteristics***, extract the SPICE parameters **KP** and **LAMBDA** for the transistor (see Eq. 4.93 in Howe & Sodini). [It is advisable to determine **KP** using data taken at low V_{DS} values and **LAMDA** using the data taken at high V_{DS} values Use the MOSFET equations given in text or the notes and take appropriate derivatives]

c. (5 points) Using the SPICE parameter set just derived (and others from the last Problem Set i.e. the SPICE parameters **VTO**, **GAMMA** and **PHI**), plot the characteristics of the transistors (use Eqs. 4.93 and 4.94 in Howe & Sodini) and compare them with the measurement data. The most effective way to do this is to construct graphs that depict the measured data as individual dots and the model as continuous lines.

- Plot on the same graph the measured ***output characteristics*** of the MOSFET and those predicted by your SPICE model. Turn in this graph. Comment on the accuracy of the model.
- Plot on the same graph the measured ***transfer characteristics*** of the MOSFET and those predicted by your SPICE model. Turn in this graph. Comment on the accuracy of the model.