6.012 Electronic Devices and Circuits Fall 2008

Problem Set #5

Assigned: October 1, 2008
Due: October 8, 2008 at lecture

Reading Assignments:	09/30/06	Sections 4.1 - 4.3 of Howe & Sodini
	10/02/08	Sections 4.3 - 4.4 of Howe & Sodini
	10/07/08	Sections 4.5 – 4.6 of Howe & Sodini

PLEASE WRITE YOUR RECITATION SESSION TIME ON YOUR PROBLEM SET SOLUTION

1. [30 points] An n-MOSFET with n^+ - poly-silicon gate has the following physical parameters: gate length L = 0.5 μm, gate width W = 10 μm, oxide thickness t_{ox} = 10 nm and substrate doping $N_a = 10^{17}$ cm^{-3}. The device is biased as follows: V_{GS} = 2 V, V_{DS} = 2 V and V_{BS} = 0 V. Assume that the mobility of electrons in the inversion layer is μ_N = 400 cm^2 / V•s. Also assume that the source and drain regions are heavily doped i.e. n^+ -doping.
   (a) In what regime is the MOSFET biased? Justify your answer with appropriate calculations.
   (b) Calculate the electron density per unit area (Q_N/q) at the source end of the channel?
   (c) Determine the approximate extent of the depletion layer underneath the inversion layer at the source end of the channel?
   (d) What is the value of the body-to-source bias, V_{BS}, that would drive the MOSFET into cut off assuming that V_{GS} and V_{DS} remain the same?

2. [30 points] High dielectric constant dielectrics are being considered as gate insulator material for next generation CMOS devices. One such material is Hafnium Oxide, which has a dielectric constant of 25 ε_o. Assume the gate material is p^+-polysilicon $\phi_m = \phi_{p^+} = -0.55V$.
   (a) What is the thickness of Hafnium Oxide needed for a threshold voltage of V_{TOp} = -0.5 V, if the substrate doping is $N_d = 10^{17}$ cm^{-3}?
   (b) Find the corresponding backgate effect parameter, γ_p for the Hafnium Oxide gate thickness?
   (c) Find the current for the operating point Q (V_{SG}=1.5 V, V_{SD}=1.5 V, V_{SB} = 0 V)? *Assume the channel length L = 1 μm, the width W = 30 μm, the channel mobility is* μ_p *= 100* $cm^2V^{-1}s^{-1}$.
   (d) What is the electron velocity in the middle of the channel (i.e. y=L/2) for the same bias point Q (V_{SG}=1.5 V, V_{SD}=1.5 V, V_{SB} = 0 V)? *Assume the channel length L = 1 μm, the width W = 30 μm, the channel mobility is* μ_p *= 100* $cm^2V^{-1}s^{-1}$.

3. [40 points] **DC SPICE parameter extraction of an n-channel MOSFET**

This is an exercise in which you will use the ***Web-based Microelectronic Device Characterization*** system to characterize a MOSFET (http://iLab.mit.edu). From the measurements, you will also extract a model and a few DC SPICE parameters of the transistor in this problem set. The remaining DC SPICE parameters will be extracted in the next Problem Set. The User Manual is available on the ***iLab*** homepage.

In this problem, you will characterize an n-channel MOSFET. Select one of the devices labeled "**3μm nMOSFET**" under the "**Devices**" Menu. Take the measurements specified below and download the data to your local machine for additional graphing and further analysis. *Only download the data when you have satisfactory results.*

For the following measurements, hold V_{GS} between 0 and 3 V, and V_{DS} between 0 and 3 V. When relevant, vary V_{BS} between 0 and -3.0 V. For the SPICE parameter determination you will need the following structural information about the transistor. The gate length of this transistor is L = 3 μm, and the gate width is W = 20 μm. In this exercise, we do not distinguish between L and L_{eff} (see Section 4.6.1 in Howe & Sodini).

Below is the characterization assignment.

a. (5 points) Measure the ***output characteristics*** of the transistor. These are I_D vs. V_{DS} measurements with V_{GS} as the stepping parameter and V_{BS} = 0 V. Download the data to your local machine and plot the ***output characteristics*** using your favorite software tool. Turn in a printout of this graph.

b. (5 points) Measure the ***transfer characteristics*** of the transistor. These are I_D vs. V_{GS} measurements with V_{DS} as the stepping parameter and V_{BS} = 0 V. Download the data to your local machine and plot the ***transfer characteristics*** using your favorite software tool. Turn in a printout of this graph.

c. (5 points) Measure the ***backgate characteristics in the linear regime*** of the transistor. That is, I_D vs. V_{GS} measurements with V_{BS} as the stepping parameter for V_{DS} = 0.05 V. Download the data to your local machine and plot the ***backgate characteristics*** using your favorite software tool. Turn in a printout of this graph.

d. (15 points) From the ***backgate characteristics***, extract V_T as a function of V_{BS}. Make a plot of V_T as a function of V_{BS} and turn in a printout of this graph. From this graph, extract the SPICE parameters **VTO**, **GAMMA** and **PHI** for the transistor (see Eq. 4.94 in Howe & Sodini). Note that it is not really possible to extract both **GAMMA** and **PHI** accurately. Since **PHI** plays the role of $-2\phi_p$ (ϕ_p is the potential in the bulk), a suitable value for it should be in the range of 0.6 to 1.0. Pick a value in this range and extract the value of **GAMMA** that best matches the data. The SPICE parameter determination should not demand extensive numerical analysis. There is no need to do regressions or least-squares fits. You will continue the SPICE Parameter Extraction in the next problem set.