Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science

6.002 – Electronic Circuits
Spring 2006

Problem Set #11 Solutions

Introduction

This homework assignment focuses on the analysis and design of a system for playing back a digitally-stored audio signal. Additionally, this assignment serves as the pre-lab exercises for Lab #4, which will involve the construction, testing and demonstration of the audio playback system. *Consequently, you should save a copy of your results for use during Lab #4.*

A block diagram of the audio playback system is shown in Figure 1. At the center of the system is a digital memory in which 32,768 samples of the audio signal are stored. Each sample in the memory has a unique numerical address between 0 and 32,767, inclusive. Consecutive samples are stored at consecutive addresses.

To obtain 32,768 consecutive samples of the audio signal, 4.096 seconds of continuous analog audio signal are first sampled at an 8-kHz rate. The analog audio samples are then digitized by an 8-bit analog-to-digital converter. That is, the samples are quantized to take on one of 256 possible discrete digital values between 0 and 255, inclusive. Here, the digital value of 0 corresponds to the most positive signal voltage, and the digital value of 255 corresponds to the most negative signal voltage. The resulting digital data is then written into the memory.

To retrieve the stored audio signal samples in sequence at the proper rate, the memory is addressed by a counter which counts from 0 to 32,767 at an 8-kHz rate established by an external clock. After counting to 32,767 the counter returns to 0, and the retrieval process repeats itself. As the memory address increments, the corresponding data appears at the memory output. This data is converted back to an analog voltage in a piecewise constant manner by a digital-to-analog converter.

During the course of recording and playing back the analog audio signal, the signal is sampled in time, quantized in amplitude, and reconstructed in a piecewise constant manner. As you will learn in 6.003, this process introduces undesirable high-frequency components into the signal. To

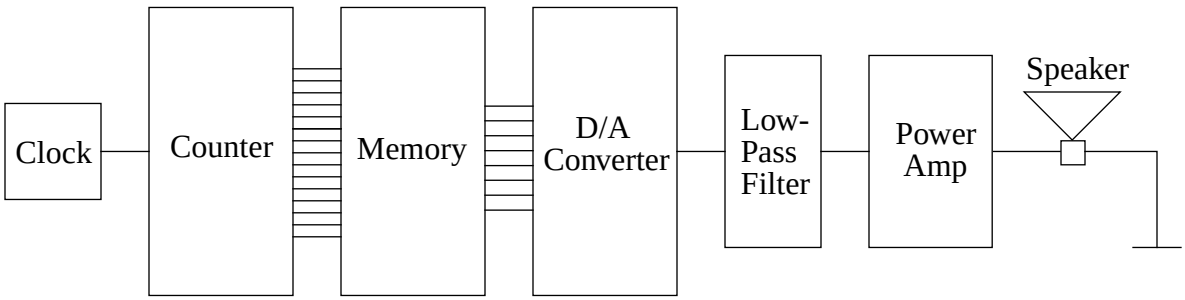

Figure 1: block diagram of the audio playback system.

minimize the perceived impact of these components, the signal is filtered by a low-pass filter after it is reconstructed by the digital-to-analog converter. Finally, the signal is amplified by a power amplifier which in turn drives a speaker. In Lab #4, you will use a piezo-electric speaker, which does not require much power. In this case, the final power-amplifier stage is not strictly necessary. Nonetheless, the stage is included here, and is used to implement volume control.

In the course of this homework assignment you will analyze and design four of the functional blocks shown in Figure 1. These blocks are the clock, the digital-to-analog converter, the low-pass filter and the power amplifier. In Lab #4, you will construct these blocks and verify that they perform as desired. Then, you will combine them with the counter, the read-only memory and the speaker to construct and demonstrate the entire audio play-back system. Since you will construct the system from the components in your 6.002 lab kit, your design of the blocks must account for the fact that the available components are limited.

Problem 1: The Clock

The circuit shown in Figure 2 is the system clock, which is a square-wave oscillator followed by a CMOS inverter; the inverter functions only as a (negative gain) buffer. The oscillator is constructed from another CMOS inverter, a resistor and a capacitor. Both inverters are powered between the positive supply voltage V_S and ground, and both exhibit the hysteretic input-output characteristic defined in the figure. The inverters are otherwise ideal.

(A) Assume that v_{CAP} has just charged up to V_H so that v_{OSC} has just switched to 0 V. How much time elapses before v_{CAP} decays to V_L, which in turn causes v_{OSC} to switch to V_S?

ANSWER: As shown in the Figure 3, the capacitor voltage now begins to decay from V_H towards 0 V. In this case, the capacitor voltage is given by

$$v_{CAP} = V_H e^{-t/RC}$$

where $t = 0$ is the time at which v_{OSC} just switches to 0 V. We must now solve for the time

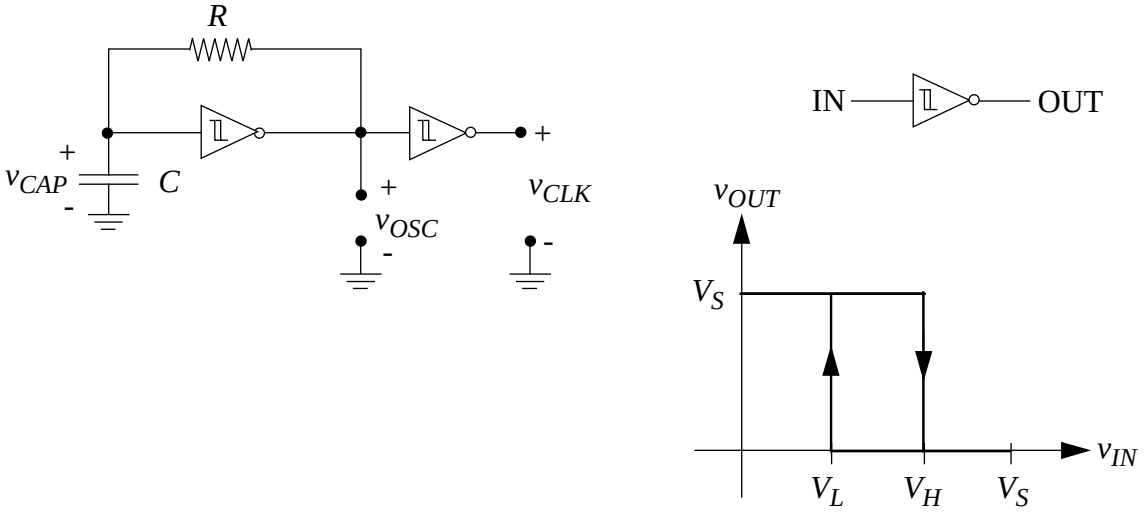

Figure 2: the system clock.

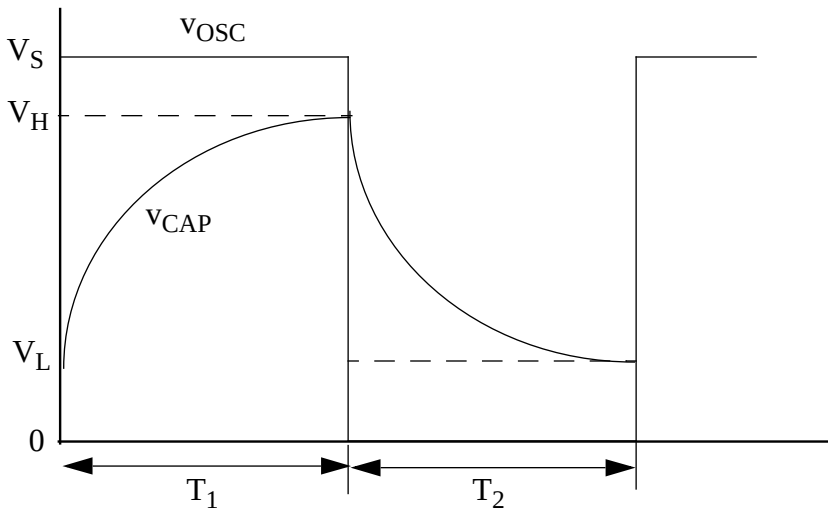

Figure 3: general clock waveforms. Note that the $v_{\rm CAP}$ curve is not drawn well. It seems to show $V_{\rm CAP}$ settling to $v_{\rm H}$ and $v_{\rm L}$ instead of $v_{\rm S}$ and 0 V.

at which $v_{\rm CAP} = V_{\rm L}$; this time is denoted by T_2 in Figure 3. Thus,

$$V_{\rm L} = V_{\rm H} e^{-T_2/RC}$$

so that

$$T_2 = RC \ln\left(\frac{V_{\rm H}}{V_{\rm L}}\right) \quad .$$

(B) Assume that $v_{\rm CAP}$ has just decayed to $V_{\rm L}$ so that $v_{\rm OSC}$ has just switched to $V_{\rm S}$. How much time elapses before $v_{\rm CAP}$ charges up to $V_{\rm H}$, which in turn causes $v_{\rm OSC}$ to switch to 0 V?

ANSWER: Again as shown in Figure 3, the capacitor voltage now begins to rise from $V_{\rm L}$ towards $V_{\rm S}$. In this case, the capacitor voltage is given by

$$v_{\rm CAP} = V_{\rm S} + (V_{\rm L} - V_{\rm S}) e^{-t/RC}$$

where $t = 0$ is the time at which just switches to $V_{\rm S}$. We must now solve for the time at which $v_{\rm CAP} = V_{\rm H}$; this time is denoted by T_1 in the Figure 3. Thus,

$$V_{\rm H} = V_{\rm S} + (V_{\rm L} - V_{\rm S}) e^{-T_1/RC}$$

so that

$$T_1 = RC \ln\left(\frac{V_{\rm S} - V_{\rm L}}{V_{\rm S} - V_{\rm H}}\right) \quad .$$

(C) Determine the frequency of the oscillator in terms of R, C, $V_{\rm L}$, $V_{\rm H}$ and $V_{\rm S}$.

ANSWER: The period T of the oscillator is

$$T = T_1 + T_2 = RC \ln\left(\frac{(V_{\rm S} - V_{\rm L})V_{\rm H}}{(V_{\rm S} - V_{\rm H})V_{\rm L}}\right) \quad .$$

The frequency f is the inverse of the period T, and is given by

$$f = \frac{1}{T} = \frac{1}{RC \ln\left(\frac{(V_{\rm S} - V_{\rm L})V_{\rm H}}{(V_{\rm S} - V_{\rm H})V_{\rm L}}\right)} \quad .$$

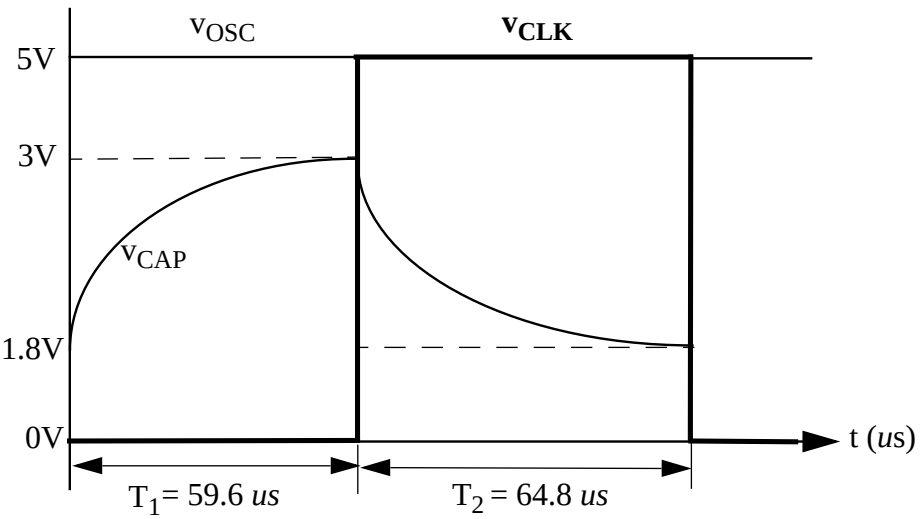

Figure 4: clock waveforms given the as-designed component values. Again, note that the $v_{\rm CAP}$ curve is not drawn well. It seems to show $V_{\rm CAP}$ settling to $v_{\rm H}$ and $v_{\rm L}$ instead of $v_{\rm S}$ and 0 V.

(D) Assume that $V_{\rm L} = 1.8$ V, $V_{\rm H} = 3.0$ V and $V_{\rm S} = 5.0$ V. Choose values for R and C so that the oscillator oscillates at or very near 8-kHz. Since oscillator frequency alone under specifies R and C, there is no single correct choice. Therefore, choose values for R and C that are easily implemented with the components in the 6.002 lab kit.

ANSWER: A frequency of $f = 8$ KHz is equivalent to $T = 1/f = 125$ μs. Pick $C = 0.0047$ μF, and solve for R using the equation from Part (C). This yields

$$R = \frac{T}{C \ln\left(\frac{(V_{\rm S}-V_{\rm L})V_{\rm H}}{(V_{\rm S}-V_{\rm H})V_{\rm L}}\right)} = 27 \text{ K}\Omega \quad ,$$

which is a standard resistor value.

(E) For the choice of R and C from Part (D), sketch and clearly label a single graph that displays $v_{\rm CAP}$, $v_{\rm OSC}$ and $v_{\rm CLK}$ as a function of time over one period of oscillation.

ANSWER: The graph is shown in Figure 4. Using the equations from Parts (A) and (B), $T_1 = 59.6$ μs and $T_2 = 64.8$ μs. These times are included in Figure 4. Notice that $T_1 \neq T_2$. This does not affect the operation of the counter because the counter in Figure 1 is triggered only by either the rising or the falling edge of $v_{\rm CLK}$, but not both.

Problem 2: The Digital-To-Analog Converter

The circuit shown in Figure 5 is the digital-to-analog converter. The voltage sources $v_{\rm DB0}$ through $v_{\rm DB7}$ represent the voltages supplied by the eight data bits of the digital memory, DB0 through DB7. These voltages will be approximately 5 V when the corresponding data bit is a logical high, and approximately 0 V when the corresponding data bit is a logical low. The voltage $v_{\rm OFF}$, which is set by a potentiometer, is an offset voltage that is used to center the output of the converter around 0 V. Assume that the op-amp in the converter is ideal.

(A) Determine $v_{\rm DAC}$ as a function of $v_{\rm DB0}$ through $v_{\rm DB7}$, and $v_{\rm OFF}$. Hint: use superposition.

Answer: Let $v_{\rm OFF} = 0$ and compute the current i going through R_8 according to

$$i = \frac{0 - v_{\rm DAC1}}{R_8} = \sum_{i=0}^{7} \frac{v_{{\rm DB}i}}{R_i} \quad .$$

This gives $v_{\rm DAC1}$, the contribution to the output voltage from the inputs. It is

$$v_{\rm DAC1} = -\sum_{i=0}^{7} \frac{R_8}{R_i} v_{{\rm DB}i} \quad .$$

Next, setting $v_{{\rm DB}i} = 0$ gives $v_{\rm DAC2}$, the contribution to the output voltage from $v_{\rm OFF}$. It is

$$v_{\rm DAC2} = v_{\rm OFF}(1 + \frac{R_8}{R})$$

where $R = R_0||R_1||...R_7$. The total output voltage is

$$v_{\rm DAC} = v_{\rm DAC1} + v_{\rm DAC2} = -\sum_{i=0}^{7} \frac{R_8}{R_i} v_{{\rm DB}i} + v_{\rm OFF}(1 + \frac{R_8}{R}) \quad .$$

(B) With $v_{\rm OFF} = 0$ V, the output of the digital-to-analog converter should span the range of 0 V to -2.5 V. Thus, the output of the converter should be given by

$$v_{\rm DAC} = -2.5 \text{ V} \sum_{i=0}^{7} \frac{2^i}{255} {\rm DB}i$$

where each data bit DBi takes on the numerical value of 1 when high and 0 when low. In this manner, each successive data bit from DB0 to DB7 is given a voltage weighting twice that of the preceding data bit, making it possible for the converter to output voltages from 0 V to -2.5 V in steps of $-2.5/255$ V. Given this, what must be the relationships between the values of R_0 through R_7, and R_8?

The voltage rating of the piezo-electric speaker used in Lab #4 is approximately ± 12.5 V. Since the low-pass filter and power amplifier between the converter and the speaker will be

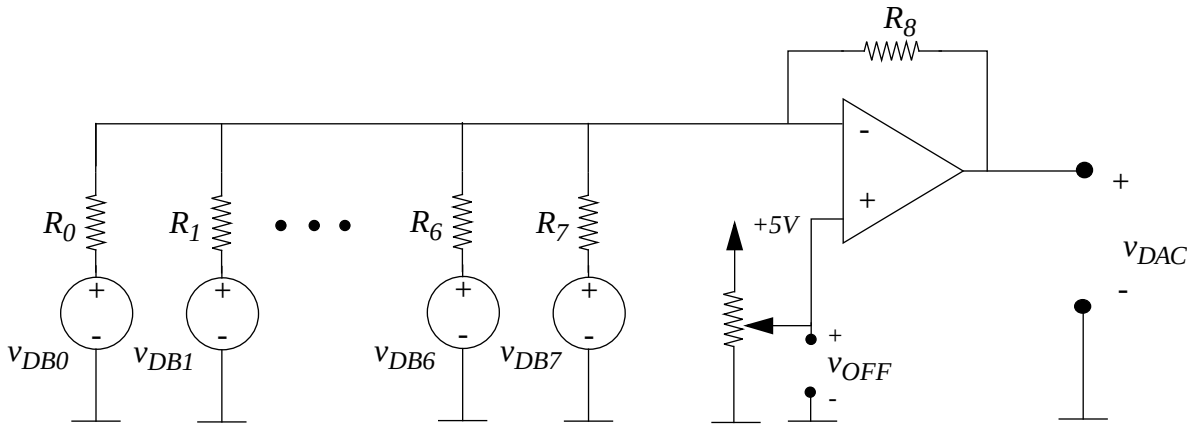

Figure 5: the digital-to-analog converter.

designed to provide a total gain of 10 over the frequency range of interest, the output range of the analog-to-digital converter must be designed to match the speaker rating divided by 10. This is why the range is chosen to be 0 V to -2.5 V, with $v_{\rm OFF} = 0$. Note further that the output range of the converter is negative. This is because the converter is based upon the inverting op-amp amplifier configuration.

Answer: The resistance progression for R_0 through R_7 is $R_0 = 2R_2 = 4R_2 = ... \ 128R_7$. If only DB0 is set to 1, then from the results of Part (A),

$$\frac{-2.5 \text{ V}}{255} = -\frac{R_8}{R_0} \ 5 \text{ V} \quad \Rightarrow \quad \frac{R_8}{R_0} = \frac{1}{510} \quad .$$

(C) The role of $v_{\rm OFF}$ is to offset the output of the digital-to-analog converter so that it is centered around 0 V. That is, with DB0 through DB7 all low, $v_{\rm DAC}$ should be 1.25 V, and with DB0 through DB7 all high, $v_{\rm DAC}$ should be -1.25 V. Given this, what must be the value of $v_{\rm OFF}$?

Answer: From the results of Part (A),

$$\begin{aligned} R &= R_0||R_1||...R_7 \\ &= R_0(1||\tfrac{1}{2}||\tfrac{1}{4}||...\tfrac{1}{128}) \\ &= R_0/(1+2+4+... \ 128) \\ &= R_0/255 \quad . \end{aligned}$$

We want to have $V_{\rm DAC} = 1.25$ V when $v_{{\rm DB}i} = 0$ V. This leads to

$$\begin{aligned} 1.25 \text{ V} &= v_{\rm OFF}(1 + \tfrac{R_8}{R}) \\ &= v_{\rm OFF}(1 + 255\tfrac{R_8}{R_0}) \\ v_{\rm OFF} &= 0.83V \quad . \end{aligned}$$

(D) Based on the results of Part (B), choose values for R_0 through R_7, and R_8. Since the results of Part (B) under specify R_0 through R_7, and R_8, there is no single correct choice. Further, since arbitrary valued resistors are not available, the results of Part (B) can not be satisfied exactly. Therefore, choose values for R_0 through R_7, and R_8 that are easily implemented with the components in the 6.002 lab kit, and that satisfy the results of Part (B) as best as possible. You may wish to use series and/or parallel combinations to construct one or more of R_0 through R_8.

Answer: Table 1 presents one set of possible values.

Problem 3: The Low-Pass Filter

The circuit shown in Figure 6 is the low-pass filter. It is a second-order filter, and is driven by the output of the digital-to-analog converter. Its purpose is to remove the high-frequency components of the audio signal that result from the sampling, quantization and reconstruction of that signal. Assume that the op-amp in the filter is ideal.

(A) Assume that the low-pass filter operates in sinusoidal steady state with $v_{\rm DAC} = \Re\{\tilde{v}_{\rm DAC}e^{j\omega t}\}$ and $v_{\rm LPF} = \Re\{\tilde{v}_{\rm LPF}e^{j\omega t}\}$ where $\tilde{v}_{\rm DAC}$ and $\tilde{v}_{\rm LPF}$ are complex amplitudes. Find the input-output transfer function $H_{\rm LPF}(\omega)$ of the filter where $H_{\rm LPF}(\omega) \equiv \tilde{v}_{\rm LPF}/\tilde{v}_{\rm DAC}$.

Resistor	Ideal Value [Ω]	Actual Value [Ω]
R_0	154K	150K
R_1	76.8K	82K
R_2	38.4K	39K
R_3	19.2K	18K
R_4	9.6K	10K
R_5	4.8K	4.7K
R_6	2.4K	2.2K
R_7	1.2K	1.2K
R_8	302	$560 \parallel 680 = 307$

Table 1: a possible set of resistor values for the design of the D/A converter.

ANSWER: One straight forward way to analyze this circuit is to use the node method. There are three nodes in the circuit, but the ideal op-amp model allows us to assume that $v_+ = v_- = v_{\text{LPF}}$. By using this simplification, we can avoid writing a node equation for the output node.

Define the internal node voltage as $\tilde{e}$. For the v_+ node,

$$\frac{\tilde{v}_{\text{LPF}}}{\frac{1}{j\omega C_2}} + \frac{\tilde{v}_{\text{LPF}} - \tilde{e}}{R} = 0 \quad .$$

For the internal node,

$$\frac{\tilde{v}_{\text{LPF}} - \tilde{e}}{\frac{1}{j\omega C_1}} + \frac{\tilde{v}_{\text{LPF}} - \tilde{e}}{R} + \frac{\tilde{v}_{\text{DAC}} - \tilde{e}}{R} = 0 \quad .$$

Next, solve the first equation for $\tilde{e}$ and substitute the result into the second equation. Mathematically, it is irrelevant how the equations are solved, but from a practical viewpoint, it tends to be easier to solve the simplest equation first, and substitute the result into the more complicated equation. In this case,

$$\tilde{e} = \tilde{v}_{\text{LPF}}(1 + j\omega R C_2) \quad .$$

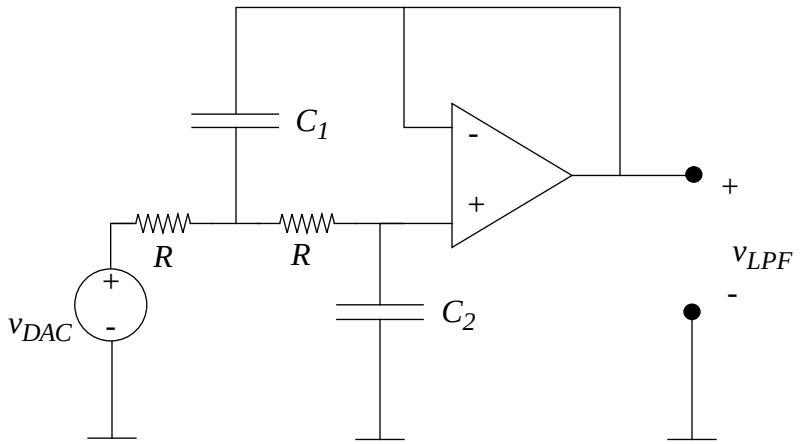

Figure 6: the low-pass filter.

Next, substituting this expression for $\tilde{e}$ into the second equation, and factoring out $\tilde{v}_{\rm LPF}$, yields

$$\tilde{v}_{\rm LPF}\left(\frac{(1+j\omega RC_2)-1}{\frac{1}{j\omega C_1}}+\frac{(1+j\omega RC_2)-1}{R}+\frac{1+j\omega RC_2}{R}\right)=\frac{\tilde{v}_{\rm DAC}}{R} \quad .$$

Finally, solving for $\frac{\tilde{v}_{\rm LPF}}{\tilde{v}_{\rm DAC}}$ yields

$$H_{\rm LPF}(\omega)=\frac{\tilde{v}_{\rm LPF}}{\tilde{v}_{\rm DAC}}=\frac{1}{1-\omega^2R^2C_1C_2+2j\omega RC_2} \quad .$$

(B) Using the results of Part (A), find the magnitude and phase of $H_{\rm LPF}(\omega)$.

ANSWER: The solution is

$$|H_{\rm LPF}(\omega)|=\frac{1}{\sqrt{(1-\omega^2R^2C_1C_2)^2+(2\omega RC_2)^2}}$$

$$\angle H_{\rm LPF}(\omega)=\arctan\left(\frac{-2\omega RC_2}{1-\omega^2R^2C_1C_2}\right) \quad .$$

(C) There is no best design for the low-pass filter to meet the needs of the audio playback system. However, with the appropriate choice of C_1, C_2 and R, the transfer function of one good design will take the form

$$|H_{\rm LPF}(\omega)|=\frac{1}{1+(\omega/\omega_{\rm LPF})^2}$$

where $\omega_{\rm LPF}$ is a specified frequency. For this design, show that the low-frequency and high-frequency asymptotes of $|H_{\rm LPF}(\omega)|$ intersect at $\omega=\omega_{\rm LPF}$, and therefore that $\omega_{\rm LPF}$ is the frequency that delineates the pass band of the low-pass amplifier.

ANSWER: The low and high frequency asymptotes are calculated by including only the lowest and highest order ω terms, respectively. Continue to simplify in this manner until you are left with only the term(s) containing the dominant power of ω. For $\omega \ll \omega_{\rm LPF}$ we drop the ω^2 term because it is much less than 1. The result is

$$|H_{\rm LPF}(\omega \ll \omega_{\rm LPF})| \approx 1 \quad .$$

For $\omega \gg \omega_{\rm LPF}$ we drop the 1 because it is much less than the ω^2 term. The result is

$$|H_{\rm LPF}(\omega \ll \omega_{\rm LPF})| \approx \frac{1}{(\omega/\omega_{\rm LPF})^2} \quad .$$

Solving for the intersection of these asymptotes gives the expected result of $\omega=\omega_{\rm LPF}$. This is the cut-off frequency of the low-pass filter.

(D) What constraints must be imposed on C_1, C_2 and R to obtain the low-pass filter transfer function described in Part (C)?

ANSWER: Our current equation for $|H_{\rm LPF}(\omega)|$ does not look much like our desired result, so expand the denominator. This yields

$$|H_{\rm LPF}(\omega)|=\frac{1}{\sqrt{1-2\omega^2R^2C_1C_2+(\omega^2R^2C_1C_2)^2+4\omega^2R^2C_2^2}} \quad .$$

If we let $C_1 = C_2 = C$, then we can easily factor that equation to obtain

$$|H_{\rm LPF}(\omega)| = \frac{1}{\sqrt{1 + 2\omega^2 R^2 C^2 + (\omega^2 R^2 C^2)^2}} = \frac{1}{\sqrt{(1 + \omega^2 R^2 C^2)^2}} = \frac{1}{1 + \omega^2 R^2 C^2}$$

This final form looks a lot more like what we want. We can see that $\omega_{\rm LPF} = 1/(RC)$.

(E) Given that the low-pass filter is to be designed as described in Part (C), use the results of Part (D) to choose values for C_1, C_2 and R so that $\omega_{\rm LPF} \approx 2\pi \times 4000$ rad/s. Since the results of Part (D) under specify C_1, C_2 and R, there is no single correct choice. Therefore, choose C_1, C_2 and R so that they are easily implemented with the components in the 6.002 lab kit.

ANSWER: We see that $RC = 1/(2\pi \times 4000) \approx 3.98 \times 10^{-5}$. To choose a good value for R and C we need to consider the parasitic elements in the circuit and the device non-idealities. There are parasitic capacitances between the pins in the protoboard. Those tend to be on the order of single picofarads. We need our value of C to be much larger than the parasitic capacitances so that it sets the total capacitance. The resistor choice is effected by the presence of source resistances and input and output resistances of the op-amps. In addition there are parasitic inductances. If the resistance is too small, the parasitic RLC circuits may be underdamped and cause ringing. In general we choose a resistance of a few kΩ. For example, let $R = 3.9$ kΩ, which requires that $C = 0.0102$ μF. Since this is much larger than a picofarad, and we have a 0.01 μF capacitor in our lab kit, it seems that these values are a good choice. Just to check, we see that our $RC = 3.9 \times 10^{-5}$ s. This is about 2% off the desired frequency, which is much less than the error of either the real resistor or the capacitor.

(F) Given the choice of C_1, C_2 and R from Part (E), determine $\omega_{\rm LPF}$, and plot both the log-magnitude and phase of $H_{\rm LPF}(\omega)$ against log-frequency for $2\pi \times 10^1$ rad/s $\leq \omega \leq 2\pi \times 10^5$ rad/s.

ANSWER: From above we see that $\omega_{\rm LPF} = 2.56 \times 10^4 = 2\pi \times 4081$ rad/s. Figure 7 shows the frequency response.

Problem 4: The Power Amplifier

Figure 8 shows the output of the low-pass filter driving the power amplifier, which in turn drives the speaker. Ordinarily, the power amplifier would be constructed from a high-power op-amp, or equivalent, because a typical low-power op-amp can not supply the current, and hence the power, required to drive a magnetic speaker. However, this will not be the case in Lab #4, during which the speaker will be a low-power piezo-electric speaker. In this case, a low-power op-amp is adequate.

Because there exists a coupling capacitor at its input, the power amplifier behaves like a high-pass filter. In this way, the amplifier is designed to prevent a possibly damaging DC voltage from being applied to the speaker. This is a particularly serious issue in the case of magnetic speakers, and a less serious issue for the case of piezo-electric speakers. Such a voltage component could be present in $v_{\rm LPF}$ if, for example, $v_{\rm OFF}$ in the analog-to-digital converter is not properly adjusted to balance the output of the converter.

(A) Assume that the power amplifier operates in sinusoidal steady state with $v_{\rm LPF} = \Re\{\tilde{v}_{\rm LPF} e^{j\omega t}\}$ and $v_{\rm OUT} = \Re\{\tilde{v}_{\rm OUT} e^{j\omega t}\}$ where $\tilde{v}_{\rm LPF}$ and $\tilde{v}_{\rm OUT}$ are complex amplitudes. Find the input-output transfer function $H_{\rm AMP}(\omega)$ of the power amplifier where $H_{\rm AMP}(\omega) \equiv \tilde{v}_{\rm OUT}/\tilde{v}_{\rm LPF}$.

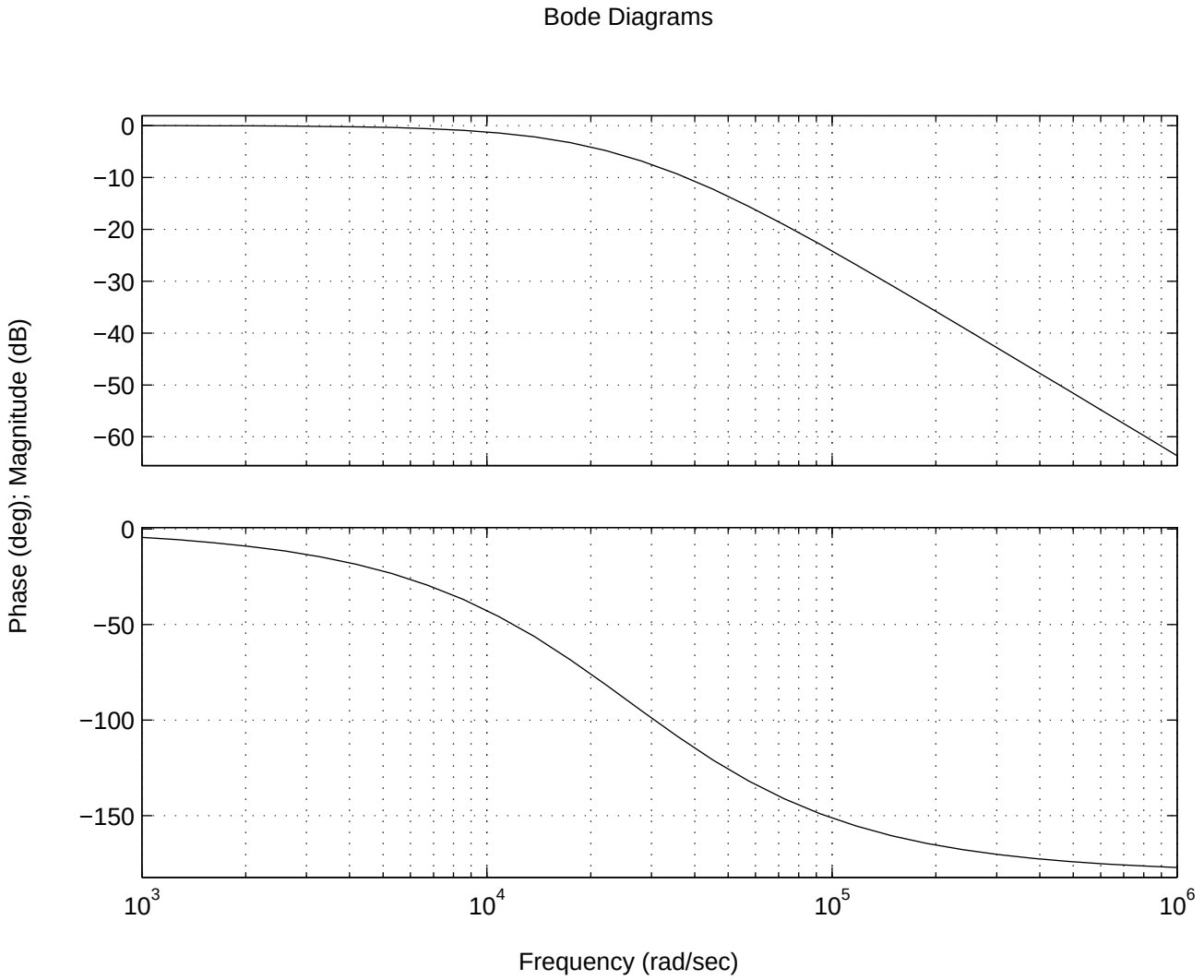

Figure 7: frequency response of the low-pass filter.

ANSWER: We can use the equation for an inverting op-amp amplifier to write down the answer directly.

$$H_{\rm AMP}(\omega) = \frac{\tilde{v}_{\rm OUT}}{\tilde{v}_{\rm LPF}} = \frac{-R_2}{R_1 + \frac{1}{j\omega C}} = \frac{-j\omega R_2 C}{1 + j\omega R_1 C} \quad .$$

Remember that this comes from assuming that $v_- = v_+ = 0$, and that the current into $v_- = 0$.

(B) Using the result of Part (A), find the magnitude and phase of $H_{\rm AMP}(\omega)$.

ANSWER: The solution is

$$|H_{\rm LPF}(\omega)| = \frac{\omega R_2 C}{\sqrt{1 + \omega^2 R_1^2 C^2}}$$

$$\angle H_{\text{LPF}}(\omega) = \arctan\left(\frac{1}{\omega R_1 C}\right) \quad .$$

(C) Let ω_{AMP} be the frequency at which the low-frequency and high-frequency asymptotes of $|H_{\text{AMP}}(\omega)|$ intersect. Determine ω_{AMP} in terms of R_1, R_2 and C.

ANSWER: This problem can be approached just as was Problem 3C. For $\omega \ll R_1 C$ we drop the ω^2 term in the denominator because it is much less than 1. The result is

$$|H_{\text{LPF}}(\omega \ll R_1 C)| \approx \omega R_2 C$$

which goes to zero as ω goes to zero. This matches our intuition that the capacitor becomes an open circuit at low frequencies. For $\omega \gg R_1 C$ we drop the 1 in the denominator because it is much less than the ω^2 term. The result is what we expect by noticing that the capacitor behaves like a short at high frequencies. It is that

$$|H_{\text{LPF}}(\omega \ll R_1 C)| \approx \frac{R_2}{R_1} \quad .$$

Solving for the intersection of the asymptotes gives the expected result of $\omega = \frac{1}{R_1 C} = \omega_{\text{AMP}}$. This is the cut-off frequency of the power amplifier.

(D) Choose values for R_1, R_2 and C so that $\omega_{\text{AMP}} \leq 2\pi \times 100$ Hz, and $|H_{\text{AMP}}(\omega)| = 10$ for $\omega \gg \omega_{\text{AMP}}$. Since these conditions alone under specifyR_1, R_2 and C, there is no single correct choice. Therefore, choose values for R_1, R_2 and C that are easily implemented with the components in the 6.002 lab kit.

ANSWER: $|H_{\text{AMP}}(\omega)| = 10$ requires that $R_1 = 0.1 R_2 \equiv R$. So now we only need to choose two values, R and C. The key here is that $RC > 1/(2\pi \times 100) \approx 1.59 \times 10^{-3}$ s. Using the same criteria as in the previous problem, one possible combination is $R_1 = R = 15$ kΩ, $R_2 = 10R = 150$ kΩ and $C = 0.1$ μF. To check: $\omega = 1/(R_1 C) = 666.7$ rad/s $= 2\pi \times 106$ Hz.

(E) If the original analog signal is recorded with a reduced amplitude, then the power amplifier must compensate by providing more than a 10-fold gain. To provide this gain, R_2 is implemented with a fixed resistor in series with a potentiometer. Design such a modification that provides a variable gain of 10 to 20. Note that the 6.002 lab kit has a limited number of potentiometers.

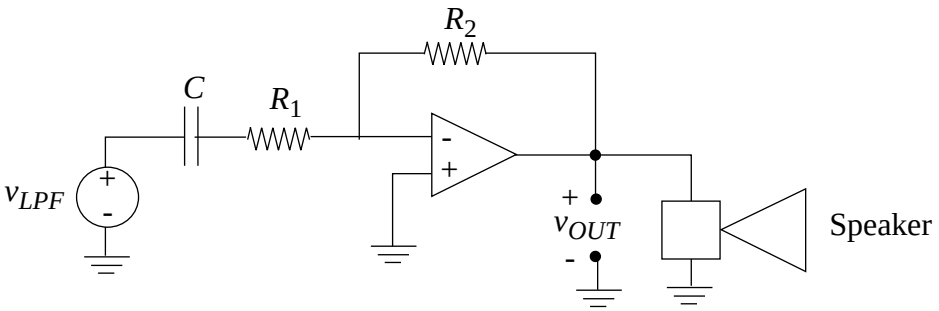

Figure 8: the power amplifier.

ANSWER: When we choose values for the potentiometer and R, we still need to obey the restriction above that $R_1 C > 1/(2\pi \times 100) \approx 1.59 \times 10^{-3}$.

Let's use a 100 kΩ potentiometer, as it is close to the 150 kΩ we found above, and place this in series with a fixed 100 kΩ resistor. We know that the ratio of the feedback resistor R_2 to the input resistor R_1 must be variable from 10 to 20. Therefore, R_1 must be 10 kΩ. When the potentiometer is at one extreme of its travel, its resistance is zero, and the power amp has a high-frequency gain of 10. At the other end, the potentiometer has a resistance of 100 kΩ, and the power amp has a high-frequency gain of 20. Finally, to satisfy the condition from Part (D), let $C = 0.2$ μF. We can implement this with two 0.1 μF capacitors in parallel. In this case, $R_1 C = 2$ ms, and $1/2\pi R_1 C = 80$ Hz.

Problem 5: Connecting The Blocks

In the complete audio playback system the output of the digital-to-analog converter is connected directly to the input of the low-pass filter, and the output of the low-pass filter is connected directly to the input of the power amplifier, as shown in Figure 1. Thus, the filter loads the converter, and the amplifier loads the filter. Explain why this loading could be ignored in Problems 2, 3 and 4. That is, explain why the converter, filter and amplifier may each be analyzed and designed in isolation.

ANSWER: The key to this simplicity is the op-amp. Using the ideal model of the op-amp (which turns out to be a relatively accurate model) we see that the output of each stage is independent of the amount of current supplied. That is to say, the op-amp in the digital-to-analog converter has the same output value no matter how much current the low-pass filter draws. Its Thevenin equivalent resistance is nearly zero so that the subsequent stage in the system does not load down the op-amp. Similarly, the op-amps in the low-pass filter and output stage maintain the same output voltage regardless of the current drawn.

Of course none of the op-amps are completely ideal. The reason we have the final power stage is precisely because the 741 op-amp we are using for the other stages might not supply enough current to drive a magnetic speaker. Even the power op-amp will show some output resistance, that is, the output will change when the speaker is attached. However, within their designed region of operation, the op-amps will be highly insensitive to loading.