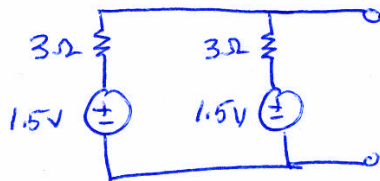


Exercise 3.1

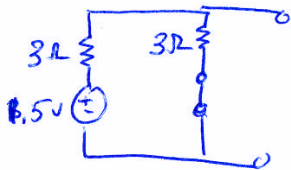
We are given  $V_{oc} = 1.5V$  and  $i_{sc} = 0.5A$  for one battery.

$$R_{th} = \frac{V_{th}}{i_{sc}} = 3\Omega$$

The parallel battery configuration can be drawn as:



Find  $V_{oc}$  &  $i_{sc}$  for this ckt using superposition.



Considering 1 supply:

$$V_{oc1} = \frac{3\Omega}{3\Omega + 3\Omega} \cdot 1.5V = \frac{3}{4}V$$

$$i_{sc1} = \frac{1.5V}{3\Omega} = \frac{1}{2}A$$

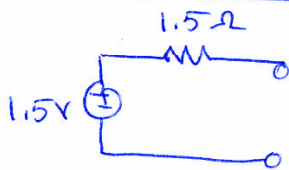
For the total circuit:

$$V_{oc} = 1.5V$$

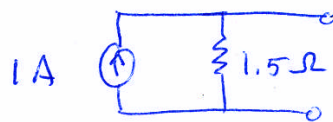
$$i_{sc} = 1A$$

$$R_{th} = 1.5\Omega$$

Thevenin Equivalent



Norton Equivalent



We know that  $P = \frac{V^2}{R} = i^2 R$ . We want to find the load resistor to deliver the maximum power. (2)

$$P_{\max} = \frac{V_{\text{th}}^2}{R_{\text{th}} + R_L} = \left( \frac{V_{\text{th}}}{R_{\text{th}} + R_L} \right)^2 \cdot R_L$$

We want to maximize power with respect to  $R_L$

$$P_{\max}(R_L) = R_L \left( \frac{V_{\text{th}}}{R_{\text{th}} + R_L} \right)^2$$

$$\frac{d}{dR_L} P_{\max}(R_L) = \frac{2V_{\text{th}}^2 (R_{\text{th}} + R_L)^2 - 4R_L (R_{\text{th}} + R_L) V_{\text{th}}^2}{(R_{\text{th}} + R_L)^4} = 0$$

$$\Rightarrow R_L = R_{\text{th}} = 1.5 \Omega$$

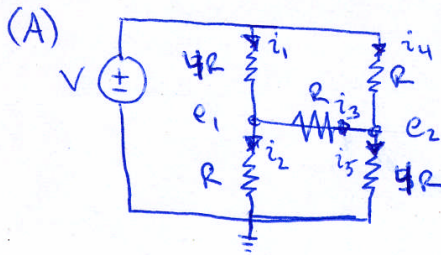
At this resistance, the power is:

$$P_{\max} = 0.75 \text{ W}$$

$$V_R = \frac{1.5 \Omega}{1.5 \Omega + 1.5 \Omega} \cdot 1.5 \text{ V} = \frac{3}{4} \text{ V}$$
$$i_R = \frac{1.5 \text{ V}}{3 \Omega} = \frac{1}{2} \text{ A}$$

### Exercise 3.2

(3)



Writing the node equations:

$$e_1: \frac{V - e_1}{4R} - \frac{e_1 - e_2}{R} - \frac{e_1}{R} = 0 \quad (1)$$

$$e_2: \frac{e_1 - e_2}{R} + \frac{V - e_2}{R} - \frac{e_2}{4R} = 0 \quad (2)$$

From (1):  $9e_1 - 4e_2 = V$

(2):  $-4e_1 + 9e_2 = 4V$

$$\begin{bmatrix} 9 & -4 \\ -4 & 9 \end{bmatrix} \begin{bmatrix} e_1 \\ e_2 \end{bmatrix} = \begin{bmatrix} V \\ 4V \end{bmatrix}$$

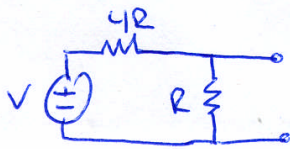
$\Rightarrow$

$$e_1 = \frac{5}{13}V \approx 0.38V$$

$$e_2 = \frac{8}{13}V \approx 0.62V$$

(B) Since the top node of Network A ~~can~~ is connected to the voltage source, both resistors will see the same voltage above them. Therefore this circuit will be the same if there is a split between the two resistors and each half is connected to an identical voltage source. This would not be true if current sources were used.

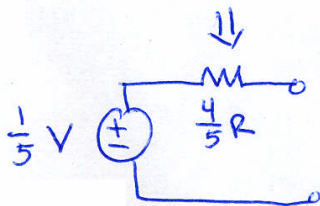
Combine Left Half:



$$V_{th} = \frac{R}{4R + R} V = \frac{1}{5} V$$

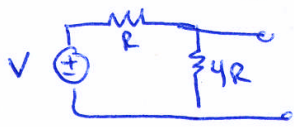
$$I_{sc} = \frac{V}{4R}$$

$$R_{th} = \frac{4}{5} R$$



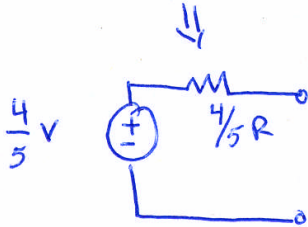
(4)

Combining the Right Half:

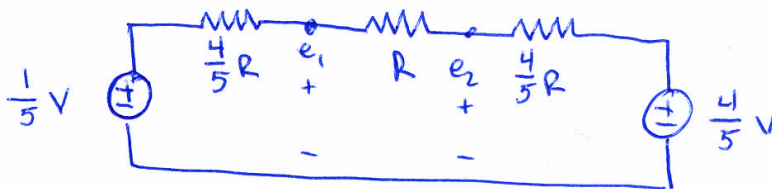


$$V_{oc} = \frac{4R}{R+4R} V = \frac{4}{5} V \quad ; \quad i_{sc} = \frac{V}{R}$$

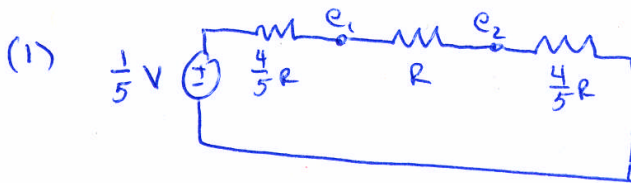
$$R_{th} = \frac{V_{oc}}{i_{sc}} = \frac{4}{5} R$$



Redrawing Network B:

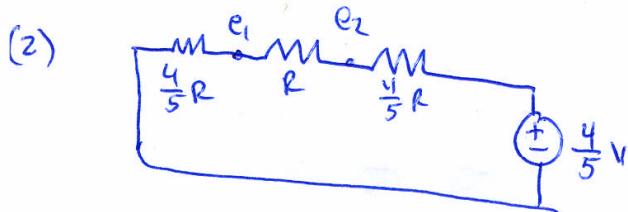


Using Superposition:



$$e_1 = \frac{R + \frac{4}{5}R}{\frac{4}{5}R + R + \frac{4}{5}R} \cdot \frac{1}{5} V = \frac{9}{65} V$$

$$e_2 = \frac{\frac{4}{5}R}{\frac{4}{5}R + R + \frac{4}{5}R} \cdot \frac{1}{5} V = \frac{4}{65} V$$



$$e_1 = \frac{\frac{4}{5}R}{\frac{4}{5}R + R + \frac{4}{5}R} \cdot \frac{4}{5} V = \frac{16}{65} V$$

$$e_2 = \frac{R + \frac{4}{5}R}{\frac{4}{5}R + R + \frac{4}{5}R} \cdot \frac{4}{5} V = \frac{36}{65} V$$

Combining (1) & (2):

$$e_1 = \frac{9}{65} V + \frac{16}{65} V = \frac{5}{13} V$$

$$e_2 = \frac{4}{65} V + \frac{36}{65} V = \frac{8}{13} V$$

Problem 3.1

5

(A) From the constitutive relation:

$$V_R = I_R \cdot R$$

$$I_R = I_S \left( e^{\frac{V_D}{kT/q}} - 1 \right) \quad \xrightarrow{\text{Solving for } V_D} \quad V_D = \frac{kT}{q} \cdot \ln \left[ \frac{I_R}{I_S} + 1 \right]$$

$$V_{IN} = V_D + V_R$$

$$V_{IN} = \frac{kT}{q} \cdot \ln \left[ \frac{I_R}{I_S} + 1 \right] + I_R \cdot R$$

(B) Using the approximation that  ~~$I_R$~~   $I_R$  is large:

$$I_R \approx I_S e^{\frac{V_D}{kT/q}}$$

From small-signal analysis:

$$z_r = \left. \frac{dI_R}{dV_D} \right|_{V_D = V_D} \cdot v_d = \frac{I_S}{kT/q} e^{\frac{V_D}{kT/q}} \cdot v_d = \frac{I_R}{kT/q} v_d$$

$$v_d = v_{in} - v_r$$

$$v_r = z_r \cdot R$$

$$\Rightarrow v_r = \frac{I_R}{kT/q} (v_{in} - v_r) R$$

$$v_r \left[ \frac{I_R \cdot R}{kT/q} + 1 \right] = \frac{I_R \cdot R}{kT/q} v_{in}$$

$$v_r = \frac{\frac{I_R \cdot R}{kT/q}}{\frac{I_R \cdot R}{kT/q} + 1} v_{in}$$

6

(C) From the constitutive relation:

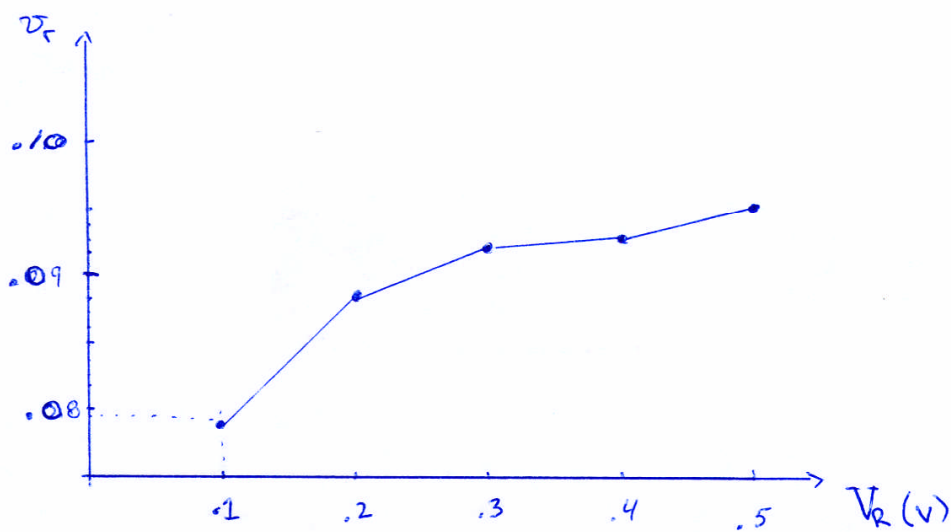
$$V_R = I_R \cdot R \Rightarrow I_R = \frac{V_R}{R}$$

Plugging into the answer for (B):

$$v_F = \frac{V_R}{V_R + \frac{kT}{q}} \cdot v_{in}$$

(D)

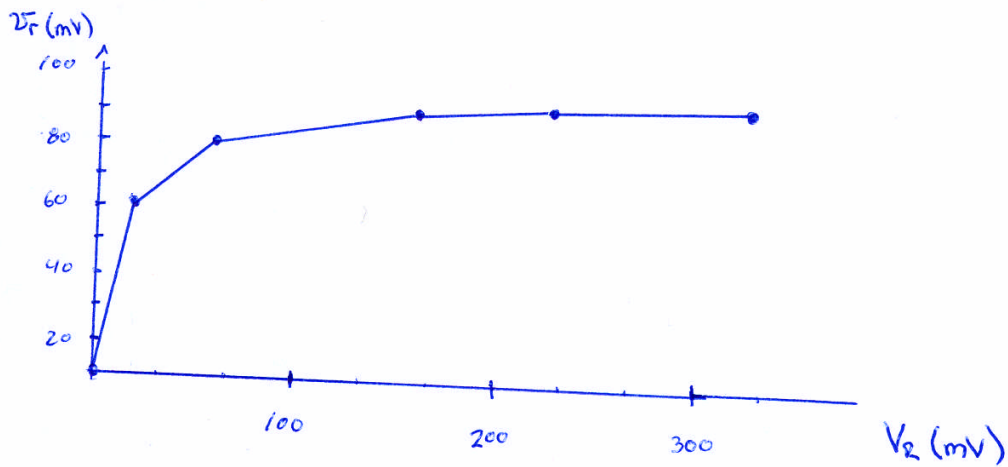
$V_R$ (v)	$v_F$ (v)
0.1	0.079
0.2	0.088
0.3	0.092
0.4	0.093
0.5	0.095



(E)

$V_{IN} (mV)$	$V_R (mV)$	$V_{r, peak} (mV)$
331.6	5.698	3.545
527.2	25.04	63.49
602.0	67.58	83.52
722.5	164.3	91.2
799.2	231.6	94.8
916.7	338.6	96.1

(F)



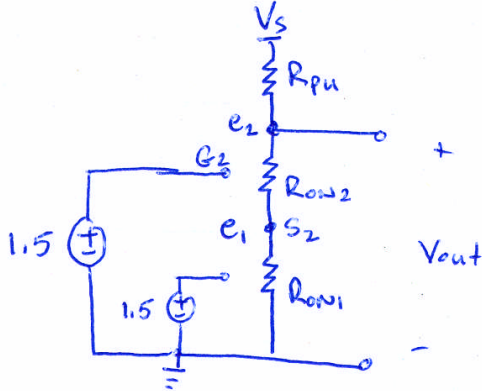
The two graphs have the same trend. As the bias current increases, the diode is able to pass enough current so that the resistor can see the full small signal oscillation.  $V_r$  will never reach 100mV because there is always a finite voltage drop across the diode.

# Problem 3.2

(8)

(A)  $V_{IN1} = V_{IN2} = 1.5V$        $V_T = 1V$

Assume: M1 on, M2 on



$R_{PU} = R_{OU2} = R_{OU1}$

Voltage Divider:

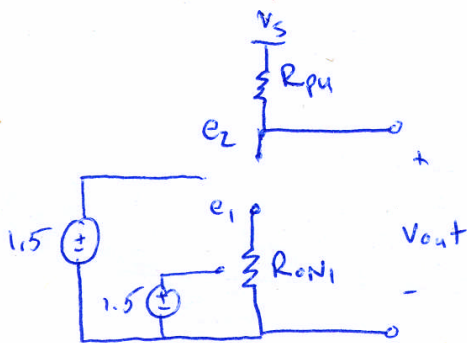
$e_2 = 2V$

$e_1 = 1V$

$V_{GS2} = 1.5 - e_1 = 1.5V - 1V = 0.5V$

$V_{GS2} < V_T$       Inconsistent

(B)



M1 ON, M2 OFF

Open Circuit:

$e_1 = 0V$

$e_2 = 3V$

$V_{GS2} = 1.5V - e_1 = 1.5V$

$V_{GS2} > V_T$       Inconsistent



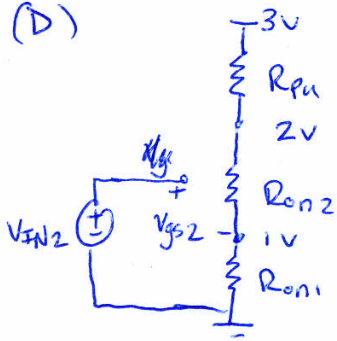
9

(C) The SR model is only reliable when

$$V_{DS} \ll V_{GS} - V_T$$

For  $V_{GS}$  very close to  $V_T$ , the on-state resistance ( $R_{on}$ ) of the MOSFET is much lower. The SR model with two extreme states is not an accurate physical model of the device for all inputs. This inconsistency is apparent in the NAND gate because the control voltage of  $M_2$ ,  $V_{GS2}$ , depends on the state of the MOSFET. The source of  $M_2$  is floating so here the inconsistency affects circuit behavior

(D)



$V_{in2}$  must be set so that:

$$V_{GS2} > V_T$$

$$V_{GS2} = V_{in2} - V_{S2} = V_{in2} - 1V > 1V$$

$$\Rightarrow V_{in2} > 2V$$

$$\boxed{V_{IH} = 2V}$$

(E) No, the SR model will not cause an inconsistency in the NOR gate. All of the MOSFET sources are tied to ground, so all control signals are referenced to ground.

Problem 3.3

(A) For the power through the gate to be minimized, we want a small voltage drop from drain to source. This ~~can~~ can be achieved by having a large drop through  $R_{pu1}$  &  $R_{pu2}$ .

ie  $R_{pu1} = R_{pu2} = 10^5 \Omega$

$R_{on3}$

When M3 is on, we need  $V_{OL} = 1V$ .

Therefore:

$$V_{OL} = \frac{R_{on3}}{R_{on3} + R_{pu2}} \cdot V_s = \frac{R_{on3}}{R_{on3} + 10^5} \cdot 5V = 1V$$

$$R_{on3} = 2.5 \times 10^4 \Omega$$

$R_{on1}, R_{on2}$

To minimize power dissipation we ~~maximize~~ <sup>maximize</sup>  $R_{on1}$  &  $R_{on2}$ :

$$R_{on1} = R_{on2} = 10^5 \Omega$$

$V_{T1}, V_{T2}$

Both M1 & M2 must obey the static discipline and turn on when their  $v_{gs}$  is higher than  $V_{IL}$  and lower than  $V_{IH}$ .

$$2V \leq V_{T1}, V_{T2} < 3V$$

(10)

 $V_{T3}$ 

The highest input voltage for M3 for which it should be OFF is when one of M1 or M2 is ON.

$$V_{in3} = \frac{R_{on1}}{R_{on1} + R_{off1}} \cdot 5V = \frac{2.5 \times 10^4}{2.5 \times 10^4 + 10^5} \cdot 5V = 1V$$

$$\therefore \boxed{1V < V_T < 5V}$$

(B) There are 4 logic combinations:

1)  $V_{IN1}$  Low,  $V_{IN2}$  Low

$$P_{M1} = P_{M2} = P_{R1} = 0$$

$$P = \frac{V_s^2}{R_{puz} + R_{on3}} = \frac{(5V)^2}{20k\Omega} = 1.25 \times 10^{-3} W$$

2,3)  $V_{IN1}$  Low,  $V_{IN2}$  High or  $V_{IN1}$  High,  $V_{IN2}$  Low.

$$P_{R2} = P_{M3} = 0$$

$$P = \frac{V_s^2}{R_{pui} + R_{on1}} = \frac{(5V)^2}{20k\Omega} = 1.25 \times 10^{-3} W$$

4)  $V_{IN1}$  ON,  $V_{IN2}$  ON

$$P_{R2} = P_{M3} = 0$$

$$P = \frac{V_s^2}{R_{pui} + R_{on1} \parallel R_{on2}} = \frac{(5V)^2}{10k + 5k} = \frac{25}{15k} = 1.66 \text{ mW}$$

IF all logic combinations are equal:

$$P_{ave} = \frac{3(1.25 \text{ mW}) + 1.66 \text{ mW}}{4}$$

$P_{ave} = 1.35 \text{ mW}$

Problem 3.4

(A) See attached plots

(B) See attached plots

(C)  $V_T$  can be determined from the plot of the transfer characteristic from part (B). It is the point at which the MOSFET starts passing current.

$$V_T \sim 1.8 \text{ V}$$

(D) For the MOSFET to behave as a switch,  $V_{DS}$  should be chosen so the device is in saturation (the flat portion of the output characteristic curve).

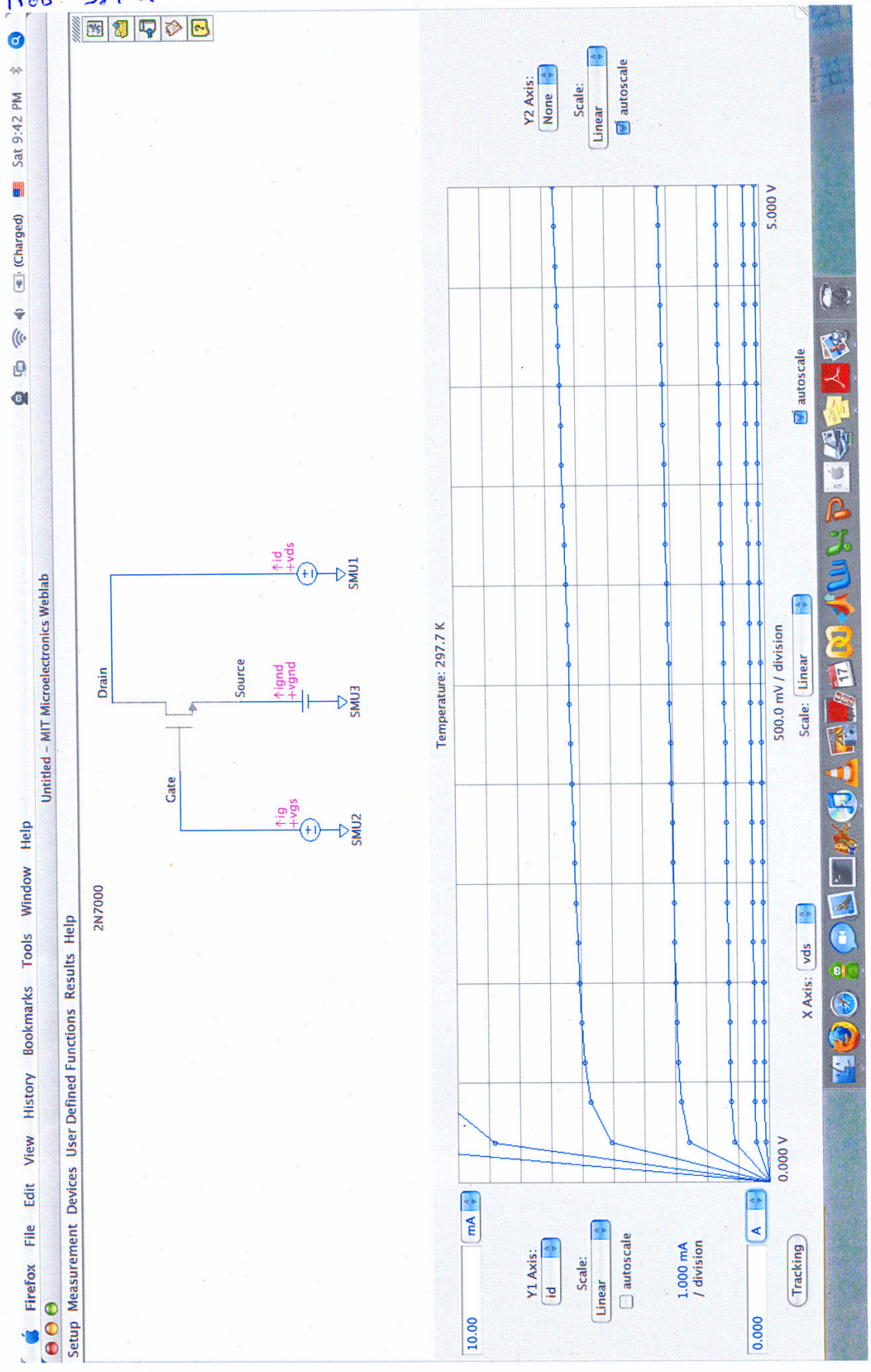
$$\therefore V_{DS} > 0.5 \text{ V}$$

$V_{GS}$  must be chosen so that the device is either fully on or off. For the on part of the switch,

$$V_{GS} > 2.1 \text{ V}$$

Prob 3.4 a

14



Prob 3.4 b

15

