Device Characterization Project

PART II: MOSFET CHARACTERIZATION - OCTOBER 13, 2000

Due: various dates at lecture (see below)

This is a continuation of the new device characterization project of 6.720J/3.43J. In this second part, the detailed characterization of an integrated MOSFET is carried out. The device is available in the MIT Microelectronics WebLab.

Part II: MOSFET characterization *(50 points)*

The MOSFET is connected as shown in the schematic on line (use any of the devices labeled "6.720 NMOS"). Take the measurements specified below. Once satisfied with the look of the data displayed through the web, you should download the data set for graphing and further analysis using your preferred software tool (typically MATLAB or EXCEL).

For all the following measurements, hold V_{GS} between 0 and 2.5 V and V_{DS} between 0 and 4 V. Unless specified, the back bias should be $V_{BS} = 0\ V$. When relevant, examine V_{BS} between 0 and $-2.5\ V$. Refer to Appendix B at end of this document for basic information about the MOSFET.

Here is your assignment:

II-1) *(5 points)* Measure and download the *output characteristics*, that is, I_D vs. V_{DS} with V_{GS} as parameter. In your local machine graph the output characteristics (**graph 1**, linear scales).

II-2) *(5 points)* Program the HP4155 to calculate the *output conductance* $g_d = \frac{\partial I_D}{\partial V_{DS}}$. Download g_d. Graph g_d vs. V_{DS} with V_{GS} as parameter (**graph 2**, linear scales). This measurement is best done in conjunction with II-1.

II-3) *(5 points)* Measure and download the *transfer characteristics*, that is I_D vs. V_{GS} with V_{DS} as parameter. In your local machine, graph the transfer characteristics (**graph 3**, linear scales).

II-4) *(5 points)* Program and download the *transconductance* $g_m = \frac{\partial I_D}{\partial V_{GS}}$. Graph g_m vs. V_{GS} with V_{DS} as parameter (**graph 4**, linear scales). This measurement is best done in conjunction with II-3.

II-5) *(5 points)* Measure and download the *backgate characteristics in saturation regime*, that is, I_D vs. V_{GS} with V_{BS} as parameter for $V_{DS} = 4\ V$. Step V_{BS} between 0 and $-2\ V$. Graph the characteristics (**graph 5**, linear scales).

II-6) *(5 points)* Measure and download the *subthreshold characteristics*, that is I_D vs. V_{GS} for $V_{DS} = 2\ V$. Graph I_D vs. V_{GS} (**graph 6**, log-linear scales).

II-7) *(5 points)* From the $V_{BS} = 0$ output and transfer characteristics and using the models described in Appendix B, extract $\mu_e C_{ox}$ and the threshold voltage, V_{th}. Graph together the experimental and the modeled output characteristics (**graph 7**, linear scales).

II-8) *(5 points)* From the $V_{BS} = 0$ output conductance data and using the models described in Appendix B, extract λ. Graph together the experimental and the modeled output conductance as a function of V_{DS} with V_{GS} as parameter (**graph 8**, linear scales).

II-9) *(5 points)* From the backgate characteristics, extract the treshold voltage as a function of V_{BS}. Extract the values of V_{tho}, γ and ϕ_{sth} (hint: try values for ϕ_{sth} in the $0.6-1\ V$ range). Graph together the experimental and modeled dependence of V_{th} vs. V_{BS} (**graph 9**, linear scales).

II-10) *(5 points)* From the transfer characteristics and using the models described in Appendix B, extract I_{off}, the ideality factor n, and compute the subthreshold slope S. Graph together the experimental and the modeled subthreshold characteristics **graph 10**, log-linear scales).

As inputs to this exercise, you need the dimensions of the gate of the MOSFET: $L = 1.5\ \mu m$, $W = 46.5\ \mu m$. The temperature of the room where the device is located is $T = 23^oC$.

Deadlines:

- Parts II-1 through II-6: due October 20 with homework (you should keep a copy for yourself);
- Parts II-7 through II-10: due October 27 with homework.

Additional information and assorted advice:

- This project might take a substantial amount of time. You must start early.

- This project is taking place simultaneously to another one on the same system in 6.012. Hence there will be a lot of traffic on the system, particularly since both asignments have the same Friday 10/20 deadline. Also, make sure you use the devices that are labeled ”6.720 NMOS”.

- The graphs need not be too fancy, just simply correct. They must have proper tickmarks, axis labeling and correct units. If there are several lines, each one should be properly identified (handwriting is OK).

- If you encounter problems with the WebLab, please e-mail the TA, Jorg Scholvin (), the instructor, Prof. del Alamo (alamo@mit.edu) or the system manager, Jim Hardison (hardison@mit.edu).

- You have to exercise care with this device. Please do not apply a higher voltage than suggested. The MOSFET is real and it can be damaged. If the characteristics look funny, let us know.

- It will be to your advantage to make good use of the *Set-up* and *User-defined* functions that are built into the tool (see manual).

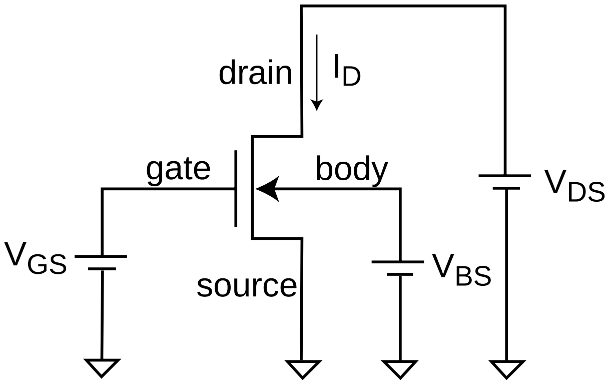
- The system keeps a record of all logins and all scripts that each user executes.

Note on collaboration policy

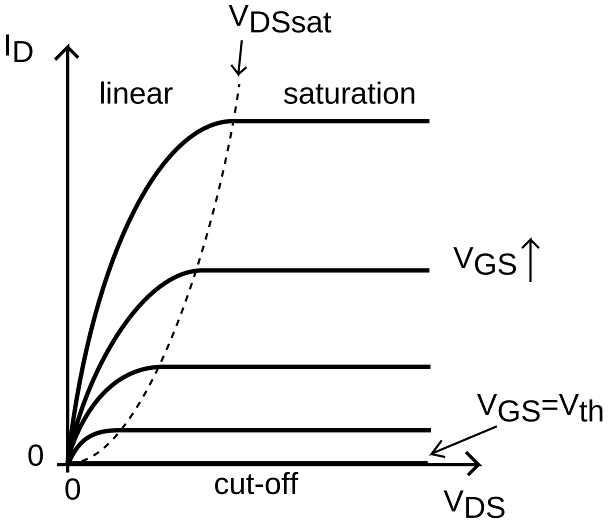
In carrying out this exercise (as in all exercises in this class), you may collaborate with somebody else that is taking the subject. In fact, collaboration is encouraged. However, this is not a group project to be divided among several participants. Every individual must have carried out the entire exercise, that means, using the web tool, graphing the data off line, and extracting suitable parameters. Everyone of these items contains a substantial educational experience that every individual must be exposed to. If you have questions regarding this policy, please ask the instructor. Prominently shown in your solutions should be the name of the person(s) you have collaborated with in this exercise.

Appendix B: MOSFET I-V characteristics

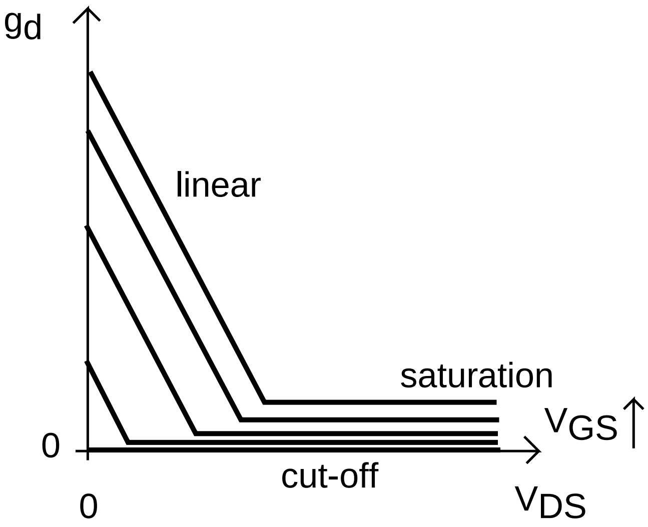
The MOSFET terminal naming convention, voltage and current notation are shown below:



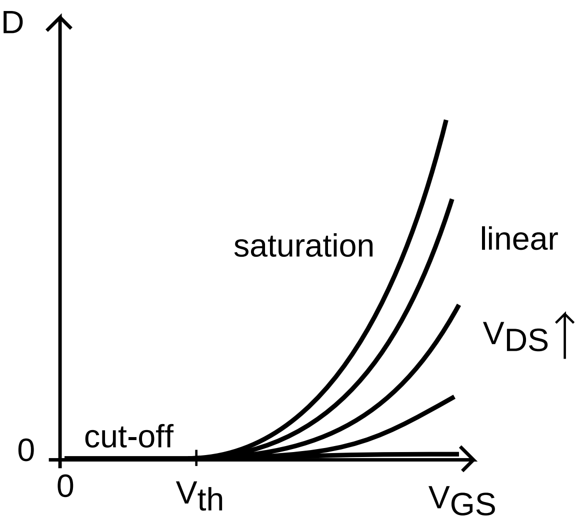
The *output characteristics* of the MOSFET refer to a graph that shows the drain current, I_D, *vs.* the drain-source voltage, V_{DS}, with the gate-source voltage V_{GS} as parameter:



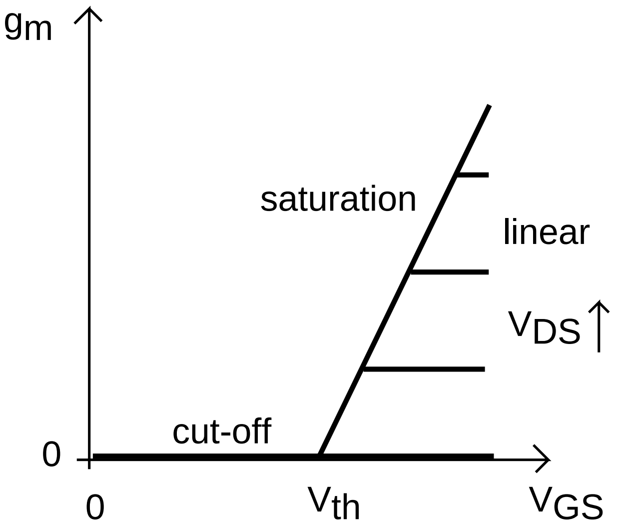
The slope of the drain current with V_{DS} is the *output conductance* g_d, which graphed as a function of V_{DS} looks like:



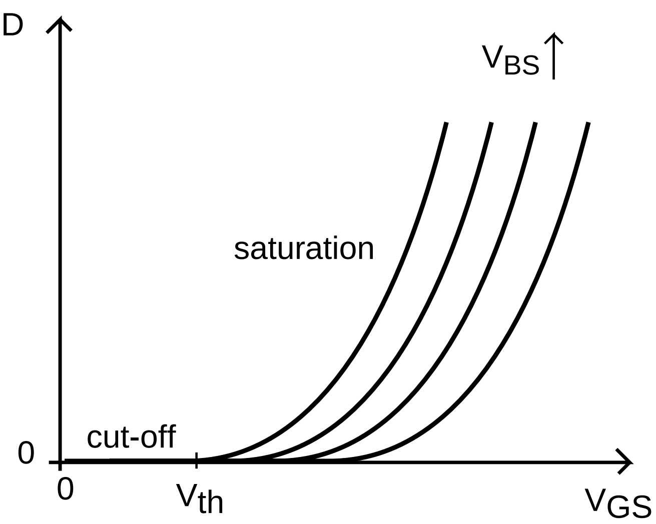
The *transfer characteristics* refer to a graph of I_D vs. V_{GS} with V_{DS} as parameter.



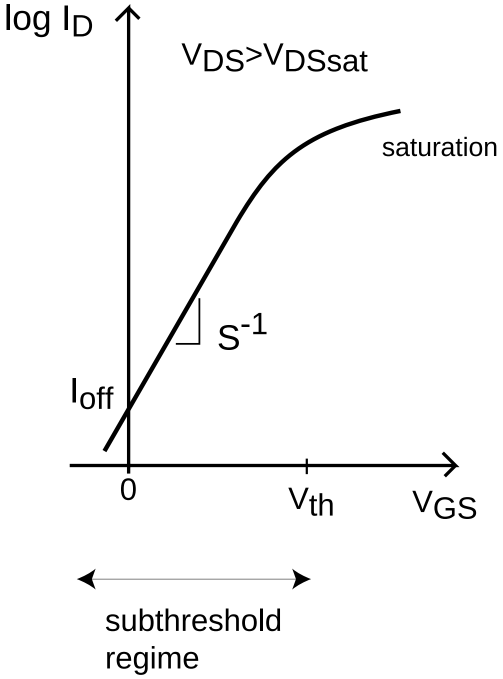
The slope of the drain current with V_{GS} is called the *transconductance* g_m, which graphed as a function of V_{GS} looks like:



The *backgate characteristics* show the drain current in saturation as a function of V_{GS} for several values of V_{BS}:



The *subthreshold characteristics* show I_D vs. V_{GS} in a semilog scale:



From these experimental characteristics, one can extract important parameters of a MOSFET. For this exercise, use the long-channel description of the I-V characteristics of a MOSFET:

- *Linear regime*, $V_{GS} > V_{th},\ V_{DS} < V_{DSsat}$:

$$I_D = \mu_e C_{ox} \frac{W}{L} (V_{GS} - \frac{V_{DS}}{2} - V_{th}) V_{DS}$$

- *Saturation regime*, $V_{GS} > V_{th},\ V_{DS} > V_{DSsat}$:

$$I_D = \mu_e C_{ox} \frac{W}{2L} (V_{GS} - V_{th})^2 [1 + \lambda (V_{DS} - V_{DSsat})]$$

  where, V_{DSsat} is the drain-source voltage that saturates the transistor. In the simplest long-channel model:

$$V_{DSsat} = V_{GS} - V_{th}$$

- Effect of *back bias*:

$$V_{th} = V_{tho} + \gamma(\sqrt{\phi_{sth} - V_{BS}} - \sqrt{\phi_{sth}})$$

- *Subthreshold regime*, $V_{DS} > V_{DSsat}$:

  $$I_D = I_{off} \exp \frac{qV_{GS}}{nkT}$$

  The *subthreshold slope* is defined as:

  $$S = n\frac{kT}{q} \ln 10$$

  and it has units of mV/dec ("millivolts per decade").