Game Theoretic Models of Inter-firm R&D Dynamics in Semiconductor Manufacturing

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SUBMITTED TO THE ENGINEERING SYSTEMS DIVISION IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF

DOCTOR OF PHILOSOPHY IN ENGINEERING SYSTEMS AT THE MASSACHUSETTS INSTITUTE OF TECHNOLOGY

June 2013

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“Essentially, all models are wrong, but some are useful.”

– *George Box*

“Innovation is often a synthesis of art and science, and the best innovators often combine the two.”

– *Thomas Friedman*

“For a well-schooled man is one who searches for that degree of precision in each kind of study which the nature of the subject at hand admits …”

– *Aristotle*

“When I am getting ready to reason with a man I spend one-third of my time thinking about myself and what I am going to say, and two-thirds thinking about him and what he is going to say.”

– *Abraham Lincoln*

“The general who wins the battle makes many calculations in his temple before the battle is fought. The general who loses makes but few calculations beforehand.”

– *Sun Tzu*

Game Theoretic Models of Inter-firm R&D Dynamics in Semiconductor Manufacturing

This dissertation demonstrates that valuable strategic insight and a reasonable measure of predictive power can be obtained by developing and analyzing context-rich parsimonious game theoretic strategy models during large technology transitions in concentrated industries. Such models enable clear and compact analysis of oligopolistic competitive dynamics which are typically addressed by more informal processes in much of current managerial practice.

This result is established by constructing 3-player game theory models of two prominent, ongoing technology transitions in semiconductor manufacturing: EUV lithography (EUVL) and 450mm silicon wafers. The iterative multi-data-source process used for establishing appropriate game structures and payoff estimates is described in detail. Contextual realism was augmented by in-depth behavioral analysis of select industry players and by interactions with the equipment supplier facing groups at a semiconductor device manufacturer.

The robust game theoretic prediction from the EUV lithography R&D model was subsequently validated by the announcement of a series of chipmaker investments totaling greater than $6B in the largest photolithography supplier in July/August 2012 (including significant financial assistance to EUV equipment readiness) and by several other industry financing events in late 2012. Although no such distinct confirmatory evidence exists for the 450mm wafer model predictions, it was found to have substantial face validity.

Based on learning from the modeling efforts, criteria are proposed for determining whether other technology transitions will be amenable to such analysis. Generalizability to similar transitions in other industries (including aerospace and automotive) is discussed. Industry strategists, technology and business strategy scholars, and innovation policy makers should find the work of interest.

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Acknowledgments

I can't thank enough all of the friends and family who have been such a big part of my amazing and transformative four-year PhD adventure. At times I've been: studious, tired, elated, frustrated, playful, proud, satisfied, and happy. It's been the memories with the people who are close to me which has made this time so very special.

First, I would like to thank my mentor and thesis supervisor, Charlie Fine, for his expert guidance. Charlie had the uncanny ability help me passionately develop my own research approach and ideas within the multidisciplinary and reality-grounded spirit of ESD, while every once-in-a-while intervening with a critical nudge when I seemed to be wandering a little too far astray! Each of my other committee members (Itai Ashlagi, Don Rosenfield, Richard de Neufville, and [unofficially] Richard Roth) also adroitly played important roles in the process by: being thoughtful sounding boards for my ideas, suggesting ways to refine and extend my work, keeping the research process moving forward, and helping me keep everything in perspective.

In addition to excellent counsel from my dissertation committee, I also want to thanks a number of other faculty and staff for their kind support of my intellectual development throughout the ESD program: Bruce Arntzen, Jarrod Goentzel, Chris Magee, Beth Milnes, Jim Rice, Joe Sussman, and Jim Utterback.

I'd also like to thank my friends and colleagues within the semiconductor industry who provided crucial feedback on this research. (All judgments, opinions, and errors in this dissertation, of course, remain solely my own.) You are unsung heroes -- both in being the steady guiding hands underlying the amazing, transformative technology which you help bring into the world every day and in providing me invaluable help with my research. I wish I could call you out by name, but you know who you are.

Specifically, regarding editorial suggestions and idea sharpening for this dissertation, I also want to single out Lily Kim, Shardul Phadnis, David Ramberg, Vivek Sakhrani, and Nils Wernerfelt as particularly helpful in this regard.

For reasons of brevity (and to avoid the inevitable embarrassment of missing someone!), I will send a shout out to big cadres of friends from my time at MIT: my ESD and Sloan PhD classmates, the ESD.83 students from Fall 2010, the LGO and Sloan MBA classes of 2005, and the SCM class of 2013. In addition to those joyous and amazing folks, I also want to say thank you to my other personal friends who shared in this adventure: Cody, Desiree, Gavin, Haitham, Jen (Larese), Joe (Duarte), Joost, and the regulars at the Muddy Charles pub.

Last but certainly not least, I want to acknowledge the deep love and tireless support that my girlfriend Lily, mother Marilyn, brother Jim, and extended family have given me along this journey. I can never express fully the gratitude and love I feel for them.

I apologize to any folks who I have omitted; let's grab a beer and laugh it off together!

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Chapter 1: Motivation -- Strategic R&D Coopetition in Highly Concentrated Industries

1.1 Research Motivation and Strategic Contexts of Interest

This dissertation addresses the strategic interactions among firms making large, partially coordinated technology bets in the context of highly concentrated and technologically-interlinked value chains. By highly concentrated, I mean that there should be generally three or fewer critical players in each important market segment across one or two tiers of the value chain. By technologically interlinked value chains, I mean that the products or services being produced are complicated enough to involve multiple complex subcomponents and production processes, leading to a value chain with R&D-intensive suppliers which are critical to overall production. I believe this work provides evidence that useful applied quantitative strategic models (i.e., industrially realistic parsimonious non-cooperative game theoretic models) can generate insights that are not currently being developed and utilized in practice.

Thus, the overarching research question guiding this dissertation is:

How can firms make better strategic R&D financing decisions during large, tightly-coupled technology transitions in highly concentrated value chains?

Below, I give an expanded description of situations where this type of modeling may be relevant and three concrete examples of such situations.

1.1.1 Expanded Description of Strategic Contexts of Interest

By their very nature, technology transitions in concentrated value chains tend to arise in industries in a relatively mature phase of their life cycle. In such mature and concentrated industries there is usually (reasonable) certainty regarding who the players are and which strategic actions are available to them, allowing accurate estimation of how much each key player stands to benefit or lose from their strategically intertwined choices.

Further, I want to focus on those situations where detailed quantitative modeling will provide the most useful strategic insight on the technology decisions under consideration (primarily from the point of view of the firms themselves). That is, I wish to study situations that are simple enough to be modeled with reasonable fidelity, yet complex enough that the strategic outcomes are not obvious. Hence, I am less interested in situations where oligopolistic firms are direct competitors to one another in a well-defined market or in situations where customers' and suppliers' interests are extremely well-aligned. In such clear-cut situations, one can perform quantitative strategic modeling, but the strategic results often turn out to be obvious – a small amount of work for a small amount of reward.

The strategic value chain interactions I am interested in here typically have significant elements of both competition and cooperation (e.g., so-called "coopetition") since it is in such situations that quantitative strategic modeling can provide the greatest strategic insight. Much real-world oligopolistic industrial interaction resides in this category (Brandenburger and Nalebuff, 1996).

Coopetition is built into strategic situations addressing customer-supplier relationships (e.g., a customer relies on its suppliers, but the customer and supplier often strategically conflict in areas such as unit prices and the split of R&D expenditure required for industry-wide transitions).

Coopetition is also in-built into horizontal supply relationships in the contexts of oligopolistic competition (e.g., Tirole, 1988; Shy 1995). It is in such strategically interlinked situations that fresh quantitative modeling frameworks are apt to provide the deepest new strategic insights to participating firms.

Particularly large and difficult technology transitions (e.g., the introduction of an entirely new category of commercial aircraft or of the first hybrid-electric automobiles) are studied here, primarily because they contain high-impact financial decisions that can withstand the significant "signal-to-noise" confounding that would plague decisions of lesser importance. For example, large firms in concentrated/mature industries tend to repeatedly interact with each other across an array of issues (e.g., pricing policies for current products, decisions regarding market entry into adjacent markets, relationship-building with common suppliers, intellectual property stances and strategies, lobbying efforts toward governments, etc.). However, in highly research-intensive industries, infrequent technology transitions can transform the entire production system, and economic costs and benefits of the transition itself are typically large enough to be decisive in each player's decision-making processes.

Further, when very large technology transitions are considered, the decisions of the firms can often be categorized with reasonable fidelity into a few discrete choices (e.g., 'Invest in the new technology' or 'Don't invest in the new technology'). This tendency also makes parsimonious game theoretic model building more tractable in such situations.

To recapitulate, the research motivation for this dissertation is to better understand those situations where only a few key strategic players exist and where the industry at large is focusing on large R&D-intensive, cross-firm technology transition projects. Such situations constitute a

fertile domain for study because they have the potential to yield useful and non-obvious insights (because they are strategically vital, yet messy situations) and are reasonably amenable to quantitative strategic modeling (because the key players and their potential actions are well-delineated and well-understood).

Because of the strategic complexity inherent in these technology transitions, it is crucial to infuse a high level of industry and institutional context and detail into any such modeling effort. This implies that the industrial situations to be studied (and corresponding research approaches) that I am proposing are in the spirit of the Alfred P. Sloan Foundation's Industry Studies Program (recently completed) and its descendent, the Industry Studies Association (ISA). A healthy amount of "go to the gemba" industry immersion is probably a necessary condition for the development of strategically relevant models of this type. Relatedly, the type of research methodology required to build effective models is quite ecumenical in its employment of data sources. In Chapter 2, the mixed-data source game theoretic methodology developed and used (in the vein of Yin 2009) will be spelled out more completely. Given the large financial stakes involved, any additional insight gleaned from these "high touch", cost-intensive research methods is likely to be worth the expense.

It has been cogently argued that the situations described above will become more frequent over time in the evolving high-technology, capital-intensive, and winner-take-all global economy (Lange et al. 2013, Hobday 1998). If true, then it will be more important than ever to have the best decision science tools possible to facilitate decision-making for these complex industry transitions. For instance, the models developed here may help in reducing the "in-fighting" and extended negotiation delay costs that can erode the benefits of such large technological innovations (Hutcheson 2006). Finally, added motivation can easily be found in the difficult

struggles that national economies and governments are experiencing in their post-Great Recession approaches to maximizing innovation, wealth creation, and high-quality jobs in the ever-evolving global economy.

1.2 Three Examples of Relevant Strategic Industrial Situations

Given the research motivation above, I now provide three concrete examples of industrial situations from the aerospace, automobile, and semiconductor industries which approximately fit the criteria for relevant strategic situations outlined above. These are merely meant as representative overview examples which concretize the objects of research interest for this dissertation; it is not a comprehensive list and does not contain exhaustive treatments of the examples given.

Example A: New engine and new aircraft development in the commercial aerospace industry

Concentration in commercial airplane manufacturing has been high for quite a while. Since 1980 there have been three or fewer significant airframe manufacturers in the single-aisle 150-seat to 185-seat market. Additionally, since 2000 this segment of the market has been dominated by a relatively evenly matched duopoly between Boeing and Airbus (Morrison et al 2012). This concentration has led several scholars to use game theory in empirical pricing models or environmental policy testing models for the aerospace industry (e.g., see Irwin and Pavcnik 2004; Morrison et al. 2012). Although there is also high concentration at the commercial jet engine manufacturer level of the value chain (Newhouse 2007, Chapter 5), the few game theoretic modeling efforts to date have been focused solely on the competition among the airframe manufacturers.

In addition to oligopolistic competitive forces among the airframe and engine manufacturers, government involvement is omnipresent from the standpoints of job creation and economic growth (Newhouse 2007), fairness of international trade (Newhouse 2007; Krugman 1987), national defense and security (Newhouse 2007), and environmental policy (Morrison et al. 2007). Thus any attempt to model strategic interaction in this industry will likely involve modeling (or at least carefully accounting for) the political incentives of one or more of the key governments involved. Finally, the market for single-aisle commercial aircraft may become considerably less oligopolistic in the near future as Embraer (Brazil), Bombardier (Canada), COMAC (China), and United Aircraft Corporation (Russia) are all readying new relevant offerings (Morrison et al. 2012). Although the increase in the number of firms (and governments) may muddy the waters for well-formulated and parsimonious quantitative strategic models which identify each firm specifically as a strategic player, Morrison et al. (2012) were able to circumvent this to some extent by assuming the existence of a generalized "new entrant". Despite these new entrants for single-aisle aircraft, the large commercial aircraft segment (e.g., dual-aisle) appears likely to remain duopolistic for the foreseeable future. Therefore, the large commercial aircraft industry is a good candidate for the type of game theoretic modeling advocated here.

Example B: The auto industry's bet on hybrid-electric vehicles

A second industry technology transition that appears to fit the description above is that of the development and volume introduction of hybrid automobiles. In terms of total sales, Toyota overtook the top spot from GM in 2008, due in part to the success of the hybrid-electric Prius and the halo benefits it provided Toyota (MySanAntonio, 1/14/13).

In the early and mid-1990s and there was significant demand uncertainty regarding the classes of vehicles which would thrive in the future. This demand uncertainty was driven by uncertainty in oil prices, governmental regulations (e.g., CAFE standards), and consumer preferences (overall cost, size, performance, environmental preferences, etc.). Given these uncertain factors, one key strategic question facing automobile makers in this time frame was whether and when to make an R&D push to develop "alternative powertrain" vehicles, where electric, hybrid-electric, and fuel cell technologies were all under consideration (e.g., see Metcalf 2001). Although there were a handful of large, global car companies that could consider major investments in alternative powertrains, the decision of whether to be an early adopter of hybrid electric vehicles was complicated by the long payback duration, the amount of capital required, supply chain coordination needed, and significant technology risks. One clear example of a required competence which all car makers lacked was expertise in large lithium ion battery manufacturing.

In this industrial context, one could argue that only the largest automobile manufacturers, e.g. GM and Toyota, had the resources and the incentive to be first to market in this category. This technology transition would thus seem to have been appropriate as another example for framing a quantitative game theory analysis of the sort I am advocating. This analysis would have required a detailed automobile industry knowledge (of both demand and supply), but it could have shed light on the strategic dynamics of the two firms as they made their investment plans. The actual outcome of this situation is now well known, with Toyota pushing forward early with the development of the Prius and gaining significant market share and customer mind-share as a result. Although we are beyond the days when the "big three" automakers were the only three manufacturers selling in high volumes into the American automobile market (and where

interesting empirical studies [e.g., Bresnahan 1987] have been done based on historical data assuming oligopolistic competition among the big three), the example of early hybrid vehicle development could plausibly be another instance in which economic and technological conditions aligned to allow for a game-theoretic analysis of high-stakes technology investment in a concentrated industry.

Example C: Technology transitions in the semiconductor industry (e.g., new photolithography equipment and larger wafer sizes)

The third and final example of a strategic situation which matches the characteristics highlighted above relates to two technology transitions in the semiconductor manufacturing industry: development of extreme ultraviolet (referred to in the industry interchangeably as EUV or EUVL) photolithography and the transition to 450mm diameter silicon wafers.

Although prior photolithography and wafer-size transitions in the semiconductor industry have entailed close coordination across the supply chain, many of these transitions have been driven by consortia of relatively large numbers of firms (e.g., see Browning and Shetler, 2000). One such prominent example has been the successful use of Sematech, an industry consortium of U.S. chip manufacturers founded in the late 1980s, to coordinate "pre-competitive" R&D for semiconductor fabrication technology across firms who were otherwise competitors (e.g., see Browning and Shetler 2000; Browning et al. 1995; Corey 1997; Link et al. 1996). This has been a well-studied case, and other industries have examined Sematech as a possible model to aid their own coordination issues (e.g., Corey 1997).

Although the semiconductor industry continued to use this consortium approach to great effect into the early 2000s, this broad-based consortium has evolved recently and rapidly to an acute

small-numbers game as the industry consolidates due to steeply rising investment levels required to continue to play. One industry consortium executive, Tom Morrow, giving voice to this concern, stated recently that: "At no time have industry executives faced more strategic uncertainty or greater doubt about the future effectiveness of past competitive and collaboration models." (Morrow, 2/9/12).

Driving this strategic inflection point are the twin industry trends of the increasing costs of R&D projects relative to size of industry (see Hutcheson 2006 and Hutcheson 2013) and the dramatic and ongoing recent consolidation at both the chipmaker and equipment-supplier tiers of the supply chain (see Hutcheson 2013; Jelinek, 2/20/11; Hutcheson 1/12/11). These intertwined trends drive the conclusion that significant sharing of the R&D costs of large technology transitions between the equipment suppliers and their chip-making customers will be necessary (Lapedus, 10/25/10; McGrath, 7/11/12).

The three largest chip manufacturers are now Intel, Samsung, and Taiwan Semiconductor Manufacturing Corporation (TSMC); together they now fabricate approximately one-third of global semiconductor products by revenue and currently purchase fully half of semiconductor fabrication equipment in the industry (Notebookcheck 3/28/13; Solid State Technology 1/23/12). Additionally, there are only two cutting-edge suppliers in photolithography (ASML and Nikon) with the substantial resources and knowledge needed to develop EUV photolithography. These few remaining companies are now in a strategic coopetitive dance to determine who will provide the substantial resources needed to develop EUV Lithography and 450mm wafer processing technology (both of which will affect significantly the economic interests of the industry players). This industry context makes these two technology transitions amenable to the quantitative strategic analysis which is the focus of this dissertation.

1.3 Chapter Summary

The examples above suggest that there are multiple technology transitions across multiple industries that approximately fit the suitability criteria outlined at the beginning of this chapter. These examples are not meant to be exhaustive, but to provide evidence of the breadth of technological and industrial situations that are potentially amenable to analysis of the type provided in this dissertation. I will demonstrate through the course of the dissertation that deeply-contextualized quantitative game theoretic analyses are in fact a fruitful lens with which to study the class of strategic interaction defined here in Chapter 1.

The bulk of the dissertation (Chapters 3 through 6, plus Appendices A and B) will focus squarely on the two technology transitions in semiconductor manufacturing mentioned above (i.e., Example C). I will again revisit the boundaries of usefulness for such detailed, yet applied, context-intensive game theoretic models in the concluding chapter (Chapter 7), which proposes a set of industry and technology criteria for determining when this type of analysis is most fruitful.

Chapter 2: General Methodological Approach

"My conviction is simply that deductive models can, ideally, express hypotheses in a language that is more amenable to progressive debate than is the language of checklists."

-Colin Camerer
(from Camerer, 1985)

2.1 Tension between Game Theory and Strategic Managerial Practice

Strategy scholars are divided over the usefulness of applied game theory to corporate strategy practice. Major proponents of its usefulness include: Brandenburger and Nalebuff (1996), McMillan (1992), Kelly (2003), Camerer (1991, 1985), and Papayoanou (2010). If game theory is directly useful for strategy-making in any industrial situation, it is most likely to be useful in highly concentrated industries where the relevant players and their potential actions are relatively well defined. Even if one is skeptical of the efficacy of this overall approach, one should still desire to understand clearly why certain strategic lenses are *not* applicable or are applicable only in delimited situations (e.g., see Adner and Levinthal 2004 for this sort of delineation regarding the appropriate use conditions for real options analysis). Finally, as with any applied modeling effort, significant robustness checks and sensitivity analyses of the model framework assumptions and payoff calculations are crucial.

Even if one agrees that quantitative game theory should be brought to bear on corporate strategy, it is widely agreed by proponents and detractors alike that there is a significant gap between the deep theory developed by mathematicians and economists for game theory and its practical applicability to everyday business situations (e.g., Brandenburger and Nalebuff 1996; Camerer 1991, etc.). There are several reasons for this chasm. First, an array of economic and business

theorists (not to mention mathematicians, computer scientists, biologists, etc.) have been expanding and codifying the body of theoretical work in game theory at a dramatic pace (Kreps 1990; Gibbons 1992, Dixit et al. 2009). Second, many game theory practitioners have been focusing the bulk of their application efforts preferentially toward computationally intensive applications (e.g. at data-intensive customer interaction-focused companies like Google, Facebook, eBay, and Amazon. See The Economist 10/19/12, Levy 5/22/09). By contrast, one premise underlying this dissertation is that contextually-rich, computationally simpler applications of game theory in the realm of business strategy should not be overlooked. Third, there is a large application gap within corporations between traditional applied decision analysis methods (e.g., E(NPV)s, decision trees, etc.) and more advanced decision science techniques such as game theory and real options. Referring to the sparing use of game theory within managerial practice, one author (Camerer, 1991) goes so far as to speculate that a generational change in managers and business strategists will be required before game theoretic analysis is more tightly integrated into the practice of strategic decision making within firms.

Figure 1 below (reproduced from Papayoanou, 2010, pp. 13) crystallizes the relationship among three decision science tools (decision analysis, real options, and game theory). In that figure "Influence Issues" refers to interconnectedness of firms' strategic outcomes and "Learning Potential" refers to the ability to use information gained (through the course of time) to modify one's strategic choices *subsequent to one's initial choice(s)*. The diagram illustrates that game theory is appropriate whenever payoffs among key actors are intertwined with one another (whether learning is possible or not).

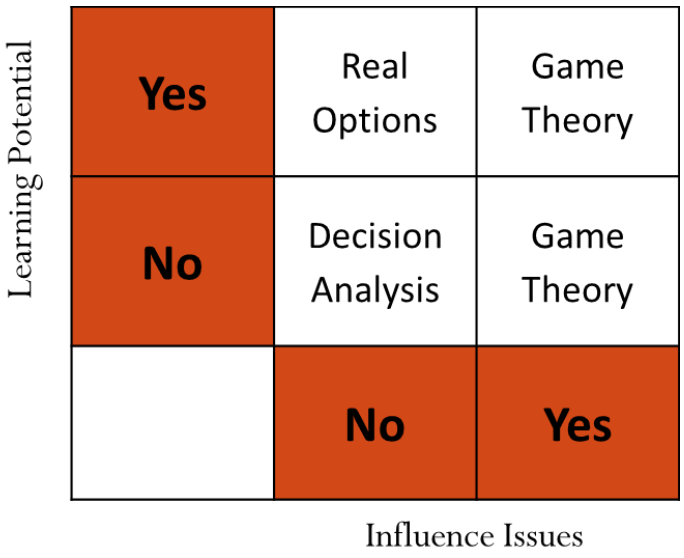


*Figure 1: Classification of Appropriate Decision Science Tools**

*From Papayoanou 2010, pp. 13.

Game theory is not well suited to "one-off" small- or medium-sized decisions because, the economic signal-to-noise ratio in such situations is simply too low. Because the same set of firms tend to interact across multiple domains and across time, a firm's economic self-interest for one small- or medium-sized decision/alliance/payment is likely to be subordinated to larger strategic aims. However, regarding the biggest strategic investments faced by a company, one can more safely assume that economic self-interest will cause those investment choices to play a major role in firm decision-making because there are (by assumption) no larger aims to which to subordinate the strategic decision in question. Also, the assumptions of common knowledge underlying tractable game theoretic models are more likely to be realistic for large industry transitions.

Additionally, there is a lack of clarity for corporate analysts and decision makers regarding how to bridge the extant strategic frameworks being employed (e.g., Porter's five forces, the

innovator's dilemma, intuitive frameworks for leader vs. fast-follower dynamics, etc.) to the rigorous game theoretic framework being advocated in this dissertation. The complex (and sometimes uncomfortable) managerial reality is that no one strategic tool is appropriate for all situations. Wise managers realize this and are open to utilizing a variety of analytical tools depending on the strategic context.

Furthermore, the situations when game theoretic analysis becomes most useful are often not obvious to firms, as industry consolidation frequently progresses gradually as an industry matures. Early in an industry's life cycle, market shares are often fragmented, rendering game theoretic strategic analysis less appropriate and less useful.

2.2 Impediments to Game Theoretic Strategy Modeling

If quantitative game theoretic business strategy analysis were straightforward to implement, it would likely already be widespread in corporate strategy groups and consulting firms (both general management consulting and decision analysis boutiques). However, the application of game theory to strategy is not straightforward for the reasons described above. In addition to those challenges, other practical challenges to implementation include:

- **Data (and strategy) sensitivity and confidentiality.** This is one reason why "best known methods" for strategy-making and implementation are not readily shared among companies and industries
- **A chicken-and-egg "education gap"** regarding game theory which is partially why it is not yet prevalent among consulting companies or internal corporate decision analysis groups. For example, Papayoanou relates the following anecdote: 'One consultant, a highly respected and consummate modeler, told me that it was unnecessary to spend

much time learning how to model options because "we don't sell much options work." "Well, of course," I responded, "when you don't look for options they won't be found." I could have said the same thing about interactive game dynamics.' (Papayoanou, 2010, pp. 59). Such conservatism in thinking as well as "group think" within firms can also be impediments to the successful introduction of such modeling techniques.

- **Funding and employee time commitment constraints** are significant for the in-depth analysis necessary to arrive at contextually realistic game theory models. If any methodology is unproven within an organization, marshaling the resources to thoroughly attempt using it can be challenging.

In general, published academic work describing game theoretic analysis of forward-looking strategic R&D investment decisions has been limited to qualitative or very rudimentary quantitative analyses (one notable exception to this is Morrison et al. 2012). However, as posited in Chapter 1, there is an important subset of strategic situations in which quantitative strategic modeling may be fruitfully employed. As stated in Chapter 1, these situations are characterized by a high degree of market consolidation and a low likelihood of new market entry. Such conditions enhance the ability to make well-justified estimations of each player's payoffs, a necessary step for quantitative strategic modeling.

Recent advances in behavioral and organizational economics attempt to improve the signal-to-noise ratio of microeconomic models. Player payoff refinements based on these advances can be incorporated into the game theoretic models, improving their predictive validity. I will illustrate how such refinements can be incorporated in a relatively straightforward manner into parsimonious game theory (see Chapter 6).

However, the main semiconductor industry models (Chapters 4 and 5) assume rational, individually maximizing decision-making by the players involved. In a number of important business situations traditional, small-number-of-player, non-cooperative game theory models can provide significant strategic insight without the added complications of behavioral and organizational economics.

2.3 Iterative and Parsimonious Modeling Approach

Progressing beyond the roadblocks mentioned earlier, in this dissertation I explore the limits to which the traditional non-cooperative game theory approach can be justifiably extended to explain strategic R&D coopetition in highly concentrated industries. Here we can recall Aristotle's advice: "For a well-schooled man is one who searches for that degree of precision in each kind of study which the nature of the subject at hand admits …" (Aristotle 2011). In this spirit, I have adopted the following perspectives and assumptions to guide and simplify initial model formulation:

- I focus on equilibrium identification, not on mechanisms of equilibrium attainment
- The games are of perfect and complete information
- There are a small number of key players (either individual firms or reasonably well-aligned firms modeled as a single player)
- There are a limited (and small) number of actions possible to each player
- The games are static or "mildly" dynamics (e.g., games consisting of only two stages)
- If necessary and appropriate, an amalgamated subset of firms (only within a single tier of the value chain) can be modeled as a single player in the game
- Prior historical events do not substantially cloud the economic rationality of the players
- The players are risk-neutral

These assumptions can later be relaxed in a controlled manner, given an initial parsimonious modeling framework.

There seems to be a division within the game theory community between the hard-core mathematical theorists and the Thomas Schelling-inspired "pragmatists". Clearly, this dissertation falls squarely into the second camp. Furthermore, many of the scholars pushing this work into business strategy hail from a (broadly speaking) political science orientation (e.g., Schelling, McMillan, Kelly, Papayoanou, etc.).

Although the models presented here (in Chapters 4 through 6) are quite applied from a game theorist's point of view, they are quite theoretical from the point of view of mainstream business strategy (e.g., see Camerer 1985, for a lively discussion of this tension). Indeed, one goal of this dissertation is to help bridge this palpable gap.

Drawing on the existing literature on the practice of managerial modeling (e.g., Little 2004; Brandenburger and Nalebuff 1996), I also adopted the following philosophical modeling principles:

- Provide decision makers with highly transparent and fully parameterized game theory models (including enabling them to "turn the knobs" of the model themselves, if practicable). This helps the users build intuition and fosters acceptance of the models (Little 2004). It also streamlines the process (for the modeler) of performing and communicating robustness checks and sensitivity analysis of model outcomes.
- Deep knowledge of institutional/industry details is crucial to good model development (and adoption). Camerer (1991) stated "… the implication is that focused case studies of firm behavior and industry evolution, which have been largely replaced in strategy by large empirical studies of archival data, might be an excellent source of data if the case researchers are sensitive to game-theoretic variables."

- Use multiple data sources when possible, including interviews to triangulate toward validated game structures and payoff estimates (e.g., see Yin 2009, pp. 114-117). Generally, it advisable to collect and attempt to integrate each relevant data source which is accessible to the modeler.
- Employ an iterative approach to model building as shown in Figure 2 below. This is consistent with the advice of Camerer (1985) and is also done for analogous reasons that multiple project cost estimates are performed iteratively with higher levels of fidelity during project management of very large projects (e.g., see ASPE 2004). An iterative approach aids accurate formulation of game structure, estimation of payoffs, ensures modeling efforts remain focused on the real business challenges of the decision maker, and minimizes wasted effort due to faulty assumptions and imprecise definition of early customer requirements.
- Be vigilant in one's efforts to adopt/maintain an *allocentric* point of view regarding the payoff estimates and strategy selection for each player in the model. Brandenburger and Nalebuff (1996) note that allocentric is defined by Merriam-webster.com as "having one's interest and attention centered on other persons". One may employ academic researchers, strategy consultants, and/or former employees of key firms now resident in one's own organization or who are otherwise available to reality-check modeling assumptions and decision outcomes. These collaborations allow the modeler to step outside oneself (and thus mitigate one's biases about others) to adopt a more fully allocentric stance.

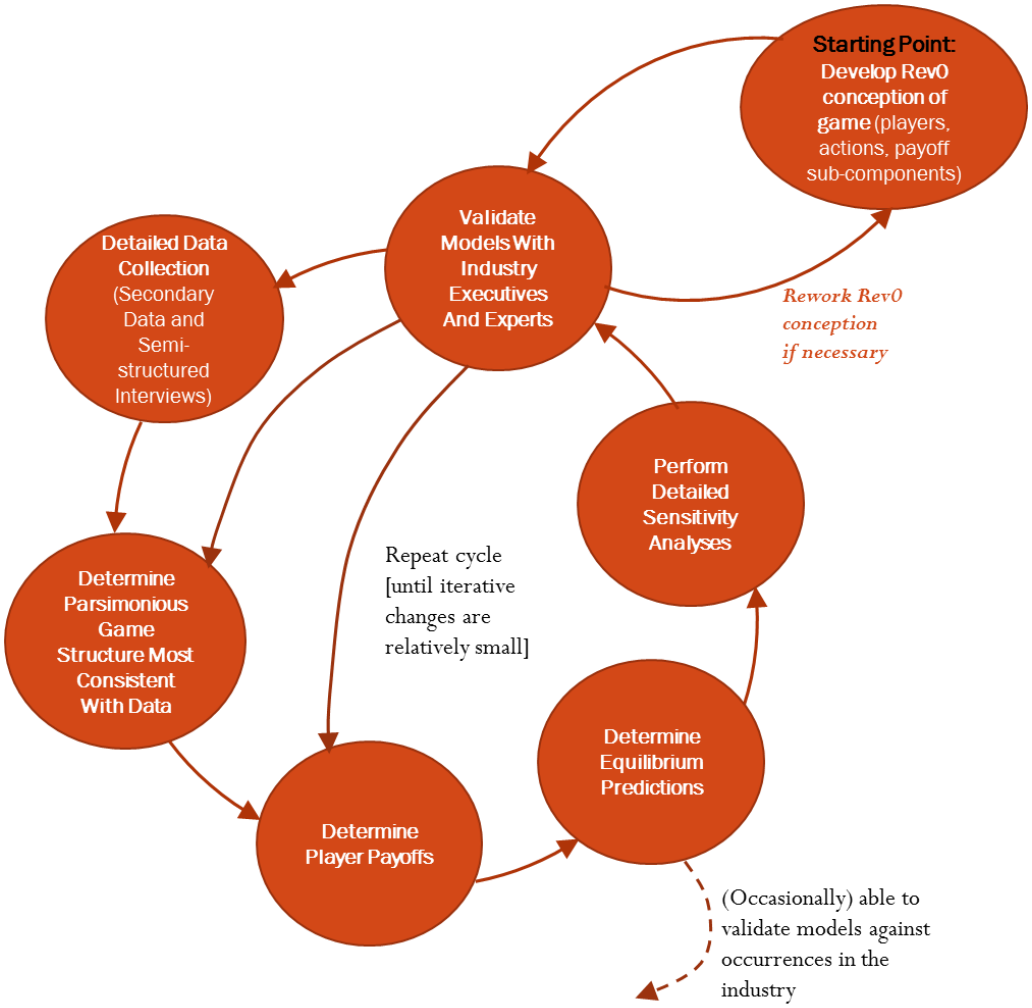


Figure 2: Iterative Methodology for Developing Strategic Game Theory Models

Given the research motivation (Chapter 1) and the methodological preamble (this chapter), Chapter 3 will provide a detailed semiconductor manufacturing industry context discussion and literature review, including describing the case selection process for the two technology transitions studied and modeled throughout the remainder of the dissertation.

Chapter 3: Semiconductor Industry Context and Case Selection

"Don't be encumbered by history. Go off and do something wonderful."

- Robert Noyce

3.1 General Semiconductor Industry Background

The semiconductor industry has long been an arena of intense interest to academicians, policy makers, and electronics and IT industry participants and analysts. Economists have unambiguously demonstrated the centrality of the IT and semiconductor industries to economic growth. For example, a National Academies report (Jorgenson and Wessner 2004, pp. 57-59) estimates that from 1995-1999 that about a third of the US GDP growth was due to IT and semiconductors despite constituting only 7 percent of the GDP itself. Along with many industries, the semiconductor industry suffered mightily during the "Great Recession" of 2008-2009, experiencing two of its worst years in recent history (Gaudin 12/17/09). However, after a sluggish 2.1% annual growth from 2007-2012, analysts at IC Insights predicted robust growth of 7.4% annually from 2012-2017 (McClean 1/2/13) driven by the explosive global growth of consumer electronic devices, especially mobile phones, tablets, and laptop computers. To feed this insatiable global demand for cheaper, faster, smaller, and lower-power chips, the semiconductor industry must find new ways to continue its amazing track record of rapid, cost-effective technological innovation.

The chip industry has been a fertile ground for studying many aspects of applied economics, management theory, and engineering systems. The industry is well-studied because of the following factors: staggering chip-density and speed improvements, technological and

manufacturing complexity, R&D manufacturing spillovers, intellectual property focus, dynamic customer/supplier relationships, uniquely strong industry roadmapping and inter-firm consortial history, and undeniable import for international trade and national competitiveness. Since so many aspects of the industry have been studied, the literature review presented here will be limited to a brief summary of the prior research with a particular focus on prior research which has a direct bearing on questions addressed by the current dissertation.

Since semiconductors are first and foremost a product of scientific and technological knowledge, scholars of technology, innovation, and strategy have scrutinized the industry carefully using a wide variety of research methodologies. Some scholars (e.g., Brown and Linden 2009, Browning and Shetler 2000, Mathews and Cho 2000, Langlois and Steinmuller 1999) have performed in-depth historical case analysis studies focused on merging secondary data with numerous industry interviews to arrive at holistic and detailed qualitative descriptions of overall trends in the industry. More detailed studies of particular aspects of the semiconductor industry have spanned a wide gamut, including studies of: intellectual property (e.g., Hall and Ziedonis 2001), chip pricing and Moore's Law-based technological evolution analyses (e.g., Aizcorbe and Kortum 2005, Kim and Lee 2003, Pillai 2011), incumbency vs. new entrants (Iansiti, 2000), learning processes (Wright 1997, West and Iansiti 2003, Shuen 1994), and R&D partnerships (Song 2011, Link et al. 1996, Longo 1995).

While almost all of the previous studies of the semiconductor industry (as with most studies of technology and innovation) are historical studies of prior technology and economic transitions, this thesis is largely aimed at exploring and developing strategic tools for two real-time *ongoing* transitions (as of the writing of this thesis in early 2013). Hence, a number of the conclusions from this work fall in the realm of specific insights for semiconductor industry participants and

scholars, while other conclusions fall in the realm of more generally applicable tools and processes for strategy development and R&D decision making. In particular, this thesis examines how/when parsimonious game theory models can (or can't) be used to understand firms' R&D spending decisions for the very largest technology transitions in oligopolistic multi-tiered value chains (through detailed analyses and models of the semiconductor manufacturing industry).

3.2 Current Technology and Supply Chain Trends in Semiconductor Manufacturing

Moore's Law is a well-known and well-studied empirical prediction about the amazing and unrelenting rate of technological improvement of semiconductor chips central to the technology transitions underlying the modeling efforts of this thesis (Chapters 4 through 6). Originally stated by Gordon Moore in 1965 (Moore 1965), the updated 1975 version (Moore 1975) predicts that the number of transistors per semiconductor chip doubles approximately every 24 months. Since Moore's prediction, the industry has undergone a remarkable number of technical transitions which have, in fact, kept pace with Moore's Law up to the present day. It is generally agreed (Pettinato and Pillai 2005) that the three main categories of innovations driving semiconductor chip improvements to date have been:

- Shrinking of transistors sizes (powered largely by improvements in a nano-scale silicon patterning technology called photolithography)
- Periodic increases in manufacturing silicon wafer size (historically, approximately once every 8-12 years, prior to the longer time gap to the currently proposed transition to 450mm diameter wafers)
- Improvements in chip transistor layout/design

Figure 3 below illustrates a simplified representation of the semiconductor manufacturing supply chain which is quite complex both technologically and economically.

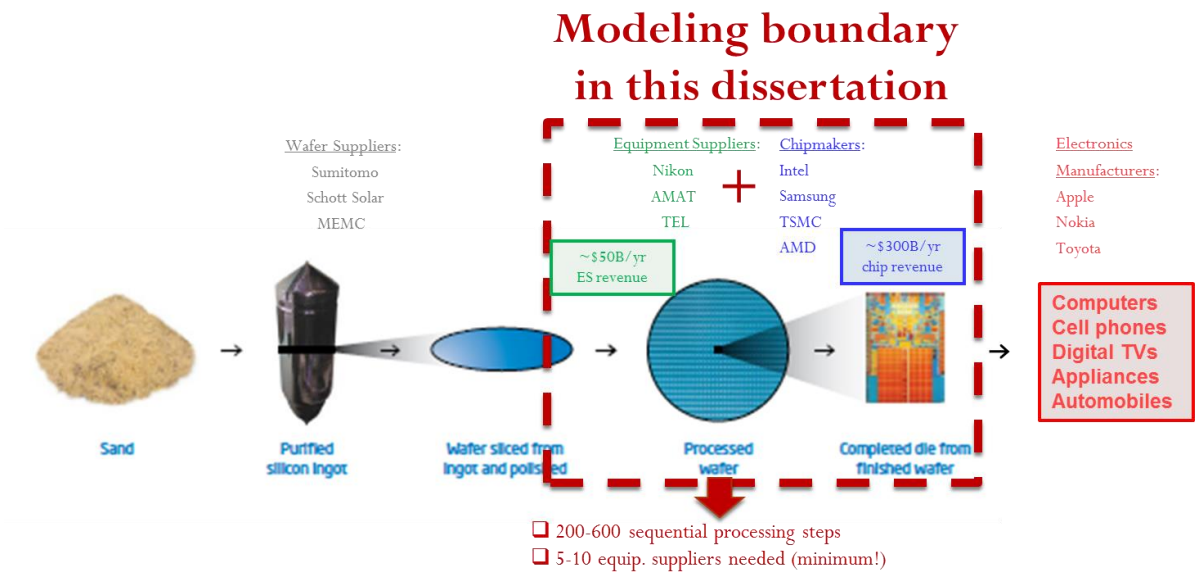


Figure 3: Overview of Semiconductor Manufacturing Supply Chain (adapted from Intel 2010)

Undoubtedly, many stakeholders beyond the industry firms identified in Figure 3 are concerned with understanding (and hence strategically influencing) the competitive dynamics in this industry. These stakeholders include: national governments (especially economic and innovation policymakers), international trade and regulatory bodies, and technology firms in adjacent market segments (e.g., software companies). For the purposes of this dissertation, the modeling boundary chosen (see Figure 3) encompasses only the chipmakers and their upstream semiconductor fabrication equipment suppliers. Future extensions to this work may also include other firms or stakeholders within an expanded modeling boundary. One boundary expansion with rich potential would explicitly incorporate the economic impacts of downstream electronics suppliers (e.g., Apple, HP, and Dell). Although the model boundary chosen enhances

tractability, all practical strategic results must be analyzed and interpreted within the broader institutional context of this complex socio-technical system.

3.3 Semiconductor Industry Consolidation Suggests Game Theory is an Appropriate Modeling Approach

R&D and manufacturing costs required for semiconductor fabrication have been continually escalating due to ever-shrinking transistor sizes, larger wafer sizes, and innovations in chip transistor layout/design. These rising costs have induced dramatic (and ongoing) industry consolidation in both the chip manufacturer and equipment supplier tiers of the value chain, progressing to the point of oligopolistic competition with only two or three viable competitors remaining in virtually all market segments (see Figure 4 and Table 1 below). This dramatic monotonic horizontal consolidation in the chip manufacturing and semiconductor equipment tiers of the supply chain suggests the possibility of new ways for strategically analyzing the semiconductor supply chain.

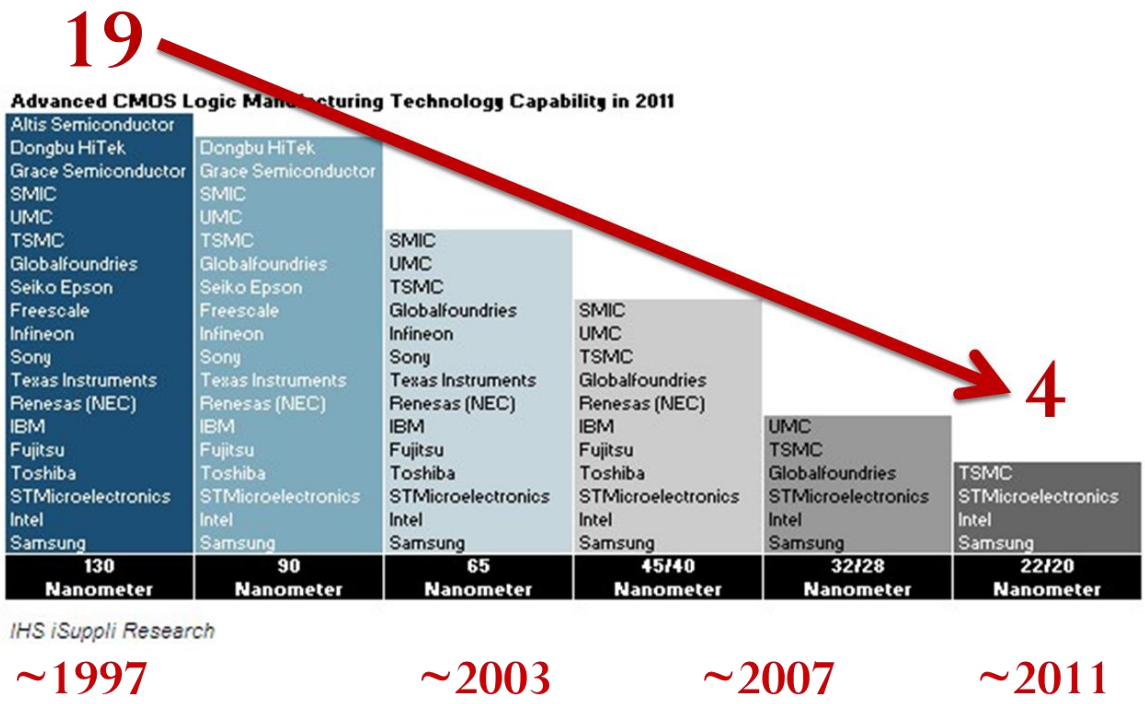


Figure 4: Dramatic Consolidation of Chip Manufacturers since the Late 1990s (adapted with permission from IHS, Inc. Original source: Jelinek 2/20/11)

Table 1: Dramatic Consolidation of Semiconductor Equipment Suppliers since 1981 (data from slides 10 and 11 of Hutcheson 1/12/11 of VLSI Research)

Equipment Suppliers (All Segments)

	1981	2011
# Suppliers	~300	~140
Top-10 mkt. share	45%	60%

Source: VLSI Research

3.3.1 The Rise of the "Fabless/Foundry Model" in Semiconductor Manufacturing

Over the past several decades there has been significant *vertical disaggregation* of the supply chain with (in many cases) distinct specialized firms providing electrical chip design, semiconductor fabrication services, and semiconductor manufacturing equipment. In portions of the semiconductor industry with a vertically disaggregated value chain, very close cross-firm coordination has been necessary for both day-to-day cooperation and for many long-term technology and R&D projects. One prominent feature which exemplifies the vertical disaggregation of the semiconductor value chain is the rise over the last two decades of the so-called "fabless/foundry model" which allows small- and medium-sized chip design firms (e.g., fabless companies such as Qualcomm and Broadcom) to have access to outsourced contract-based semiconductor fabrication services at large, specialized chip manufacturing firms (e.g., foundries such as TSMC and GlobalFoundries) which enjoy the economies of scale associated with large manufacturing plants and semiconductor manufacturing R&D organizations. The success of this business model helped accelerate the consolidation shown in Figure 4. However, there is a vigorous debate regarding the continued strength and viability of the fabless/foundry disaggregated business model going forward (e.g., Jones 6/15/12).

3.3.2 Strategic Modeling Implication of Semiconductor Manufacturing Consolidation

Because so few firms compete in the manufacturing portion of the semiconductor value chain (now often only two prominent firms in a given *market segment*), it has become appropriate to consider the possibility of modeling certain inter-firm strategic dynamics during technology transitions using game theory (along the dimensions outlined in Chapter 1). The goal of Chapters 4 through 6 is to explore this possibility fully within the semiconductor industry, to

push it as far as is justifiable, and to characterize the limits to this approach (which will be summarized in Chapter 7).

While exact figures are difficult to obtain due to the fabless/foundry distinction described above, it is clear that the three largest chip manufacturers by revenue, and likely by silicon wafer volume as well, are Intel, Samsung, and TSMC. Recent data shows that those three largest chipmakers produced about one-third by revenue of the semiconductor output worldwide in 2012 (Notebookcheck 3/28/13). Also, those three companies have been the largest semiconductor capital equipment purchasers since 2009 and they comprise over half of that $30B-$50B annual spending bucket (EE Times 1/20/2012; Solid State Technology 1/23/12). As shown in Figure 5 below, these different chip manufacturers tend to specialize in certain sub-categories of chips (e.g., memory chips, microprocessors, etc.). However, importantly, these specialization boundaries seem to be blurring significantly over time, concomitant with the rise in significance of the semiconductor foundries (e.g., TSMC, GlobalFoundries, and more recently portions of Samsung as well). Despite the end chip market specializations, the same fundamental manufacturing platform is common to all the major chip markets, meaning that semiconductor sales (or "equivalent sales" for foundry chip manufacturers) and capital equipment expenditure are reasonable first-order proxies for market power and significance of the various chip manufacturers during fundamental semiconductor manufacturing transitions.

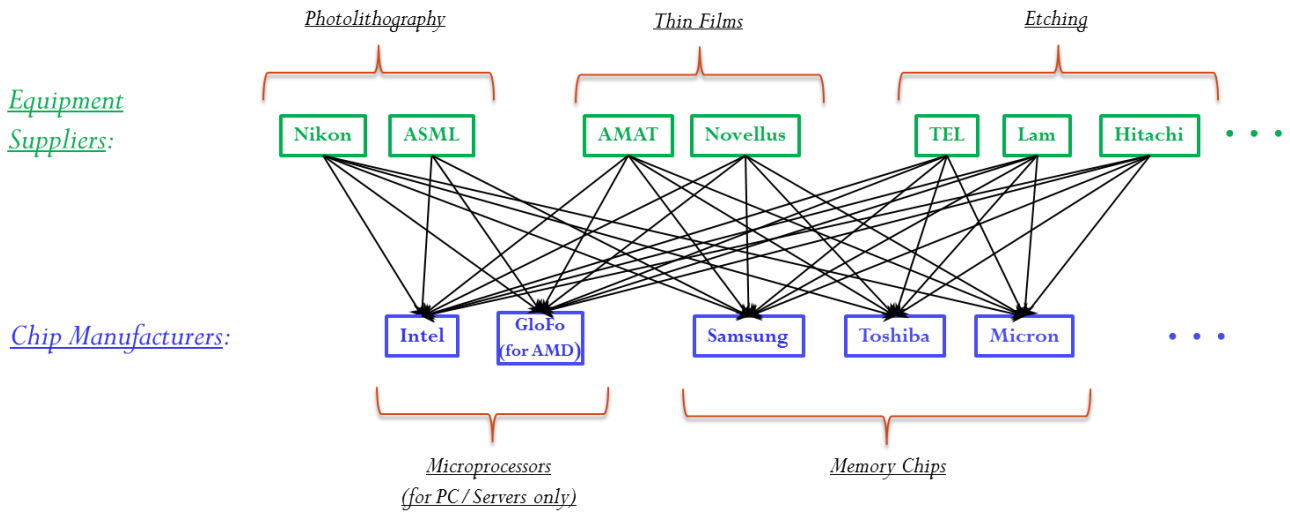


Figure 5: Schematic of the Chip Manufacturer and Equipment Supplier Tiers of the Semiconductor Supply Chain

In the photolithography equipment market, quite arguably the most technologically sophisticated of the semiconductor equipment segments, there has also been dramatic industry consolidation. There were numerous viable photolithography equipment suppliers in the 1960s, 1970s, and 1980s (Henderson and Clark 1990). However, by the mid-2000s and to this day, there were only three lithography equipment suppliers with any significant market share (see EE Times 4/1/12; Chuma 2006). Furthermore, for the current most cutting-edge photolithography technology, dubbed 193nm immersion lithography, only two of these three suppliers remain – the market leader, ASML, with approximately 80% market share and a market laggard, Nikon, with the remaining 20% market share (EE Times, 4/1/12). Additionally, it was universally acknowledged at the time of the EUV model development in Chapter 4 (late 2011) that ASML had a formidable multi-year lead over Nikon in R&D on the next generation of lithography equipment, the so-called extreme ultraviolet (EUV) lithography technology and that these two companies were the only ones seriously considering the development and introduction of EUV lithography technology (McGrath 4/1/12). Finally, in many of the other non-lithography semiconductor

equipment segments (ion implantation, thin films deposition, etc.) there are often only two viable suppliers which command the virtually all of the market share in that equipment segment (Hutcheson 2013).

Figure 4 above is a stylized schematic of this concentrated market structure at both of the tiers of the supply chain being studied in this dissertation. The chip categories are not comprehensive, and the customer-supplier linkages are meant only to represent *potential* linkages – not actual equipment supply flows currently active in the industry. As posited earlier, this dramatic consolidation at both the chipmaker and equipment supplier levels of the supply chain raises the distinct possibility that one can now employ strategically useful non-cooperative game frameworks to describe and, at least to some degree, predict the key interactions among the few remaining participating firms in the large technology transitions that the industry faces. Clearly, minor decisions and strategic interactions are not prime candidates for such analysis (due to unfavorably low economic "signal-to-noise ratios"). However, for very large semiconductor manufacturing technology transitions (e.g., ones costing multiple billions of dollars and those which only tend to occur every 5 to 10 years or even less frequently) the development of such games is a promising idea worth exploring.

3.4 Four key semiconductor manufacturing technology transitions (as of 2012)

As of 2010-2011, the four main manufacturing technology transitions collectively facing the semiconductor industry were: EUV lithography, 450mm wafers, 3-Dimensional Integrated Circuits (3D IC), and vertical transistors (EE Herald, 6/23/11). In addition to the broad consensus on key transitions in industry trade publications, this sentiment was consistent with informal interviews I performed with semiconductor industry experts. Hence, I examined these four technology transitions further for their suitability for game theoretic strategic analysis (along

the lines outlined in Chapters 1 and 2). Recall that some key transition traits engendering suitability are: clarity of the technological requirements of the transition, a relatively "monolithic" characterization of the transition (meaning that it is unified and associated with a well-delineated manufacturing platform), clarity regarding which firms are most likely to develop and implement the necessary technology, and relative difficulty of new market entry.

Because 3D IC and vertical transistors are not monolithic manufacturing transitions and the large chipmakers' options and plans are not distinctly delineated, these two transitions were deemed inappropriate candidates for the proposed game theoretic modeling. The 3D IC manufacturing transition is less a single manufacturing technology transition, and more an interesting amalgamation of semi-related "point solution" efforts in various chip market segments (Armbrust 2012). Although vertical transistors (a.k.a., 3D-transistors or fin-FETs) represent a more consistent trend in the industry (with all the major foundries and integrated device manufacturers [IDMs] either already producing or having announced plans for such transitions), chipmakers are largely developing this technology "in house" and are executing to their own plans and timelines.

However the EUVL and 450mm transitions are both substantially monolithic, making them more suitable for the game theoretic analysis developed here. Now that we have narrowed our scope to these two industry technology transitions, let's take a deeper dive into each of these ongoing technology transitions.

3.4.1 Background on the current transition to EUV Lithography

It is widely agreed that photolithography improvements have been at the very heart of Moore's Law improvements in computer chips (e.g., Chuma 2006; Krzanich 2011). In lay terms,

photolithography is the process of projecting light through carefully designed masks to achieve nanoscale patterning of features on an engineered device. Figure 6 below shows the progression of photolithography equipment improvements (and corresponding light source wavelengths) super-imposed onto ongoing microprocessor and memory chip transistor size reductions. Although this 2007 diagram is somewhat dated, it illustrates the tremendous patterning capability "reset" which EUV lithography enables. The large downward arrow shown in 2011 indicates the ~15X reduction of exposure wavelength possible with EUV lithography. This fundamental wavelength reset is vital because the use of a smaller wavelength of the exposure light source makes the lithographic patterning of the increasingly miniscule features on computer chips much easier to accomplish.

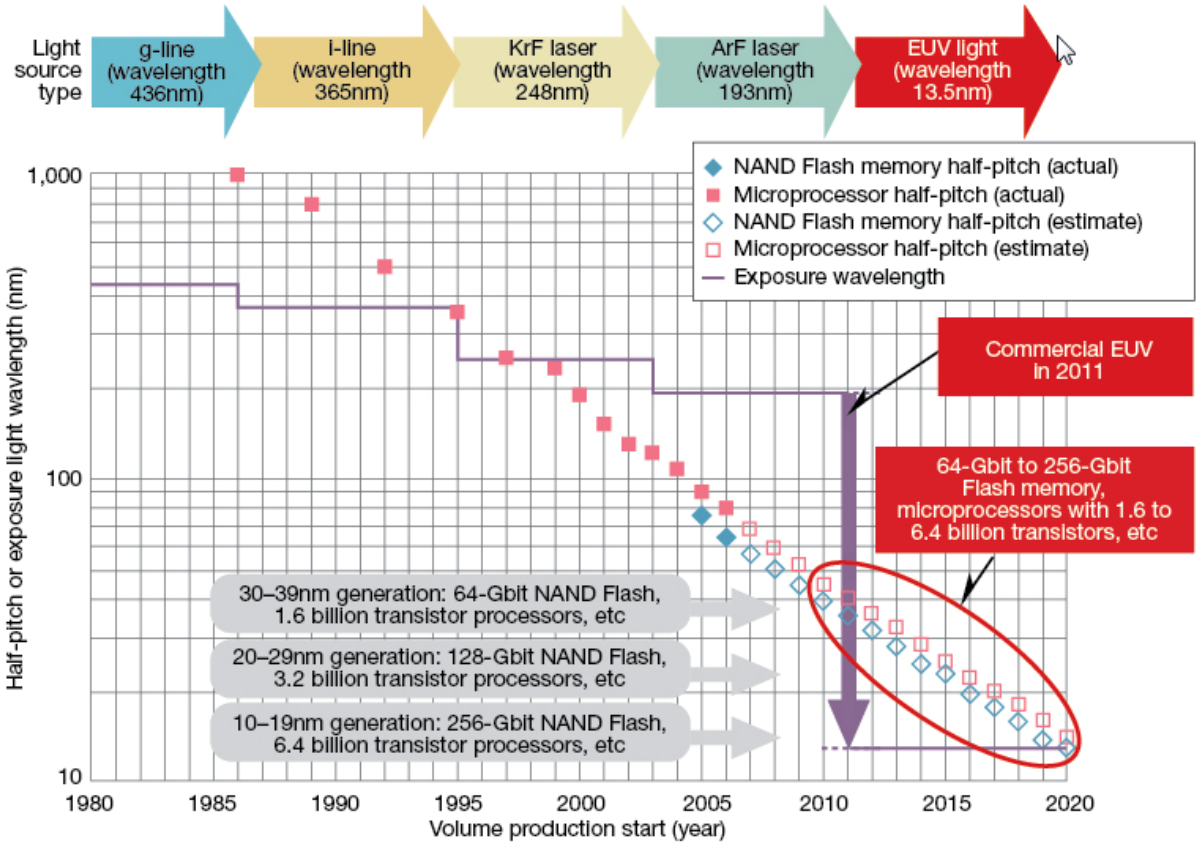


Figure 6: Schematic Illustration of the Importance of EUV Lithography to Continuation of Moore's Law (adapted with permission from Kimura 9/26/07)

Despite the fact that optical lithography was deemed to have an "unexpected long life" in 1995 (see Henderson 1995), with some significant modifications and auxiliary technology improvements, optical lithography is still the dominant chip patterning technology used in semiconductor manufacturing today. However, the continued future use of optical lithography to pattern smaller features *with continued cost-effectiveness* is now highly questionable. This is due to the amazing technological and scientific complexity becoming embodied into photolithography equipment. Chuma states that "[Photolithography] is often regarded as an ultimate precision tool in human history and represents the quintessence of the latest scientific and technological knowledge." (Chuma 2006, pp. 395)

It is widely believed that there are two likely paths forward for the near-future of photolithography. The first is finally improving EUV lithography equipment to the point of commercial viability (which is largely an issue of increasing wafer throughput of the currently slow, but process-capable, EUVL "Beta" equipment. The second (fallback) option is to continue using current optical lithography patterning equipment in a much more expensive multiple patterning mode in which two to five times the amount of current optical lithography equipment, as well as significantly increases in non-lithography equipment, must be utilized (see Merritt 9/12/12). These two lithography technology options are the ones explicitly considered and modeled in the EUVL model developed in Chapter 4.

EUV lithography is a dramatic technological departure from the existing optical photolithography solutions corresponding to an approximately 15X reduction in wavelength of electromagnetic radiation used (from 193 nm down to 13.5 nm). For a further description of the dramatic technological shift that EUV represents see Lin (2006).

Because of the extremely high technological complexity of EUV lithography, it is not surprising that there have been many push-outs to the commercial introduction date of EUV. The original expected introduction years included 2009 and 2011 (see Clarke 10/10/03; Kimura 9/26/07; Hutcheson 2013), and fully commercial technology has not been introduced yet as of early 2013. In the next section, the prior academic work over the last three decades studying the photolithography equipment industry will be briefly summarized.

3.4.2 Prior Academic Studies of the Photolithography Equipment Industry

In the 1990s Rebecca Henderson performed seminal economic studies of the semiconductor photolithography equipment industry (Henderson 1995; Henderson 1993; Henderson and Clark 1990). Her work concluded that incumbent firms in this industry became caught in capability traps and thus became unwilling and/or unable to invest sufficiently in the new skills required to retain market leadership as new vintages of photolithography equipment were successively introduced. This ossification of existing suppliers' thinking and efforts enabled new entrant lithography suppliers to "leapfrog" existing suppliers and gain substantial (and even dominant) market share as each new vintage of lithography equipment was introduced. More recently, Kapoor and McGrath (2012) determined that the nature of inter-organizational lithography R&D collaboration underwent significant shifts from 1990-2010 over the life cycle of the current workhorse class of optical photolithography equipment (so-called 'DUV lithography'). Chuma (2006) studied the differing organizational and innovation practices which led to one lithography equipment supplier (ASML) attaining a substantial market lead over the others in the early 2000s, a lead which persists to the present day. This market lead persistence indicates that the photolithography equipment market has shifted away from the repeated market leadership leapfrogging which was observed in Henderson's earlier studies. It is firmly from within this

new era of high persistence among photolithography equipment suppliers that this dissertation's strategic EUV lithography model (Chapter 4) was developed; the high level of persistence and associated market share concentration implies that the EUVL transition is an oligopolistic transition amenable to game theoretic analysis (per the criteria outlined in Chapter 1).

Much academic research has been done on so-called Next Generation Lithography (NGL), which designates the broader set of possible successor technologies to current optical lithography technologies (including EUVL). Linden et al. (2000) and Mowery (2003) examined the efficacy of public/private R&D alliances to help develop NGL technology, especially an expansive one for early EUV lithography research between large semiconductor firms and three US National Laboratories established in 1997. Several scholars (Möllering 2010; Sydow et al. 2012a; Sydow et al 2012b; Appleyard 2008) have since examined the processes by which support for alternative NGL technologies has been systematically weighed and, over time, winnowed down to primarily one technology – EUV lithography. Lange et al. (2013) examine the individual and collective approaches taken to help fund EUVL development. These studies all provide relevant context to the EUV lithography R&D investment game theory model framework developed in Chapter 4. Figure 7 below summarizes this prior work on photolithography.

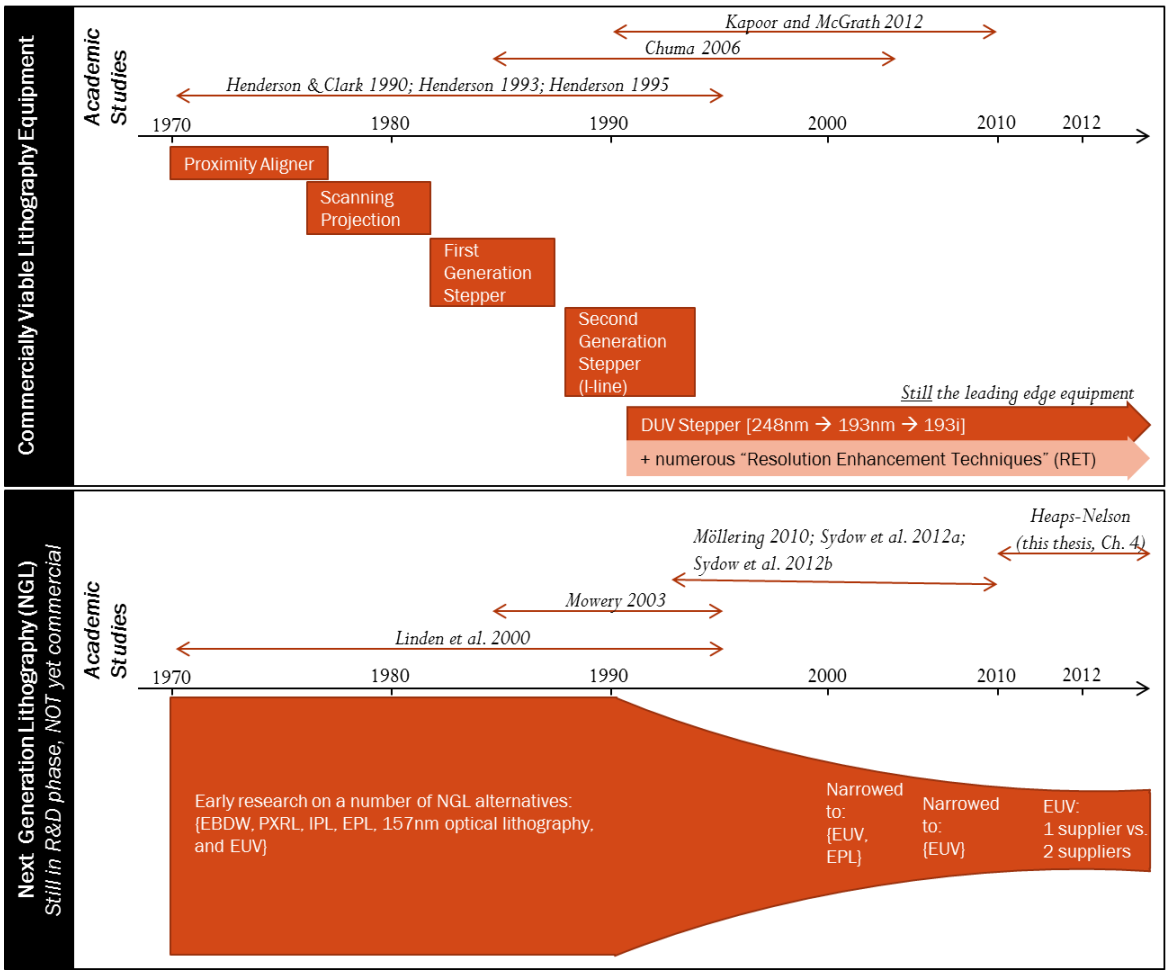


Figure 7: Schematic of Prior Photolithography Equipment Vintage Transitions and Studies

3.4.3 Background on the Proposed Transition to 450mm Diameter Wafers

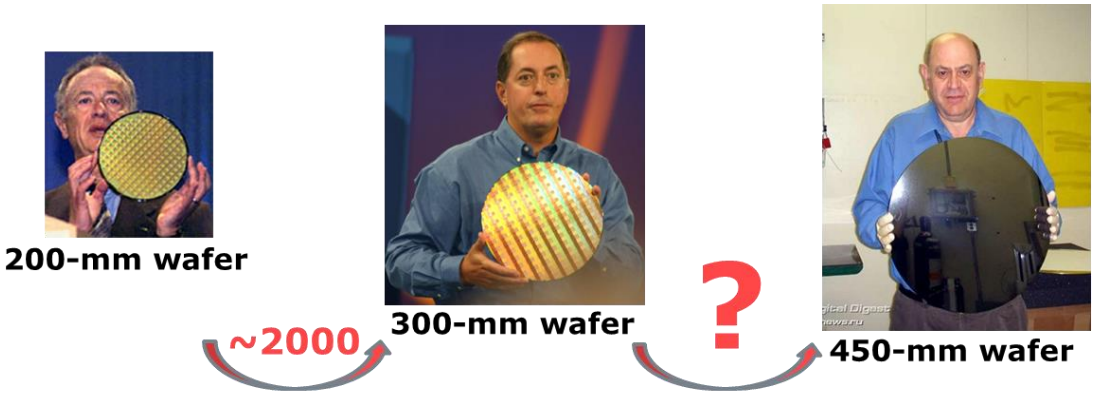


Figure 8: Dramatic Silicon Areal Increases Due to Wafer Size Diameter Increases

The wisdom and timing of the silicon manufacturing wafer-size transition currently under consideration (i.e., moving from 300mm- to 450mm-diameter wafers) was being vigorously debated among the various industry participants at the approximate time of the model development (Lapedus 10/25/10). The potential transition is pictorially illustrated in Figure 8 above. Vis-à-vis the 450mm transition, each key industry firm has partially overlapping and partially conflicting strategic interests with the others. A wafer size increase requires extremely high levels of inter-firm coordination since a minimum of five to ten semiconductor equipment suppliers must simultaneously develop technically compatible flavors of wafer processing equipment (capable of using the larger wafers) for the hundreds of processing steps required for chip fabrication (see Figure 3). Although the semiconductor industry exhibits significant inter-firm coordination on a year-in, year-out basis, the infrequent wafer-size transitions necessitate even more highly cultivated inter-firm coordination (see Hutcheson 2006).

Semiconductor wafer-size increases are undertaken in anticipation of reduced long-run manufacturing costs per chip. For a 50% increase in diameter, chip output per wafer increases

by about 130%, significantly outstripping the increase in manufacturing cost per wafer. Aggregate estimates of the long-run manufacturing cost savings (per chip) expected for this transition range from 10%-40% (SEMI 9/1/12; Mack 8/20/12; McGrath 7/9/12). Despite the possibility of large aggregate industry cost savings, not all industry firms favor the proposed transition to 450mm wafers. In particular, some smaller chipmakers and equipment suppliers will not be able to afford the expense required to make the transition themselves. Such firms may be forced to merge with others or to exit the market altogether (Mack 8/20/12).

Additionally, equipment suppliers have a unique, asymmetric relationship to chipmakers during large technology transitions, including shifts to larger wafer sizes. Within the context of NGL decisions, Möllering states: 'The interviewees agreed that "the financial risk of going the wrong way is considerable, especially for small suppliers" (interview with consortium). Even representatives from major customers (chipmakers) conceded that "unfortunately for the suppliers the risks are much, much higher" (interview with chip manufacturer).' (Möllering 2010, pp. 22). Some of this perception is undoubtedly driven by the fact that equipment suppliers must develop new equipment significantly in advance of its use by chipmakers for volume manufacturing and thus experience long payback periods and great demand risk.

It is also well understood that chipmaker revenues (and employment levels) are typically more stable on average than those of equipment suppliers, consistent with the presence of the bullwhip effect in this industry (Handy 2012). These asymmetries clearly suggest that efforts at risk-sharing vertically across the supply chain for fundamentally new equipment development are appropriate for major new equipment development (Möllering 2010, pp. 22; Longo 1995).

The totality of these factors conspired to make the last wafer-size transition (from 200mm to 300mm diameter wafers in the late 1990s and early 2000s) much more economically painful for the equipment suppliers than for the chipmakers (Hutcheson 2006). Industry analyst C.J. Muse was not alone in his October 2010 assessment: "We believe 450-mm is going to happen, but is likely to involve funding from chip companies. Equipment companies will not foot the bill alone this time." (Lapedus 10/25/10). Stated in other terms, leadership by a subset of the largest chipmakers (and probably partial equipment R&D financing and/or risk-sharing) will be necessary to incentivize and enable the transition to 450mm wafer semiconductor fabrication. In fact, during the course of this research a global consortium dubbed G450C, consisting of five chip manufacturers (Intel, Samsung, TSMC, GlobalFoundries, and IBM) and the state of New York, was announced in September 2011. This consortium quickly established close ties to the semiconductor equipment suppliers and clearly serves the purposes of 450mm roadmap definition and risk-sharing.

3.4.4 Largest Chipmakers' Perspectives on 450mm Wafer Fabrication

The largest chipmakers desire a transition to 450mm wafers both because they anticipate lower long-run manufacturing costs and because they expect fewer chipmaking competitors to remain after the transition (Mack 8/20/12). However, the large chipmakers also each strongly prefer not to unilaterally financially contribute to new equipment R&D by the suppliers (unless they could recoup some of the investment by a large enough first mover advantage). Said differently, a chipmaker who desires quick development of 450mm wafer equipment would like to find effective mechanisms to induce other "co-travellers" among the chipmakers to share in the equipment R&D investment burden instead of allowing free-riding on its desire to make 450mm

wafer fabrication an expeditious reality. A secondary reason large chipmakers want 450mm wafer technology is that it reduces chemical, energy, and water usage on a per chip basis (Vogler 5/18/11; Trafas 3/1/12).

Though less fully a fit than the EUVL transition to the Chapter 1 criteria for transitions of interest (for reasons to be fully elaborated in Chapter 5), the 450mm transition possesses enough of the appropriate characteristics to make it a worthy transition to study within the context of this dissertation. Chapters 5 and 6 provide several versions of game theoretic models which illuminate this transition. Thus, a terse summary of the previous studies on wafer-size transitions is given below.

3.4.5 Prior Studies of Wafer-size transitions

Although less research has been published about wafer-size transitions than about photolithography transitions, some studies have been performed (e.g., Hutcheson 2006; George 2009; Chien et al. 2007).

3.5 Situating Dissertation Models within the Extant Semiconductor Manufacturing Literature

For context, I give a summary of how the work in this dissertation (on both EUVL and 450mm wafers) fits into the extant research studying semiconductor manufacturing in Table 2 below.

Table 2: Situating Chapters 1-3 in the context of extant semiconductor-focused literature

Topics in semiconductor-focused literature	**EUV Lithography-related research**	**450mm Wafer Transition-related research**
Studies of Precursor Technologies (e.g., Earlier Lithography Equipment and Wafer-size transitions)	Henderson and Clark 1990 Henderson 1993 Henderson 1995 Kapoor and McGrath 2012 Chuma 2006	Goodall et al. 2002 Hutcheson 2006
Industry Mechanism for Selecting among Alternative Potential Technologies	Möllering 2010 Sydow et al. 2012a Sydow et al. 2012b	Not Applicable
Quantitative Estimation of Technology's Contribution to Aggregate Industry Value	**Quantitatively modeled in this thesis (Chap. 4)**	Chien et al. 2007
Determination of Non-cooperative R&D Funding Equilibria	**Quantitatively modeled in this thesis (Chap. 4)** Appleyard et al. 2008	**Quantitatively modeled in this thesis (Chap. 5&6)** Hutcheson 2006 George 2009
Analyzing Mechanisms for Attaining Non-cooperative R&D Funding Equilibria	Lange et al. 2013	*[Future work]*

In addition to these prior studies of photolithography and wafer-size transitions (Table 2), there have been other important studies of chipmaker/equipment supplier R&D interactions, including formal joint development programs, for other semiconductor manufacturing technologies (e.g., Lim 2009; Appleyard 2002; Longo 1995; Langlois 2000). There have also been numerous studies of the role of industry consortia, especially Sematech, on the advancement of semiconductor manufacturing (e.g., Browning and Shetler 2000; Langlois and Steinmuller 1999; Link et al. 1996; Corey 1997).

3.6 Specific Research Question (for Chapters 4 through 6)

Given the detailed industry context and literature review outlined above, the general research question posited at the beginning of Chapter 1 is now narrowed down to the more specific research question which is the focus of the bulk of this dissertation (Chapters 4 through 6):

How can firms make better strategic semiconductor equipment R&D financing decisions during large, tightly-coupled industry technology improvements such as EUV lithography and manufacturing with 450mm-diameter silicon wafers?

The next chapter contains the first semiconductor case study, a detailed examination and game theoretic model of the ongoing EUV lithography (EUVL) transition.

Chapter 4: The EUV Lithography (EUVL) Model

"At no time have industry executives faced more strategic uncertainty or greater doubt about the future effectiveness of past competitive and collaboration models."

- Tom Morrow, Industry Consortium Executive (February 2012) (from Morrow, 2/9/12)

4.1 Game Structure of EUVL Model

Given the semiconductor industry background and case selection described in Chapter 3, I describe in detail the two technology transition cases in this chapter (EUV lithography) and in Chapter 5 (450mm wafers). It will turn out that there is much stronger industry evidence supporting the modeling of EUV lithography development as a parsimonious game than there is for modeling the transition to 450mm wafers in that fashion. This evidence includes internal model consistency, validation of model structure and inputs, and confirmatory recent financing events in the semiconductor manufacturing supply chain. A deeper comparison of the differing efficacy of these two modeling efforts will be provided at the end of Chapter 5 after we examine each of the two cases/models in depth.

First, I quickly recapitulate the extended EUVL history and supply chain context provided in Chapter 3 (covering the timeframe prior to this case study, which culminated in the events of October 2011). Just as with Moore's Law itself, there have long been predictions of the imminent demise of optical lithography as the patterning workhorse of semiconductor manufacturing (e.g., Henderson 1995). Numerous potential replacements (so-called Next Generation Lithography [NGL] solutions) have been researched and proposed. As described in

Chapter 3, EUV is the most recent of such NGL technologies, and it garnered front-runner status in the mid-2000s. Several significant consortia helped provide early-stage funding of this technology. Only now has the urgency of the EUV lithography transition reached a fevered pitch due to the dramatically increasing patterning costs inherent in the prospect of continued extensions of optical technology using double or multiple patterning (DP/MP). This costly extension of optical lithography would require two to five times as many lithography exposures (with roughly proportional throughput reductions) than current single exposure technology (see Lapedus 6/10/09; Merritt 9/12/12). One lithography equipment supplier (ASML) has a dominant position in both the current cutting edge optical lithography (~80% market share) and a multi-year lead in EUV lithography development. The trailing lithography supplier (Nikon) has the remaining 20% share in current optical lithography and lags significantly behind ASML in EUV lithography development. Although ASML possesses a commanding lead in EUVL development, there have nonetheless been numerous delays in ASML's EUVL roadmaps causing increased anxiety on the part of leading chipmakers (see Section 3.4.1).

It is in this technology and supply-chain context that I developed a game theory model for strategic EUV lithography R&D spending interactions among the key industry players. During the process of defining the game framework, I considered several parsimonious sets of strategic players (either individual firms or, where appropriate, coordinated alliances of firms) and R&D investment strategies possible to those players. After successive iterations, I selected a simplified 3-player finite 2-stage game structure shown in Figure 9. I chose this parsimonious game framework because of the difficulties associated with structuring a tractable (yet economically realistic) game with more than three players and/or with more finely-grained strategies included.

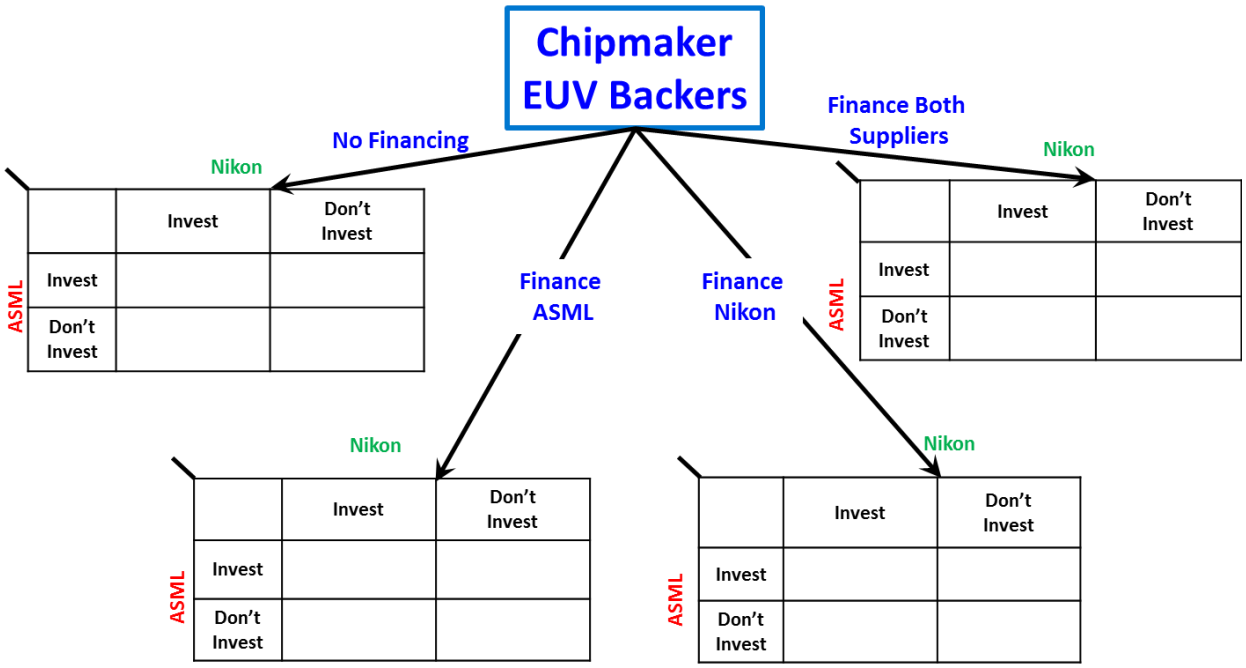


Figure 9: Game Structure for EUV Equipment R&D Financing game

Notice in Figure 9 that the two lithography equipment suppliers (ASML and Nikon) have been defined as distinct and asymmetric players, each deciding (fundamentally) whether to undergo the big push of research required to produce commercial EUV lithography machines or not. The second thing to notice is that I have aggregated the large chipmakers into a single player called "Chipmaker EUV Backers". Because of the special aggregated/amalgamated nature of this player, I have chosen to capitalize "Chipmaker EUV Backers" (sometimes referred to as simply "Chipmakers") to remind the reader that this player represents a subset of chipmakers (i.e., those who choose to help finance EUVL) and that some process of alignment among them is still required to provide the ultimate funding assistance to the equipment supplier(s). I created the amalgamated Chipmakers player for several reasons. One was simply tractability of the game, as it has been observed that gathering insight from strategic game theory models becomes increasingly difficult with the addition of each successive player (e.g., see Papayoanou 2010).

Another reason was the clear evidence of sophisticated financing and coordination mechanisms used in the semiconductor industry in the past (e.g., Longo 1995 and Müller-Seitz & Sydow 2012) leading one to believe that early EUV investors (among the chipmakers) could recoup their investments through early manufacturing cost reductions and/or market share gains. This meant that although it was not clear which particular chipmakers would choose to invest, it was fairly certain that some subset of them would choose to financially support lithography equipment development at ASML, Nikon, or both suppliers through their individual investment decisions. Assuming that such financing would be reasonably efficient and effective, the chipmakers were lumped together into one player and deemed to have four general strategies (which were also their possible *actions,* in the game theoretic sense of the term, since the Chipmakers move first in this two-stage game): 'No financing', 'Finance ASML only', 'Finance Nikon only', or 'Finance both'. Having observed the first-stage action by the Chipmakers, ASML and Nikon were modeled to each have a simultaneous second-stage binary choice to significantly invest in EUV lithography development or not. Robustness to this two-stage sequential game formulation will be considered later in this chapter via re-interpretation and re-analysis of the EUVL game as a single-stage simultaneous move game for all three players.

A careful examination of the game tree in Figure 9 may raise concerns regarding the possibility (in 3 of the 4 proper subgames) that an equipment supplier may choose not to invest in EUVL technology after financing for EUVL development has been provided by the Chipmakers to that supplier. This possibility does indeed exist in the game as formulated. However, because of the payoff structure we have assumed (and because this is a game of perfect information), Chipmakers will never optimally choose an action in stage 1 which allows an equipment supplier to rationally make such a choice in stage 2, given that there is a unique pure strategy Nash

Equilibrium (NE) in each proper subgame. In addition to this mathematical argument which allays concerns about the inclusion of such future states of the world, these states (and their associated player payoff estimates) will be required when I later consider a reformulation of the EUV game as a single-stage simultaneous game.

4.2 Payoff Sub-components for EUVL Model

Given the three players defined in the game and their possible actions (see Figure 9), there are 16 (=4x2x2) possible future states of the world. This also implies the challenging task of estimating the 48 (=3x16) player payoffs which this model framework entails. We first decided to use the expected NPV (a.k.a. E(NPV)) of future profitability of each of the firms as our proxy for each player's utility. This is the same basic E(NPV) approach used frequently in practice in the semiconductor industry and followed by Irwin and Pavcnik (2004) and Morrison et al. (2012) when performing their game theoretic analyses of the aerospace manufacturing industry. Clearly, the E(NPV) approach implies a relatively strong assumption of risk neutrality, especially regarding Nikon, the smaller and EUVL-lagging equipment supplier. Any desired relaxations of this assumption can be performed after the foundational analysis (assuming risk-neutrality) has been done; such relaxations are introduced informally later in this dissertation (e.g., Sections 4.7 and 4.10).

Although the main body of this chapter will only provide the general approach used for E(NPV) payoff estimation for each player in the EUVL model, Appendix A contains a quite detailed quantitative treatment of these calculations. Specifically, Appendix A contains the following items: a complete list of EUVL model variables, parameters, and acronyms used in the calculations; complete expressions of the game-theoretic objective functions and optimization

formulations for each player; a fully explained tabulation of all "base case" EUVL model input parameter estimates with data source attribution; a full set of algebraic equations linking the model parameters to the ultimate payoff estimates; and an example calculation which ensure full traceability to the equipment supplier payoff estimates presented in this chapter.

Given the adoption of an E(NPV) payoff framework, the following factors were incorporated into the payoff calculations for the (aggregated) "Chipmaker EUV Backers":

- Direct expense to Chipmakers of their EUVL equipment R&D financing investments
- Ramp (by year) of expected manufacturing cost savings when high-volume manufacturing EUVL becomes available, assuming that Chipmakers financing would enable pull-ins of EUVL launch dates (which will be provided in Table 3 below) for suppliers which choose to invest in EUVL themselves
- EUVL equipment pricing difference expected between monopoly and duopoly EUVL equipment supply situations

Given these payoff sub-components, the fundamental tradeoff faced by the Chipmaker EUV Backers is driven by two countervailing factors: undesirable monopolistic pricing power in the monopoly EUVL supplier scenario versus the duplication of costly EUVL R&D expenditures in the duopoly supplier scenario. Figure 10 shows a conceptual illustration of this economic tension.

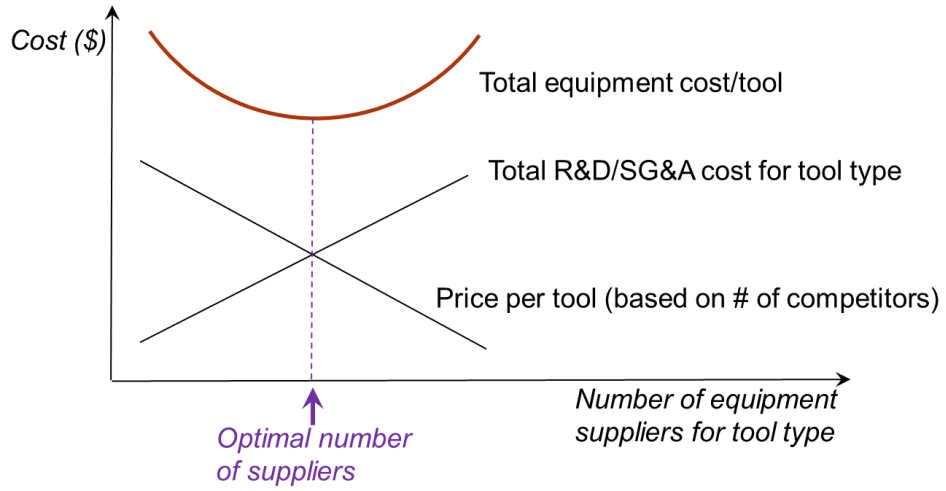


Figure 10: Cost Tradeoff between Equipment Supplier Pricing Power and Duplication of R&D Expenditures

In the semiconductor equipment industry, a rough quantification of this tradeoff was possible after estimating two critical factors:

- A monopoly vs. duopoly equipment price ratio. Both empirical data on equipment supplier gross margins and Cournot duopoly theory can inform rough estimation of this ratio.
- Estimates of the cost (remaining) to complete EUVL development at each lithography supplier. This was calculated by breaking the costs down into specific remaining tasks and estimating: the cost of each task, which tasks were precompetitive (and hence pursued only once), and how much spillover benefit a fast-following equipment supplier would enjoy for each task. As indicated in Table 3 below, the rough estimates arrived at were $2B for ASML and $4B for Nikon, and the fraction of chipmaker investment was estimated at 50% of these amounts. (See Appendix A for more details of these calculations.)

For ASML and Nikon, payoffs were comprised of the following two sub-components:

- Direct expense to equipment suppliers of their EUVL R&D investments (including the reductions enabled by Chipmakers' financing help, where applicable)
- Expected yearly profits for both the current optical lithography equipment product stream and the new EUV lithography equipment product stream (with introduction dates, EUV ramp rates, and market shares all estimated as a function of the actions selected by all three players)

4.3 Scenario Definition for EUVL Model

Given the payoff sub-components enumerated above, let me proceed to describe several key industry attributes which help specify the calculation of payoff estimates. One undeniable reality of this industrial context is the deep technological uncertainty which continues to accompany the potential introduction of EUVL technology (recall from Chapter 3 the numerous delays to the introduction of EUVL already experienced). Industry trade press articles, financial analyst reports, and discussions with industry content experts helped me define five plausible outcomes with respect to EUVL high volume manufacturing (HVM) introduction dates and subsequent ramp envelopes over the modeling period (2011-2021). The investment amounts, EUVL insertion dates, and the ultimate ceiling (i.e., maximum market share achieved) for critical patterning for each of the five assumed EUVL outcomes are shown in Table 3 below. Here critical patterning is defined as lithographic patterning of those semiconductor processing layers with such miniscule features that they require either EUVL or the especially intensive use of current optical lithography associated with DP/MP patterning. (Recall these two cutting-edge

lithography options defined in Section 3.4.1.) The full justifications for these various assumptions are given in detail in Appendix A.

Table 3: Assumed EUVL Introduction Dates and Market Share Ceilings for Five EUVL Scenarios and Investment Amounts by Chipmakers and Equipment Suppliers

Chipmakers EUV Backers Financing Contribution	ASML: Remaining Needed EUVL R&D Expenditure	Nikon: Remaining Needed EUVL R&D Expenditure	**SCENARIO #4.1** "EUV Captures All" (100%)" Anticipated EUVL HVM Insertion Dates:	**SCENARIO #4.2** "Lower EUV Ceiling" (60%)" Anticipated EUVL HVM Insertion Dates:	**SCENARIO #4.3** "2 Year Delay + Lower Ceiling" (60%)" Anticipated EUVL HVM Insertion Dates:	**SCENARIO #4.4** "3 Year Delay + Lower Ceiling" (60%)" Anticipated EUVL HVM Insertion Dates:	**SCENARIO #4.5** "No EUV" (0%) Developed" Anticipated EUVL HVM Insertion Dates:
$0B (No financing)	$2B	$4B	ASML – 2013 Nikon – 2016	ASML – 2013 Nikon – 2016	ASML – 2015 Nikon – 2018	ASML – 2015 Nikon – 2018	ASML – Never Nikon – Never
$1B (Finance ASML only)	$1B	$4B	ASML – 2012 Nikon – 2016	ASML – 2012 Nikon – 2016	ASML – 2014 Nikon – 2018	ASML – 2014 Nikon – 2018	ASML – Never Nikon – Never
$2B (Finance Nikon only)	$2B	$2B	ASML – 2013 Nikon – 2015	ASML – 2013 Nikon – 2015	ASML – 2015 Nikon – 2017	ASML – 2015 Nikon – 2017	ASML – Never Nikon – Never
$3B (Finance both suppliers)	$1B	$2B	ASML – 2012 Nikon – 2015	ASML – 2012 Nikon – 2015	ASML – 2014 Nikon – 2017	ASML – 2014 Nikon – 2017	ASML – Never Nikon – Never

The benefits Chipmakers expect to derive from helping finance EUVL development are mediated by the equipment suppliers' strategic choices regarding EUV investment, which are in turn driven ultimately by the assumed impacts to the HVM introduction dates, ramp profiles, and the anticipated competitive environment for EUV lithography equipment supply. Note from Table 3 above that, absent any Chipmaker financing, Nikon is assumed to be three years behind ASML in EUVL development and that Chipmaker financing for either supplier corresponds to a one-year pull-in of the HVM introduction date for that supplier (see McGrath 4/1/12). The rationale for the one-year pull-in (even when the sum of EUV R&D investment by all players

remains unchanged) is that Chipmaker financing would provide direct financial assistance to the supplier and reduce the time required for EUVL insertion through galvanizing action and reducing uncertainty throughout the EUVL ecosystem (i.e., support technologies and companies required to make EUVL commercially useful). The ASML EUVL HVM introduction dates in 2012 or 2013 roughly corresponded to stated industry roadmaps at the time of the modeling in 2011. As will be shown later in this chapter, given the five outcomes scenarios in Table 3, one can analyze expected game outcomes either by assuming one of the scenarios holds with certainty or by assuming various (discrete) probability distributions across the five scenarios.

4.4 Other EUVL Model Assumptions

In addition to the uncertainty regarding the development and adoption of EUVL technology, a number of other modeling parameter assumptions were needed to quantify the costs and benefits of development of EUVL technology. Recall per the generic modeling assumptions in Chapter 2, I have assumed common knowledge among the three players of each of these parameters. The EUVL model assumptions generally fell into the following categories (all parameters were defined annually from 2011 to 2021):

- Expected annual demand for wafers (which required critical patterning)
- Expected number of critical layers/wafer assumed
- Cost (2011-2021) of patterning layers using EUVL
- Cost (2011-2021) of patterning layers using DP/MP 193i lithography
- Non-recurring investment costs for ASML's and Nikon's EUVL R&D projects
- Division of non-recurring investment costs between the Chipmaker EUVL backers and the lithography equipment suppliers

- Fraction of Chipmakers cost savings which become Chipmakers profits
- Profitability (to the equipment suppliers) of providing EUVL and 193i DP/MP patterning solutions
- EUVL ramp profiles (including competitive dynamics between the two suppliers under the five scenarios defined in Table 3 above)
- Corporate project evaluation discount rates

The full list of model input parameter definitions and base case values can be found in Table 39 and Table 40 in Appendix A. Given the high technological uncertainty involved, a 10-year time horizon was chosen (2011-2021), and a relatively high discount rate (15%) was selected.

For the interested reader, a much more detailed and complete treatment of the payoff calculations (including model parameter justifications and full traceability to the actual payoff estimates derived) is given in Appendix A. The "base case" model results will now be examined in detail. Subsequent to that, the effect of changing the game reformulations and key model parameters on the model outputs/predictions will be tested through robustness checks and model sensitivity analysis (in Sections 4.9 and 4.10 below).

4.5 Base Case EUVL Scenario Game Trees and Equilibrium Analysis

Given this game framework, payoff compositions, and other base case assumptions regarding expected future demand for chips, discount rates, etc., the E(NPV) payoffs for all three players were calculated under the five scenarios assuming differing levels of "technological difficulty" for EUVL equipment development outlined in Table 3. Populating these payoffs in the game tree framework (Figure 9*: Game Structure for EUV Equipment R&D Financing game*) yields the five game trees shown in Figure 11 through Figure 15 below. Note that the underlining in these

figures corresponds to the best responses of each player (given fixed action of the other two players), ovals represent Nash Equilibria (NE) of the four proper sub-games, and thickened arrows and boxes indicate the overall sub-game perfect NE of the game. For convenience, the Chipmaker EUV Backers are designated as Player 1, ASML is designated as Player 2, and Nikon is designated at Player 3. Hence, when an action profile or a payoff triplet of the three players is considered (e.g., ('Finance ASML only', 'Invest', 'Don't Invest') or (($166B, $16.4B, $2.8B)), the first action in the triplet corresponds to the action of the Chipmaker EUV Backers and so on. Additionally, for simplicity, in the EUVL model I have adopted the convention that when E(NPV)s for two choices for a given player are equal, when rounded to the nearest $0.1B, I assume that the player in question chooses the option which involves the smallest total financing/investment amounts.

After the figures displaying the game trees for the five scenarios are shown, the economic intuition behind the results in these games will be explored, with a particular focus on understanding the sub-game perfect Nash Equilibria (SPNE) determined. A summary of the SPNE found in these five scenarios is shown in Table 4 below.

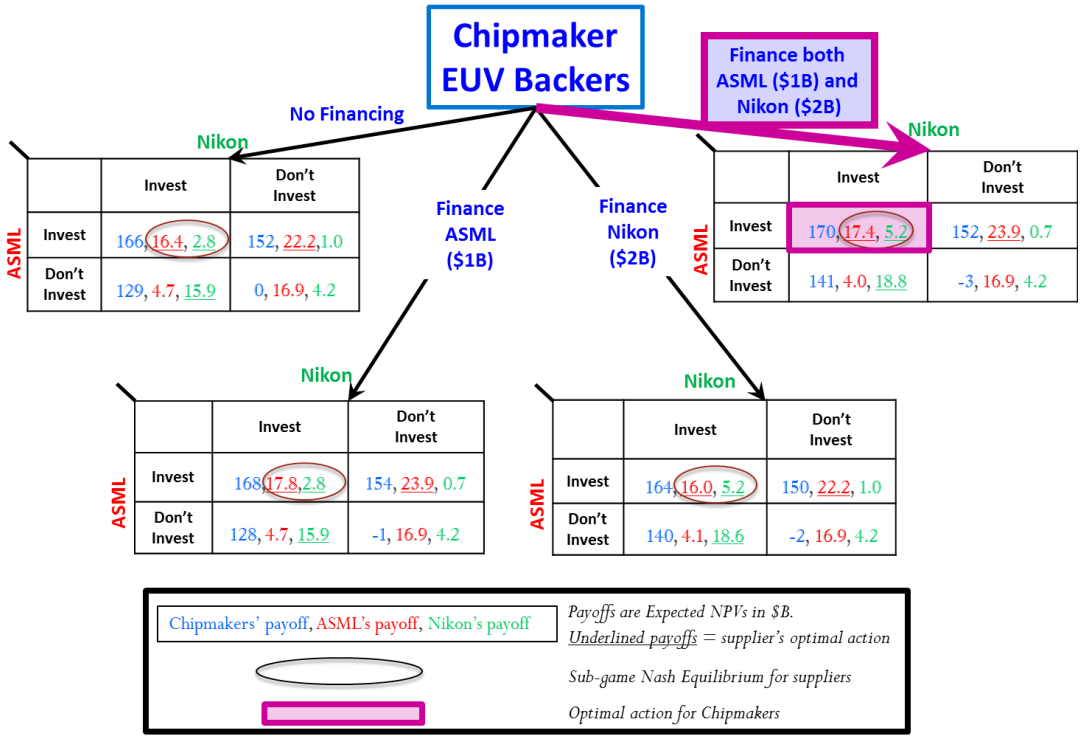


Figure 11: 3-Player Base Case Game Assuming Scenario #4.1 EUVL Difficulty

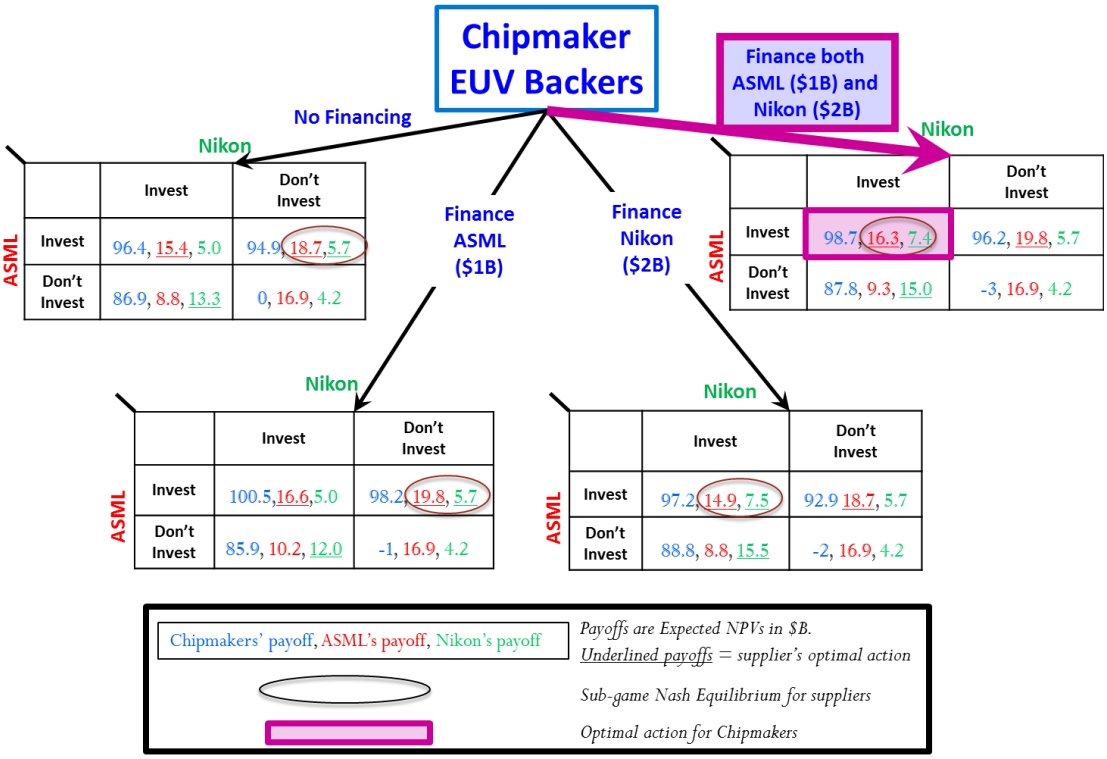


Figure 12: 3-Player Base Case Game Assuming Scenario #4.2 EUVL Difficulty

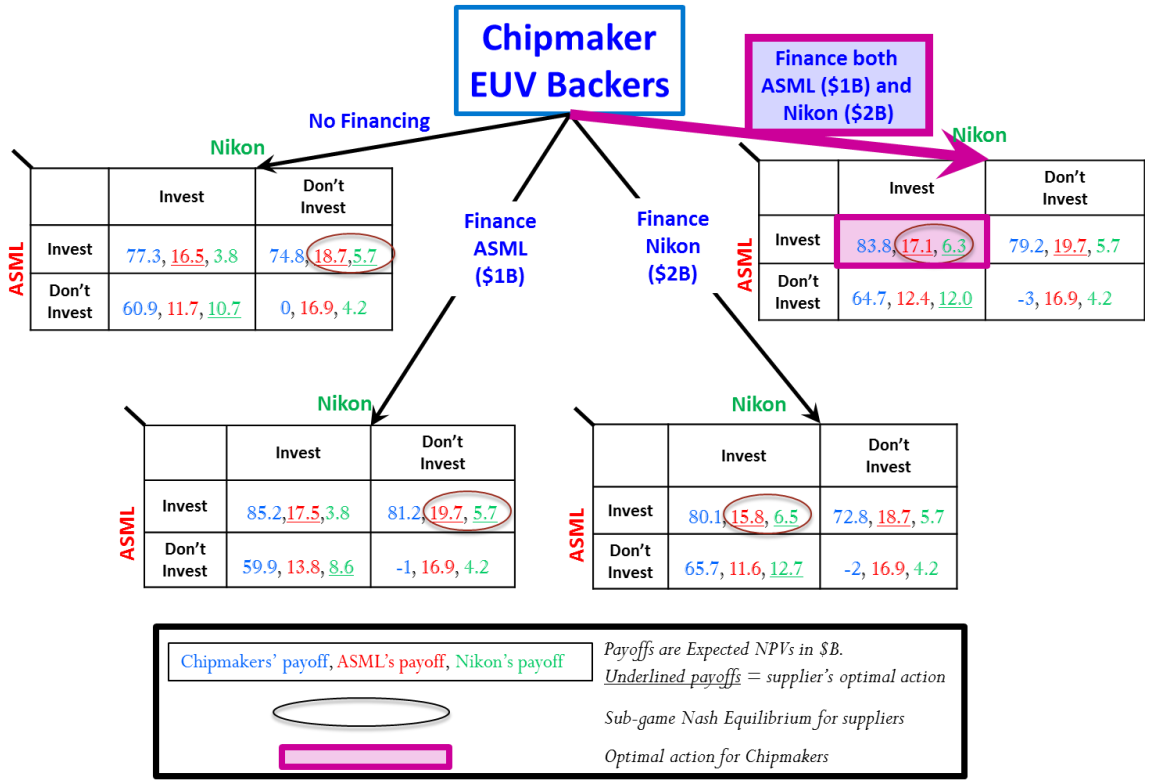


Figure 13: 3-Player Base Case Game Assuming Scenario #4.3 EUVL Difficulty

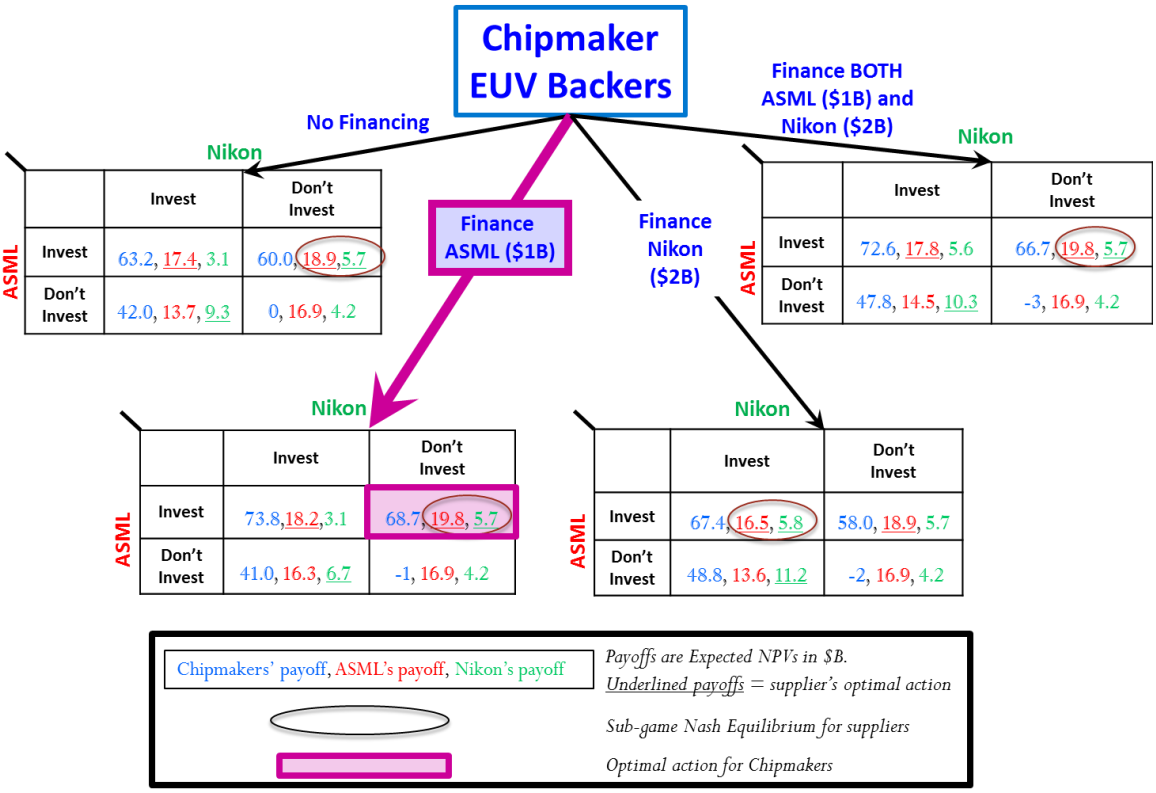


Figure 14: 3-Player Base Case Game Assuming Scenario #4.4 EUVL Difficulty

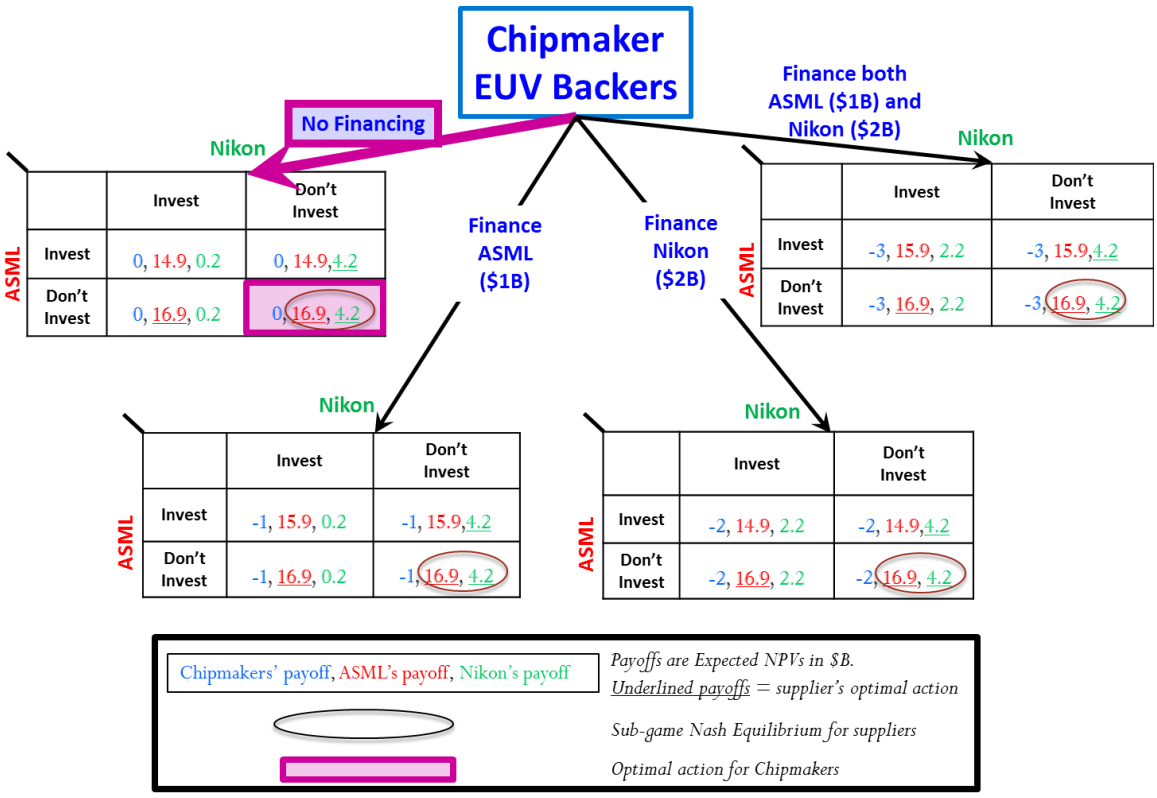


Figure 15: 3-Player Base Case Game Assuming Scenario #4.5 EUVL Difficulty

Table 4: Summary of Base Case SPNE Outcomes for Scenarios #4.1 Through #4.5

		Chipmakers' Actions			
EUVL Scenarios:		No Financing	Finance ASML ($1B)	Finance Nikon ($2B)	Finance Both ($3B)
Scenario #4.1	ASML	Invest	Invest	Invest	Invest
	Nikon	Invest	Invest	Invest	Invest
	Chipmakers				Optimal First Stage Chipmaker Choice
Scenario #4.2	ASML	Invest	Invest	Invest	Invest
	Nikon	Don't Invest	Don't Invest	Invest	Invest
	Chipmakers				Optimal First Stage Chipmaker Choice
Scenario #4.3	ASML	Invest	Invest	Invest	Invest
	Nikon	Don't Invest	Don't Invest	Invest	Invest
	Chipmakers				Optimal First Stage Chipmaker Choice
Scenario #4.4	ASML	Invest	Invest	Invest	Invest
	Nikon	Don't Invest	Don't Invest	Invest	Don't Invest
	Chipmakers		Optimal First Stage Chipmaker Choice		
Scenario #4.5	ASML	Don't Invest	Don't Invest	Don't Invest	Don't Invest
	Nikon	Don't Invest	Don't Invest	Don't Invest	Don't Invest
	Chipmakers	Optimal First Stage Chipmaker Choice			

4.5.1 Discussion of Base Case EUVL Scenario Equilibria

To foster understanding of the EUVL model, a detailed step-by-step interpretation of only two of the five games will be given here. (Scenario #4.2 in Figure 12 and Scenario #4.4 in Figure 14 have been chosen for their illustrative merit.) Then, a more general comparative analysis of the outcomes across the five games (see Table 4) will be discussed.

Given modeling EUVL investment as a two-stage game where the Chipmaker EUV Backers credibly (i.e., with some level of irreversibility) decide to invest and then the two equipment suppliers choose their actions, backward induction is the appropriate method to ascertain the SPNE. First, notice that ASML has a dominant strategy to invest regardless of the actions of the other two players. (Much more will be said later in this chapter about whether E(NPV) values fully define the basis for each player's decision making process.) This dominant strategy arises because ASML is already far enough along in EUVL development (and selling EUVL equipment is profitable enough relative to the alternative optical lithography solutions) that it is universally in ASML's best interest to push forward with EUV lithography development regardless of the actions of others. (However, recall that ASML will be able to accelerate development and introduce EUVL equipment one year sooner if they do receive chipmaker backer financing.) Next, notice Nikon's best responses:

1. If Nikon gets the large financing amount ($2B) from the chipmakers, it should invest in EUVL.
2. If Nikon does not get the large financing amount ($2B), they should only invest if they believe ASML is not going to invest.

Given those observations about the suppliers' best responses, it is straightforward to determine the NE of the four proper sub-games involving the two suppliers (designated by ovals in Figure 12). Thus, via backward induction, the unique SPNE outcome is for the Chipmaker Backers to finance both suppliers and for both suppliers to subsequently decide to invest. The economic interpretation of this is that if EUV lithography is expected to come to market relatively quickly (as is the case in Scenario #4.2), Chipmakers should help finance ASML because it will pull in EUV introduction timing overall (refer back to Table 3) and they should also help finance Nikon because this will accelerate the overall EUVL ramp and (likely) induce stiffer price competition for EUV equipment once Nikon introduces its EUV tool onto the market. (Although, given the model's assumptions, this later factor is explicitly captured in Scenario #4.1, but not in Scenarios #4.2 through #4.5. See Appendix A for more details.)

Given the numerous historical push-outs in the EUVL introduction mentioned above, the probability of further delays (relative to those in Scenarios #1 and #2) was deemed quite significant. Thus, Scenarios #4.3, #4.4, and #4.5 were also developed with the same set of actions for each player, but with payoff timing (but not the R&D investment timing, which is universally assumed to occur in 2011) delayed according to the EUVL timing schedules indicated in Table 3. For illustrative purposes the results of Scenario #4.4 (Figure 14) will be discussed here and contrasted to the Scenario #4.2 outcome discussed above. Notice that ASML still has a dominant strategy to invest but that Nikon's pattern of best responses has changed relative to Scenario #4.2's pattern. Nikon's best response to 'Finance both' by the Chipmakers and 'Invest' by ASML is now *not* to invest in EUVL. Hence, by backward induction, the optimal choice by the Chipmakers is now to finance *only* ASML. In fact, the 'Finance both' action, which was optimal in Scenario #4.2, would now yield the second lowest payoff (from the

four possible) if the two suppliers always play their best responses. The economic intuition here is that a three-year delay in EUVL introduction, would erase Nikon's incentive to invest their required portion ($2B) to develop an EUVL machine. Hence, a financing contribution of $2B on the part of the Chipmakers toward Nikon would constitute wasted effort.

4.5.2 Base Case Scenario Overall EUVL Model Prediction

The above first-cut, E(NPV)-only analysis indicates that the equilibrium R&D investment outcome could depend on whether the industry players believed the publicly stated roadmap for EUVL (i.e., Scenarios #4.1 and #4.2) or whether they believed a substantial further delay would occur (i.e., Scenarios #4.3 and #4.4). Notice that Table 4 summarizes the SPNE of all five EUVL scenarios (assuming that all 3 players are risk-neutral). In this formulation Scenarios #4.1, #4.2, and #4.3 lead to the Chipmakers financing both suppliers, while Scenario #4.4 leads to Chipmakers financing ASML only. Trivially, Scenario #4.5 leads to the Chipmakers not investing in either supplier. Generally, due to risk-aversion, the approach employed so far of relying directly and solely on E(NPV) as a decision criterion overstates suppliers' willingness to invest and hence Chipmakers' incentives to finance the EUVL R&D at the suppliers. For instance, in this model, even the assumption of moderate (commonly known) risk aversion on the part of Nikon in Scenario #4.3 would cause that scenario's equilibrium to shift to the ('Finance ASML', 'Invest', 'Don't Invest') equilibrium outcome. A more complete approach to incorporating the impact of players' risk aversion will be discussed and analyzed later in this chapter.

As with some other industries, it is not uncommon for semiconductor industry participants to distrust or outright disbelieve published industry roadmaps (see Möllering 2010, pp. 21-22.)

With the numerous slips to the EUV roadmap already (see Clarke 10/10/03; Kimura 9/26/07; Hutcheson 2013), it is quite likely that, at the time of the EUVL modeling in October 2011, the general industry belief (more specifically the beliefs on the part of the large chipmakers and the two lithography equipment suppliers) was that a further push-out of the EUVL introduction was expected. It is widely agreed that collaboration, including proprietary information and realistic schedule sharing, between equipment suppliers and their large chip-making customers during new equipment development has increased during the last few years as Moore's Law has become more difficult to maintain (see Kirk 2012). Hence, if a further push-out to the officially maintained roadmap was believed likely by ASML, it is plausible to think that such a push-out was common knowledge (in the game theoretic sense of the term) among all three players, especially when the prospect of $1B or more of chipmaker support was under consideration. Thus, one could plausibly argue at the timeframes of the initial EUVL modeling (October 2011) that Scenario #4.3 or Scenario #4.4 assume were closer to the commonly-held industry belief than was the timeframe assumed in Scenario #4.1 and Scenario #4.2. In any event, the EUVL timeline which most closely matched the beliefs by the three players would have been expected to drive the decision-making of the Chipmaker EUV Backers. Additionally, subsequent to this initial model development (in October 2011), there were additional reported delays to EUV progress (see Clarke 4/19/12).

4.6 Blended Scenario EUVL Model Definition

Now that the general possibilities and outcomes associated with Scenarios #1 through #5 have been analyzed, I will formalize how views could become a "blended mix" of these five scenarios by introducing the idea of players and interested parties holding (discrete) probability distribution beliefs across the five scenarios. Table 5 below defines four possible such

probability distributions which are likely to approximate many of the viewpoints represented in the industry (at the time of the initial EUVL modeling work in October 2011).

Table 5: Definition of Four Possible Outlooks on EUVL as Probability Weightings Across Scenarios #1 Through #5

	Probability Weightings				
Outlook:	**on Scenario #4.1**	**on Scenario #4.2**	**on Scenario #4.3**	**on Scenario #4.4**	**on Scenario #4.5**
Optimistic	0.3	0.3	0.3	0.05	0.05
Uniform	0.2	0.2	0.2	0.2	0.2
Moderately Pessimistic	0.05	0.05	0.3	0.3	0.3
Very Pessimistic	0	0	0	0.5	0.5

Using the probability weightings shown in Table 5, results in the four "blended" games are shown in Figure 16 through Figure 19 below. For the purposes of analysis, these games are assumed to be ones of complete information, common knowledge, and risk neutrality (recall the general modeling assumptions outlined in Chapter 2). That is, in order for straightforward complete information Nash Equilibrium analysis (outlined below) to apply directly, one must assume that all players share the same beliefs (i.e., the same probability distribution across the five scenarios) and that each player knows that the other players hold the same beliefs as their own. To maintain simplicity of the payoff calculations one must also (at least preliminarily) assume risk neutrality of all three players.

4.7 Blended Scenario Game Trees and Equilibrium Analysis

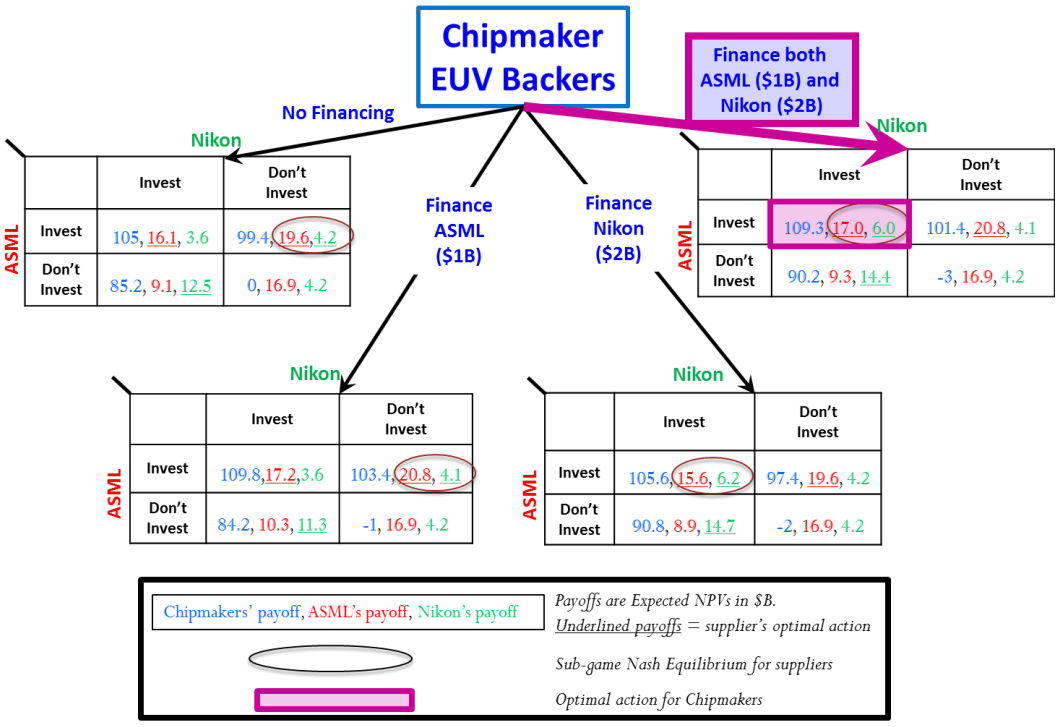


Figure 16: 3-Player Base Case Game 'Optimistic' Weighted Average Across Scenarios #4.1 Through #4.5

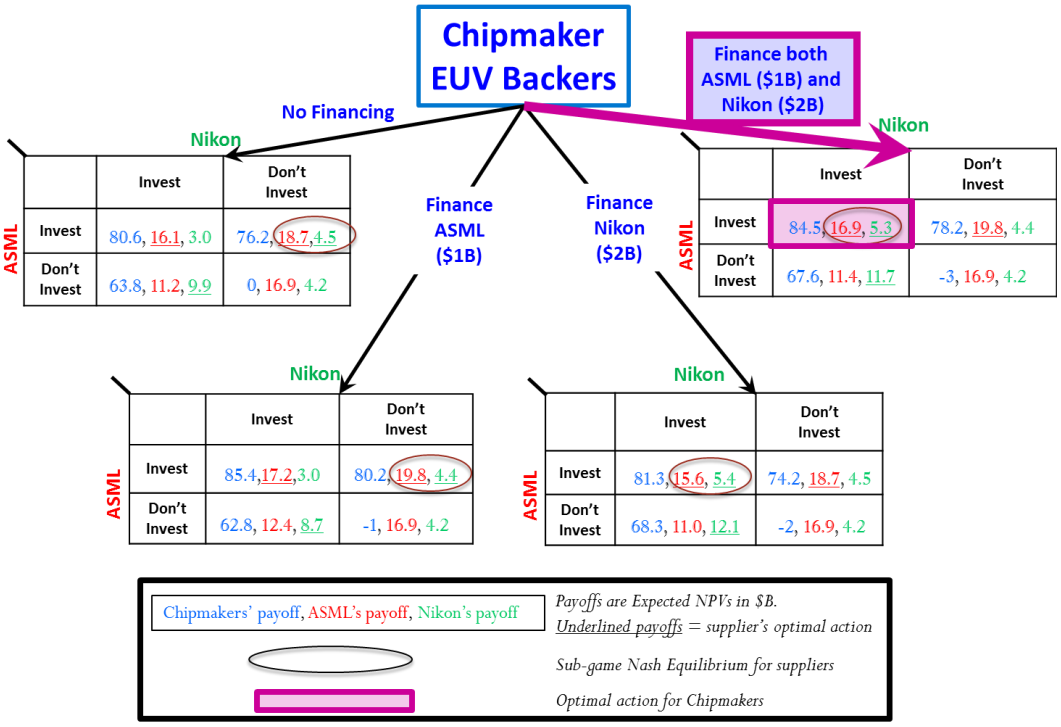


Figure 17: 3-Player Base Case Game 'Uniform' Weighted Average Across Scenarios #4.1 Through #4.5

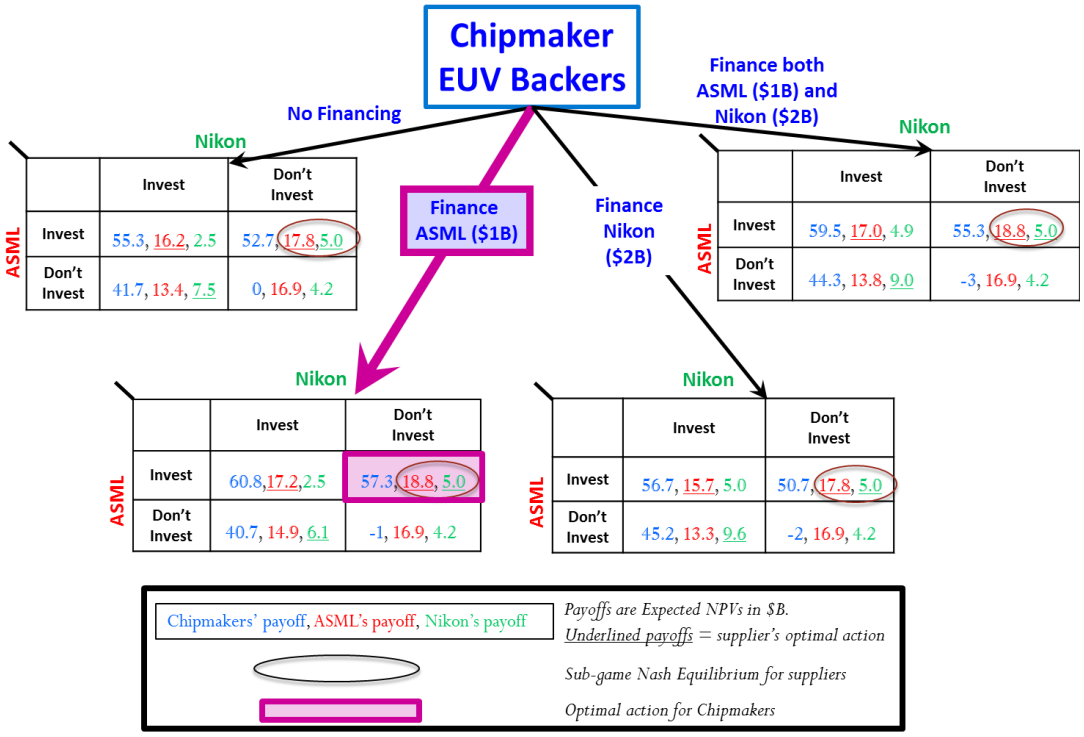


Figure 18: 3-Player Base Case Game 'Moderately Pessimistic' Weighted Average Across Scenarios #4.1 Through #4.5

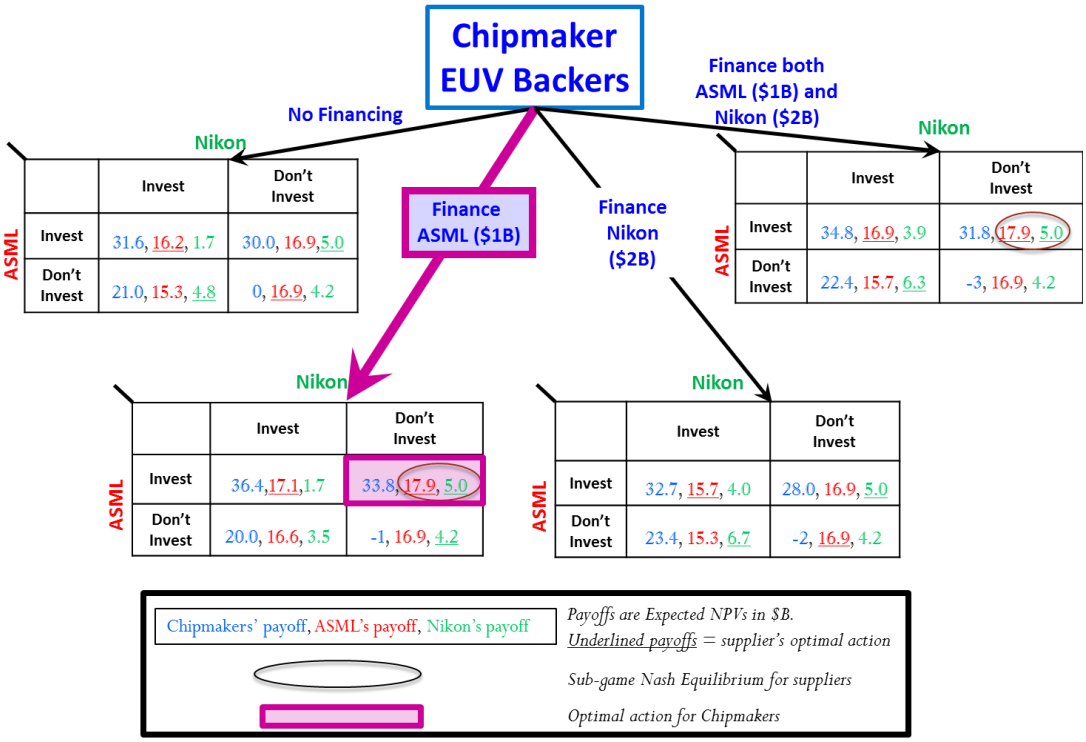


Figure 19: 3-Player Base Case Game 'Very Pessimistic' Weighted Average Across Scenarios #4.1 Through #4.5

4.7.1 Discussion of Blended EUVL Scenario Equilibria

As previously, a summary of the sub-game perfect NE outcomes is shown in Table 6 below. In addition to the SPNE outcomes, this table also contains data which quantifies by how much the E(NPV) of the best response of each player exceeds that of their alternative actions. Specifically, in addition to indicating 'Invest' (shortened to 'I') or 'Don't Invest' (shortened to 'DI') for each supplier, the difference $E(NPV)_{i,\ Invest} - E(NPV)_{i,\ Don't\ Invest}$ (in \$B) and the ratio $\frac{E(NPV)i,Invest}{E(NPV)i,Don't\ Invest}$ (followed by the letter 'r' to signify a dimensionless ratio) are shown in the table as well. Both of these measures give a quantification of how strongly a supplier is incentivized to invest if the E(NPV) difference is positive or, equivalently, if the E(NPV) ratio is greater than one. Also, the measures quantify how much disincentive a supplier should expect from investing if the E(NPV) difference is negative, or, equivalently, if the E(NPV) ratio is less than one.

Table 6: Summary of Base Case SPNE Outcomes for Blended EUVL Outlooks (Including Quantification of the Incentives for Each Player to Play Their SPNE Actions)

		Chipmakers' Actions			
EUVL Outlook Beliefs:		No Financing	Finance ASML ($1B)	Finance Nikon ($2B)	Finance Both ($3B)
Optimistic	ASML	I (+$2.7B; 1.16(r))	I (+$3.9B; 1.23(r))	I (+$6.7B; 1.75(r))	I (+$7.7B; 1.83(r))
	Nikon	DI (-$0.6B; 0.86(r))	DI (-$0.5B; 0.88(r))	I (+$2.0B; 1.48(r))	I (+$1.9B; 1.46(r))
	Chipmakers	$99.4B	$103.4B	$105.6B	$109.3B* (Optimal Choice (+$3.7B))
Uniform	ASML	I (+$1.8B; 1.11(r))	I (+$2.9B; 1.17(r))	I (+$4.6B; 1.47(r))	I (+$5.5B; 1.48(r))
	Nikon	DI (-$1.5B; 0.67(r))	DI (-$1.4B; 0.68(r))	I (+$0.9B; 1.20(r))	I (+$0.9B; 1.20(r))
	Chipmakers	$76.2B	$80.2B	$81.3B	$84.5B* (Optimal Choice (+$3.2B))
Moderately Pessimistic	ASML	I (+$0.9B; 1.05(r))	I (+$1.9B; 1.11(r))	I (+$0.9B; 1.05(r))	I (+$1.9B; 1.11(r))
	Nikon	DI (-$2.5B; 0.5(r))	DI (-$2.5B; 0.5(r))	DI ($0B; 1.00(r))	DI (-$0.1B; 0.98(r))
	Chipmakers	$52.7B	$57.3B* (Optimal Choice (+$2.0B))	$50.7B	$55.3B
Very Pessimistic	ASML	MSNE**. Assumed that none of players invest here.	I (+$1.0B; 1.06(r))	MSNE**. Assumed that none of players invest here.	I (+$1.0B; 1.06(r))
	Nikon		DI (-$3.2B; 0.34(r))		DI (-$0.1B; 0.98(r))
	Chipmakers		$33.8B* (Optimal Choice (+$2B))		$31.8B

* The quantities with asterisks next to them are the Chipmakers E(NPV) in the optimal SPNE. The quantity in parentheses (for the Chipmakers' boxes) represents the increment of E(NPV) for Chipmakers in selecting their optimal (i.e., within-SPNE) choice above the E(NPV) they could receive from their second best choice.

** These two sub-games results in unique mixed-strategy NE (MSNE). Since no pure strategy resulted, I conservatively assumed (based on risk-aversion) that no investment would be made by either supplier in these sub-games, and subsequently that no investment would be made by Chipmaker either.

Quantification of the player's incentives to invest allows the modeler to use judgment regarding the level of risk aversion or other strategic factors to incorporate into one's decision making (and into the predictions about decision making by other players). For example, if the E(NPV) ratio is only marginally greater than one, it is reasonable to assume that the E(NPV) increase is not sufficient to justify the inherent riskiness represented by the investment in EUVL R&D. I have not attempted to quantify firms' risk aversion here, as others have done elsewhere. (Clearly, if one feels confident in such quantification of risk-aversion, these estimates could be used to modify the players' payoffs within the EUVL model.) Thus, I have largely assumed here that

deviations from risk neutrality are considered part of the holistic managerial judgment which must go into any strategic R&D decision making process. Analogously to the case of pure Scenario #4.3, even a moderate amount of risk aversion on the part of Nikon would shift the equilibrium outcome in the 'Uniform' blended scenario to the ('Finance ASML', 'Invest', 'Don't Invest') equilibrium outcome.

One clear observation from the blended games is that as the prospects for EUVL become more bleak (i.e., more delayed), the incentives for equipment suppliers become weaker, as do the incentives for Chipmakers to provide financing help. If one imposes a commonly known required E(NPV) ratio (e.g., 1.25 or 1.5), the "modified Nash Equilibrium" of the game could change significantly toward less investment in EUVL (this can be seen directly from the ratios shown in Table 6).

Closer scrutiny of Figure 16 through Figure 19 and Table 6 reveal several key features. According to the unalloyed E(NPV) decision criterion represented by these figures, ASML has an "virtually dominant" strategy to invest in EUVL (the only *marginal* exceptions coming in the very pessimistic outlook case). However, ASML's E(NPV) incentives to invest in EUVL are quite muted when receiving no financing from the Chipmakers (e.g., see that the E(NPV) ratio ranges from only 1.05 to 1.11 in the uniform and moderately pessimistic cases). It is interesting to note that ASML's incentive to invest improves significantly when financing is provided by the Chipmakers. Even so, in this case, ASML does not obtain an overwhelming incentive to invest. The economic explanation here is that, for ASML, existing DP/MP 193i patterning is roughly comparable in profitability to EUVL in the later modeling years (2016-2021) assuming ASML can maintain its large (~80%) market share in DP/MP 193i lithography. This result is consistent with the general sense that the large chipmakers have a greater urgency about the timing of

EUVL introduction than does ASML (McGrath 7/11/12). It also highlights (and allows quantification of) one strategy large chipmakers should keep in mind: if they support Nikon's health in the DP/MP 193i optical lithography equipment market, they also indirectly increase ASML's incentive to develop EUVL more quickly.

4.7.2 Overall Prediction of the EUVL Model

Given the model equilibria analysis above, the overall prediction of the model is that Chipmakers will finance EUV at ASML (by approximately $1B), but not finance EUV at Nikon. Subsequently, ASML will invest heavily in EUV technology, but Nikon will not.

The Nash Equilibrium outcome ('Finance both', 'Invest', 'Invest') seen in some of the EUV lithography scenarios analyzed relies on too many tenuous assumptions to be a viable game outcome prediction. Specifically, as discussed previously, it relies on an overly optimistic view about the EUVL introduction timeline and on a high degree of risk neutrality on the part of Nikon. In addition, because the incremental E(NPV) of the Chipmakers of financing Nikon is only marginally higher in this future state of the world, it relies on risk-neutrality of the Chipmakers and avoidance of large inter-chipmaker coordination costs in this more complex R&D financing situation.

4.8 Subsequent 2012 Industry Events Consistent with EUVL Model Prediction

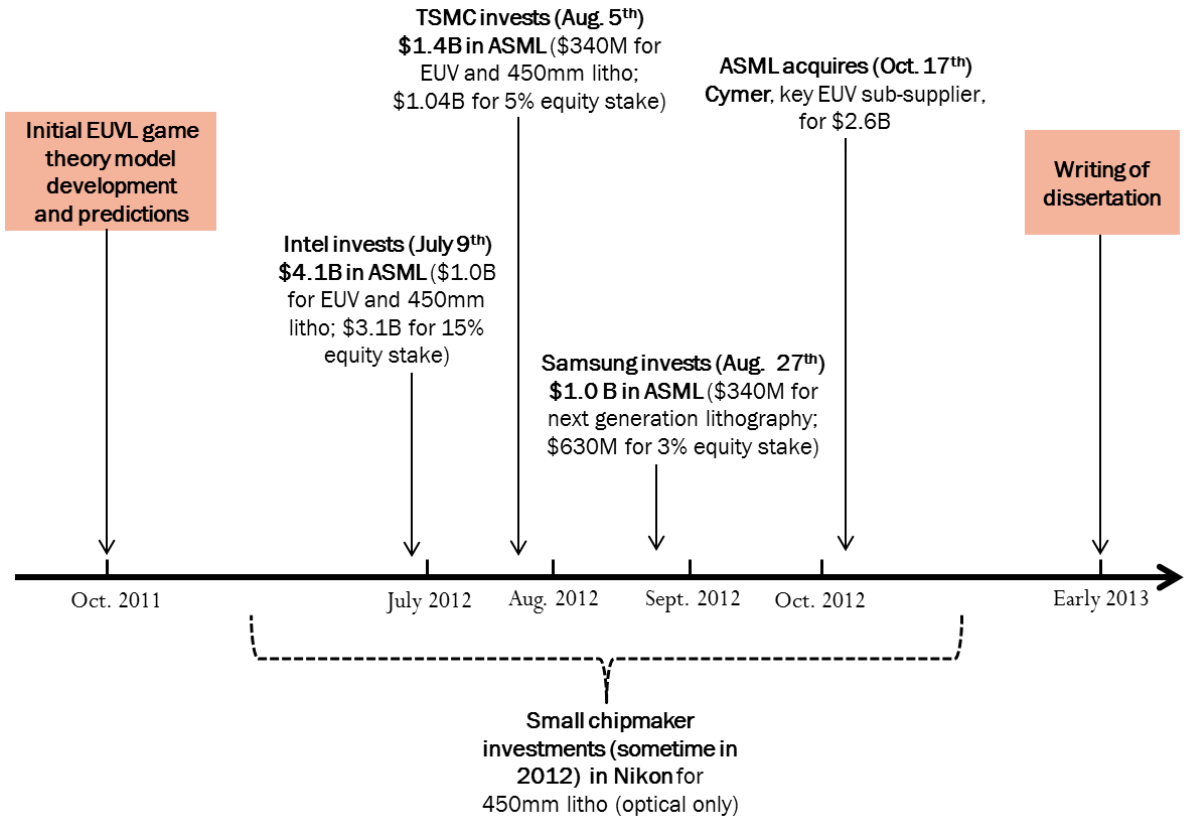


Figure 20: Timeline of Five Industry Events Consistent with EUVL Game Theory Model Predictions

Subsequent to the EUVL model development in late 2011, a series of five industry financing events occurred in 2012 (see Figure 20) which provided evidence solidly consistent with the EUVL model prediction just described. Below we will discuss those five events in detail, starting with three extremely large, successive investments by Intel, TSMC, and Samsung in lead lithography supplier ASML.

4.8.1 Intel, TSMC, and Samsung invest in ASML

In July and August of 2012, a series of three large, distinct investments in ASML by the three largest chip manufacturers (Intel, TSMC, and Samsung) were undertaken totaling approximately

$6.5B (McGrath 7/9/12; Clarke 8/6/12; McGrath 8/27/12). The EE Times (Electronic Engineering Times) named this series of three investments one of the "top 10" business deals in the overall electronics industry in 2012 (Clarke 12/5/2012).

These real-world investments provide evidence consistent with the model predictions (based on the sub-game perfect Nash Equilibria) seen in Scenarios #4.1 through #4.4 (Figure 11 through Figure ***15***) and all four of the blended scenarios (Figure 16 through Figure ***19***). In all eight of these games, the SPNE outcome involves Chipmakers helping finance ASML's EUVL R&D effort by approximately $1B (recall that in some of the scenarios, the SPNE's additionally suggest the possibility of a larger $2B investment in EUVL development at Nikon as well). The magnitude, timing, and composition of these three distinct chipmaker investments is shown in Table 7 below.

Table 7: Investments in ASML by three largest chip manufacturers (July 2012-Aug 2012)

Company Investing:	**Investment Date**	**R&D investment in ASML**	**Non-voting Equity in ASML**	**Total Investment Amount in ASML**	**Data Source**
Intel	July 9th, 2012	$1.0B total ($340M for EUVL; $680M for 450mm litho)	$3.1B (15% stake)	$4.1B	McGrath 7/9/12; ASML 7/9/12
TSMC	August 5th, 2012	$340M for EUVL and 450mm litho (breakdown not specified)	$1.04B (5% stake)	$1.4B	Clarke 8/6/12; ASML 8/5/12
Samsung	August 27th, 2012	$340M for "Next generation lithography" (which includes EUVL)	$630M (3% stake)	$1.0B	McGrath 8/27/12; ASML 8/27/12

It is worth examining the composition of this series of large investments because it sheds some light on the correspondence of the variants of the EUV R&D models presented above to the economic reality which has subsequently unfolded in the industry. As is apparent from Table 7, the investments involved the acquisition of significant equity stakes in ASML by each of Intel, Samsung, and TSMC. The three distinct investments were made as part of a "customer co-investment program" offered by ASML through which large chipmaker equity investments in ASML were coupled with direct contributions to the R&D programs for EUVL and 450mm capable lithography equipment at ASML (see ASML 7/9/12).

The ASML customer co-investment program consisted of two stages. In the first, only the three largest customers of ASML (Intel, Samsung, and TSMC) were given the option to acquire non-voting ownership of up to 25% of ASML (with an additional linked amount of R&D investment in ASML's lithography research programs as well). If the three largest customers had not participated to the high degree they did in the first stage (i.e., acquiring 23% of the 25% on offer), then similar options to participate would have likely been extended to other chipmakers in a second stage of co-investment offers (Clarke 8/6/12). This co-investment mechanism seems to have ultimately worked as intended, as all three large chipmakers invested heavily. However, as stated earlier, the intent of the EUV game theory models described above was *not* to predict which particular type of mechanism(s) would be used to achieve inter-chipmaker coordination. The intent was a higher level prediction about chipmakers' financing actions as a whole and the corresponding investment actions of the two viable lithography equipment suppliers.

In addition to the fundamental match of the chipmakers' investments in ASML to the SPNE outcome from the EUVL model, other key observations from these three investments include:

- *Approximate match of the aggregate Chipmaker EUV Backer R&D contribution for EUVL to the estimate derived in the modeling process* (see Section 4.2 above and Appendix A for details). Although the total chipmaker R&D contribution was ~$1.7B USD, the contribution specifically for EUVL research was ~$1B USD (assuming that the lion's share of TSMC's and Samsung's R&D investments were intended for EUVL), matching the EUVL modeling estimate.
- *Asymmetry of investment magnitudes among the three largest chipmakers* (with Intel providing the largest investment). Such asymmetry has been common in chipmaker financing of semiconductor equipment R&D in the past. For example, Sematech (whose early charter became pre-competitively strengthening U.S.-based semiconductor equipment offerings) set their annual chipmakers dues proportional to firm semiconductor revenue, making their contributions asymmetrically sized (see Browning and Shetler 2000, pp. 35). Additionally, early EUV development funding efforts in the late 1990s included asymmetric chipmaker investments, with Intel contributing the largest share of investment (Linden et al. 2000, pp. 102).
- *The order of the investments in ASML* was first Intel (July 9th, 2012), then TSMC (August 5th, 2012), and then Samsung (August 27th, 2012). Although this order of investment might have been expected based on corporate public announcements and prior behavior patterns of the three chipmakers involved, these predictions do not stem from the EUVL models above because the models assume one amalgamated chipmaker entity without directly considering *which* chipmakers are incented to invest or any details regarding mechanisms of the financing. Intel played an R&D investment leadership role in the early development of EUVL in the late 1990s (see Linden et al., 2000, pp. 102).

Conversely, Samsung is historically known for its strong tendency to engage in "fast following" behavior (more will be said about this in Section 6.5.1). Further exploration of such investment timing phenomena would require the theoretical and/or empirical study of equilibrium attainment mechanisms for firm R&D decisions, a topic ripe for future work, but not the focus of the EUVL model developed here.

- *Lower likelihood of large future investments in Nikon's EUVL effort* due to the fact that the three chipmakers took large equity stakes in ASML. Although it is still possible for the chipmakers to make large investments in Nikon's EUVL effort, the fact that they took a combined 23% equity stake in ASML is highly suggestive that they are putting their weight firmly behind ASML's EUVL effort.

Recall that some of the more optimistic scenarios analyzed in the EUVL model have SPNEs in which the Chipmakers finance Nikon's EUVL effort as well, but in these equilibria Nikon attained relatively modest E(NPV) benefits which means that it was not likely to be induced, by the $2B assumed from chipmakers, to invest their resources robustly in EUVL development (assuming just a moderate level of Nikon risk-aversion). Additionally, Nikon had at times voiced its belief that the publicly announced EUVL roadmaps were overly optimistic (e.g., see Lapedus, 2/22/10) noting specific concerns regarding the readiness of EUVL "ecosystem" developments (including EUVL masks and metrology tools). Although this could be dismissed as mere business posturing on the part of Nikon (i.e., convincing investors of the correctness of its purposeful slow-pedaling of EUVL R&D funding and persuading chipmakers that any effort to help support Nikon's EUVL effort should be large in financial magnitude), it does lend some credence to the idea that Nikon holds a relatively pessimistic viewpoint regarding

EUVL's introduction timeline. As was seen in Table 4 and Table ***6***, the more pessimistic view a player adopts, the lower its economic incentive to invest heavily in EUVL.

- *Some "co-mingling" of chipmaker EUVL equipment investments and 450mm lithography investments* (not surprising given that ASML and Nikon are also crucial actors for the 450mm wafer equipment development roadmap). However, this co-mingling fundamentally does not contradict the EUVL modeling analysis performed here.

In summary, the three investments by Intel, Samsung, and TSMC provide evidence consistent with the SPNE equilibria outcomes in which the Chipmakers invest heavily in EUVL development for ASML only. Subsequent to these ASML customer co-investment deal announcements, there were two other industry financing events which provide strong additional evidence supporting the strongest SPNE prediction from the EUVL model: (Chipmakers: 'Finance ASML', ASML: 'Invest', Nikon: 'Don't Invest'): 1) ASML acquired key EUVL sub-supplier Cymer and 2) one or more chipmakers made small investments in Nikon in 2012 to help develop 450mm *optical (193i)* lithography equipment. These two industry occurrences indicate that ASML is accelerating its investments in EUVL, Chipmakers are focusing their financing on helping Nikon bolster its optical lithography vitality, and Nikon is focusing the bulk of its investment efforts in optical lithography as well.

4.8.2 ASML acquires critical EUVL supplier Cymer

On October 17th, 2012, ASML announced its intention to purchase lithography component supplier Cymer for $2.6B (Lapedus, 10/17/12). Cymer makes one of the most crucial components for EUV lithography equipment (the light source for the incident EUV radiation) and the merger was meant to speed up the market introduction of EUV technology. It is widely

recognized that the light source for EUVL technology represents one the largest, if not the largest, technical bottleneck for commercial introduction of EUVL (e.g., see Bakshi, 2011). According to the ASML press-release:

> "The purpose of the acquisition of Cymer is to accelerate the development of Extreme Ultraviolet (EUV) semiconductor lithography technology…. ASML and Cymer have collaborated closely for over a year, and this merger is the natural evolution of their existing cooperation in developing EUV technology. Combining Cymer's expertise in EUV light sources with ASML's expertise in lithography systems design and integration will reduce the risk and accelerate the introduction of this extremely complex technology." (ASML, 10/17/12)

Thus, this announced acquisition represents clear evidence that ASML is very aggressively investing in EUVL after the three large chipmaker investments in ASML in July and August of 2012. This is consistent with ASML's choosing to 'Invest' in EUVL R&D, one component of the EUVL model SPNE outcome prediction.

4.8.3 Chipmakers Invest in Nikon's 450mm Optical Lithography Development

In 2012 there were strong indications in the press of moderately-sized investments by one or more chipmakers for 450mm optical lithography development at Nikon. Although no press release was issued, an Intel executive mentioned small Intel investments in "ASML's competitor" for 450mm lithography (presumably for 193i *optical* lithography) in 2012 (Intel, 7/9/12). The most likely candidate for "ASML's competitor" here is Nikon given that it is the only lithography supplier beside ASML with significant market share in leading edge lithography equipment (see EE Times 4/1/12).

Additionally, although unsubstantiated by any press announcements by Intel or Nikon, a number of trade press articles indicated that Intel had made a small 450mm optical lithography investment in Nikon (Semicondportal 8/8/12; EE Times 8/7/12; Japan Times 8/10/12). These sources do not prove conclusively that Intel was the source of this funding, but an executive at Nikon reported to the press that "We are receiving financial support for the development." (Japan Times 8/10/12) and another indicated Nikon was involved with a 450mm joint development effort with a chipmaker (SEMI 12/6/12). Thus it is clear that Nikon is receiving some financing for 450mm optical lithography from one or more chipmakers.

Such optical lithography equipment will certainly be required in significant volumes to enable 450mm wafer production (see SEMI 12/6/12). Moderate chipmaker financing of Nikon's optical lithography development helps further substantiate the prediction of the EUVL model analysis, since it strongly suggests that the Chipmakers are not spending their R&D financing dollars on Nikon's EUVL development (and hence that the Chipmakers are choosing 'Finance ASML' instead of 'Finance both'). It is also strongly suggests that Nikon is spending its R&D dollars more on smoothly porting current (193i) optical lithography equipment to the upcoming 450mm diameter wafer size, and not on EUVL (and thus provides some evidence that Nikon is choosing 'Don't Invest', consistent with the EUVL model prediction).

In summary, the five 2012 lithography investments discussed above are quite consistent with the prediction from the EUVL model presented above that a subset of the large chipmakers would align their EUVL support (including significant R&D funding of approximately $1B USD) behind the lithography market leader, ASML. Taken in total, these market events are also highly suggestive that the Chipmakers were not planning (at the time of their large ASML investments)

to invest heavily in supporting Nikon's EUVL program. Finally, the events provide evidence that ASML is aggressively pursuing EUVL development, while Nikon is not.

4.9 Robustness of EUVL Model Predictions to Game Reformulation

Now that we have outlined the EUVL model structure, payoff estimation, NE predictions, and subsequent confirmatory evidence, let us explore the robustness of the payoffs and NE predictions to alternate assumptions. One easy and relevant robustness check is to examine the impact of reformulating the five scenarios of the EUVL game discussed above as simultaneous games (instead of two-stage sequential games). This is a reasonable check to perform because the modeling effort described above has abstracted substantially away from the continuous time nature of the (actual) business game being played; multiple small investment and technology decisions are in fact being made over time by all three players simultaneously. In some sense, the two-stage EUVL game examined so far and the reformulated simultaneous EUVL game can be thought of as "brackets" which likely enclose the complex economic reality of this technology transition. Another relevant factor lending additional plausibility to the simultaneous game interpretation is that fact that the financial and human resources invested into EUVL development by the equipment suppliers is not completely observable by the Chipmakers.

Table 8 below summarizes the results of this simultaneous game robustness check. In a number of cases (italicized in the table) the corresponding Nash Equilibrium under the simultaneous game re-interpretation changes to ('Finance ASML', 'Invest', 'Don't Invest'). Thus, to the extent that one believes that the simultaneous game model represents reality, this robustness check provides even more evidence for the Chipmakers' investment in ASML and casts even more doubt on the prudence of investment in Nikon's EUVL effort by the Chipmakers.

Table 8: Summary of NE Outcomes for Both 2-Stage and 1-Stage Formulations

	Sequential 2-stage game equilibrium outcome*:	**Reformulated Simultaneous 1-stage game equilibrium outcome*:**
Scenario #4.1	(Finance Both, I, I)	(Finance Both, I, I)
Scenario #4.2	(Finance Both, I, I)	*(Finance ASML, I, DI)*
Scenario #4.3	(Finance Both, I, I)**	*(Finance ASML, I, DI)*
Scenario #4.4	(Finance ASML, I, DI)	(Finance ASML, I, DI)
Scenario #4.5	(No Financing, DI, DI)	(No Financing, DI, DI)
Optimistic Outlook	(Finance Both, I, I)	*(Finance ASML, I, DI)*
Uniform Outlook	(Finance Both, I, I)**	*(Finance ASML, I, DI)*
Moderately Pessimistic Outlook	(Finance ASML, I, DI)	(Finance ASML, I, DI)
Very Pessimistic Outlook	(Finance ASML, I, DI)	(Finance ASML, I, DI)

* Action triplet order is (<Chipmakers action>, <ASML action>, <Nikon action>). I = 'Invest', DI = 'Don't Invest'.

** Recall the discussions earlier that even a moderate amount of (commonly known) Nikon risk aversion would toggle the game to the (Finance ASML, I, DI) equilibrium outcome in these two scenarios.

4.10 Parameter Sensitivity Analysis for EUVL Model

Now, let us proceed to a detailed sensitivity analysis of the E(NPV) values and SPNE to the model parameters. Table 9 below shows educated guesses of possible values of key model input parameters which are higher and lower than the base case parameter values.

Table 9: Low, Base Case, and High Values for Critical EUVL Model Parameters

Low, **Base Case**, High	**EUVL Model parameter**	**Parameter description**
$1B, **$2B**, $5B	$I_{TOTAL, ASML}$	Additional non-recurring engineering (i.e., R&D) costs remaining for ASML's EUVL project completion in October 2011
$2B, **$4B**, $7B	$I_{TOTAL, Nikon}$	Additional non-recurring engineering (i.e., R&D) costs remaining for Nikon's EUVL project completion in October 2011
6%, **10%**, 14%	g_{wafer}	Wafer Demand Compound Annual Growth Rate (CAGR), 2011-2021, assuming EUVL is ultimately developed
-5%, **0%**, 8%	$\mathbf{g_{wafer, no\ EUV}}$	Annual Growth Rate in Demand for 300mm Wafer Starts (starting in 2016 if no EUVL is developed)
6%, **12%**, 18%	$g_{critical\ layers}$	Annual growth rate of average number of critical layers/wafer
-5%, **5%**, 15%	$g_{EUV\ cost}$	Annual growth of EUVL patterning cost/wafer)
5%, **10%**, 15%	$g_{cost\ ratio}$	Annual growth rate of RATIO of DP/MP patterning costs to EUVL patterning --from 2011-2021
10%, **15%**, 20%	$m_{net, DP/MP}$	Average Net Margin of Lithography Equipment Suppliers on DP/MP products/services
15%, **20%**, 25%	$m_{net, EUV}$	Average Net Margin of Lithography Equipment Suppliers on EUVL products/services
30%, **50%**, 70%	$f_{financing}$	Fraction of remaining required financing which "Chipmaker EUV Backers" must provide to ASML and/or Nikon in order to significantly accelerate their EUVL development efforts
30%, **50%**, 70%	$f_{leading\ edge}$	Fraction of wafer starts which are "Leading Edge" (i.e., which require DP/MP or EUV lithography technology for patterning)
20%, **33%**, 50%	$f_{sr, DP/MP}$	Fraction of overall DP/MP patterning cost which corresponds to equipment and services purchases from the lithography suppliers
50%, **68%**, 80%	$f_{sr, EUV}$	Fraction of overall EUV patterning cost which corresponds to equipment and services purchases from the lithography suppliers
30%, **50%**, 70%	$f_{chipmaker\ profit}$	Fraction of chipmaker manufacturing cost savings (from the introduction of EUVL) which are converted to net Chipmaker profits
12%, **15%**, 18%	= 1/δ-1 (where δ is the discount factor)	Discount Rate

The E(NPV) sensitivity of the Chipmakers (Figure 21*: Sensitivity of the Chipmakers' E(NPV) to Model Input Parameter Changes Shown in* below), ASML (Figure 22 below), and Nikon (Figure 23 below) are calculated using the high and low values from Table 9. It should be emphasized that these sensitivity analyses are the results of "one at a time" parameter changes, and, additionally, they assume that no changes occur regarding the strategies of the three strategic players in the EUVL game. (i.e., these figures do not account for possible shifts of the NE resulting from introducing the low or high model parameter values being analyzed.) The figures are only meant to provide a general sense of how impactful model parameters are to the E(NPV)s in several relevant future states of the world.

One key background point is necessary to understand the values in Figure 21. It may seem counterintuitive that as lithography costs go up, the Chipmakers' E(NPV) goes up. However, to resolve this apparent conundrum, it is important to understand that I am defining Chipmakers' E(NPV) in each of the five scenarios in Table 3 to be a relative E(NPV), not an absolute E(NPV) of Chipmakers' expected profit. More specifically, I have defined the Chipmakers' E(NPV) as relative to the status quo state of the world in which no investments are made by any player given the assumed model input parameters (see Appendix A for a specific mathematical formalization of this assumption). Thus in Figure 21, and in fact in Figure 11 through Figure ***19*** as well, the E(NPV) values must be thought of as the impact to the Chipmakers of ASML investing in EUVL, not as an expected value of overall Chipmaker profits under a given future state of the world. With this clarification in mind, the relative E(NPV) for the Chipmakers will rise as the lithography cost growth model parameters increase.

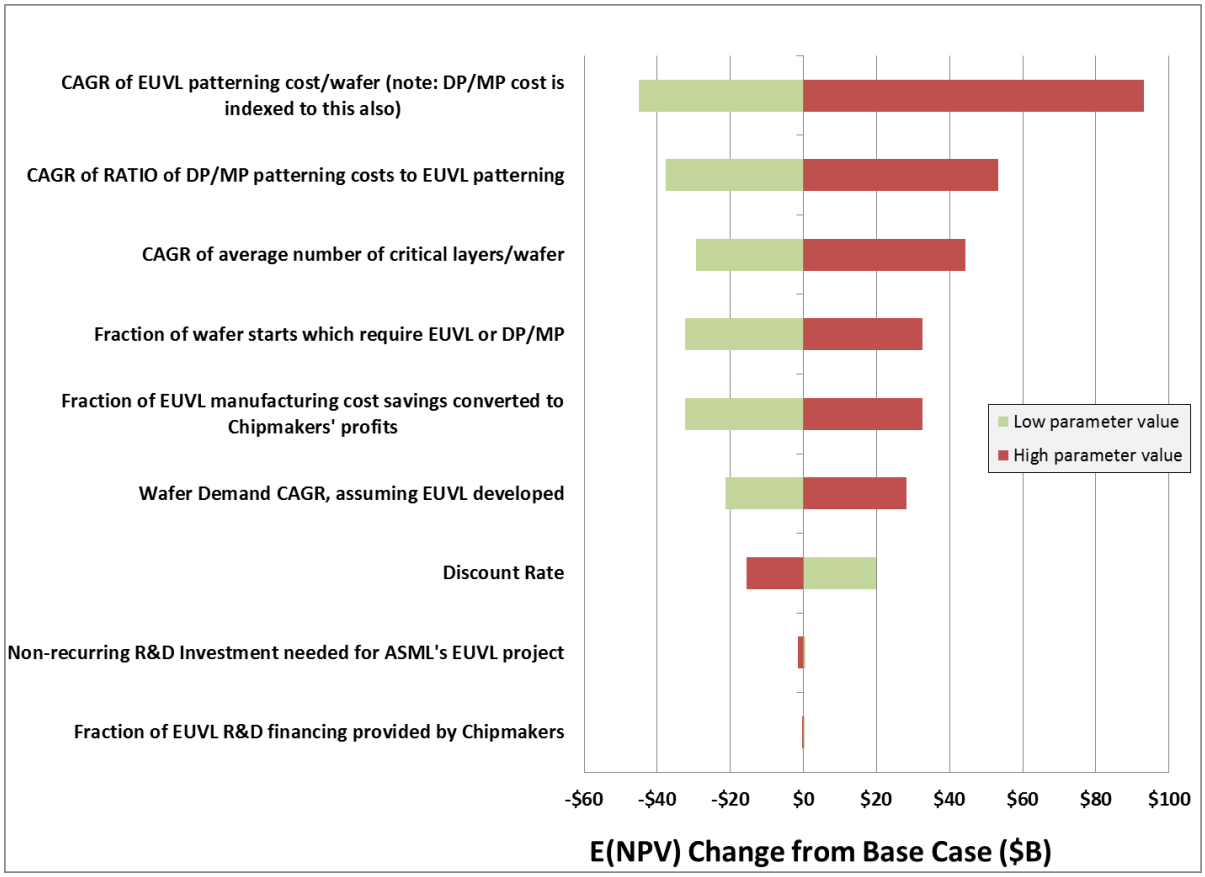


Figure 21: Sensitivity of the Chipmakers' E(NPV) to Model Input Parameter Changes Shown in Table 9

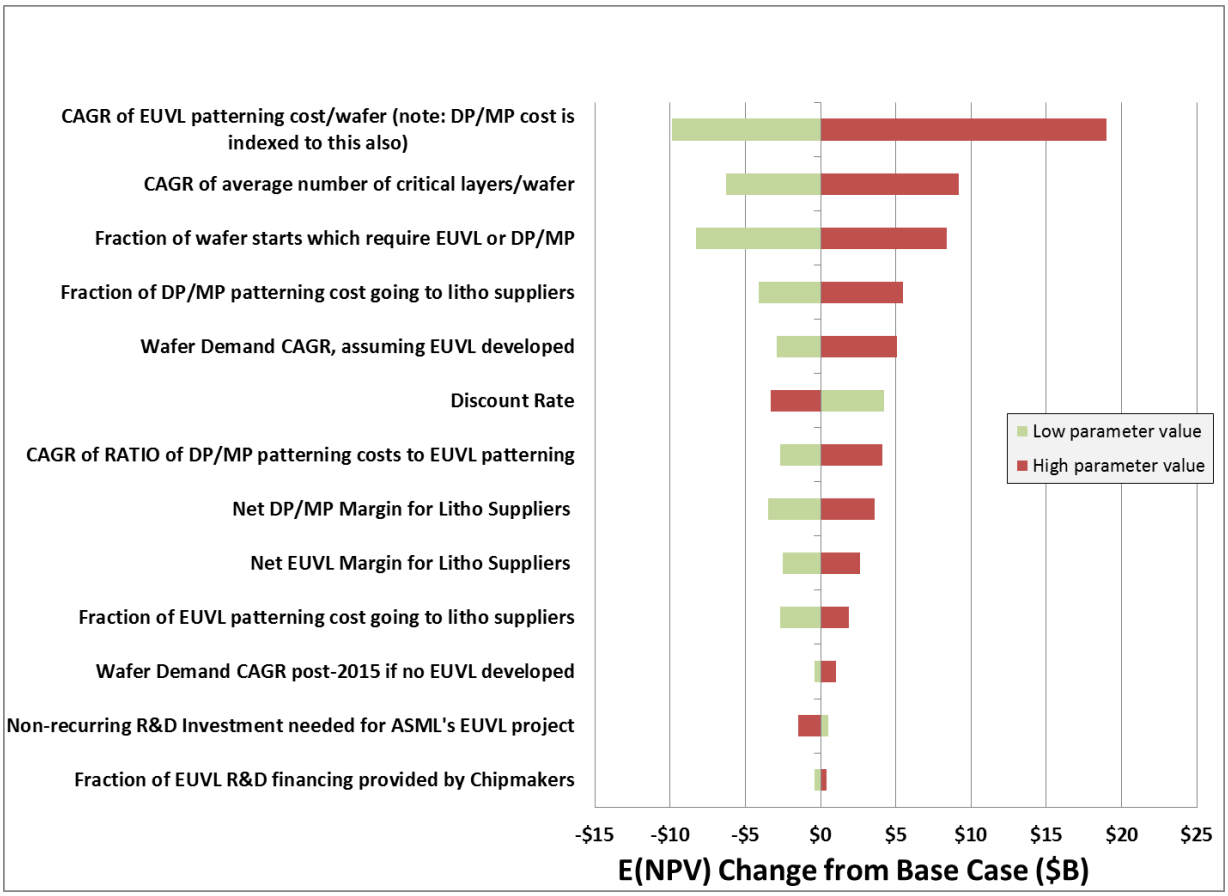


Figure 22: Sensitivity of ASML's E(NPV) to Model Input Parameter Changes Shown in Table 9

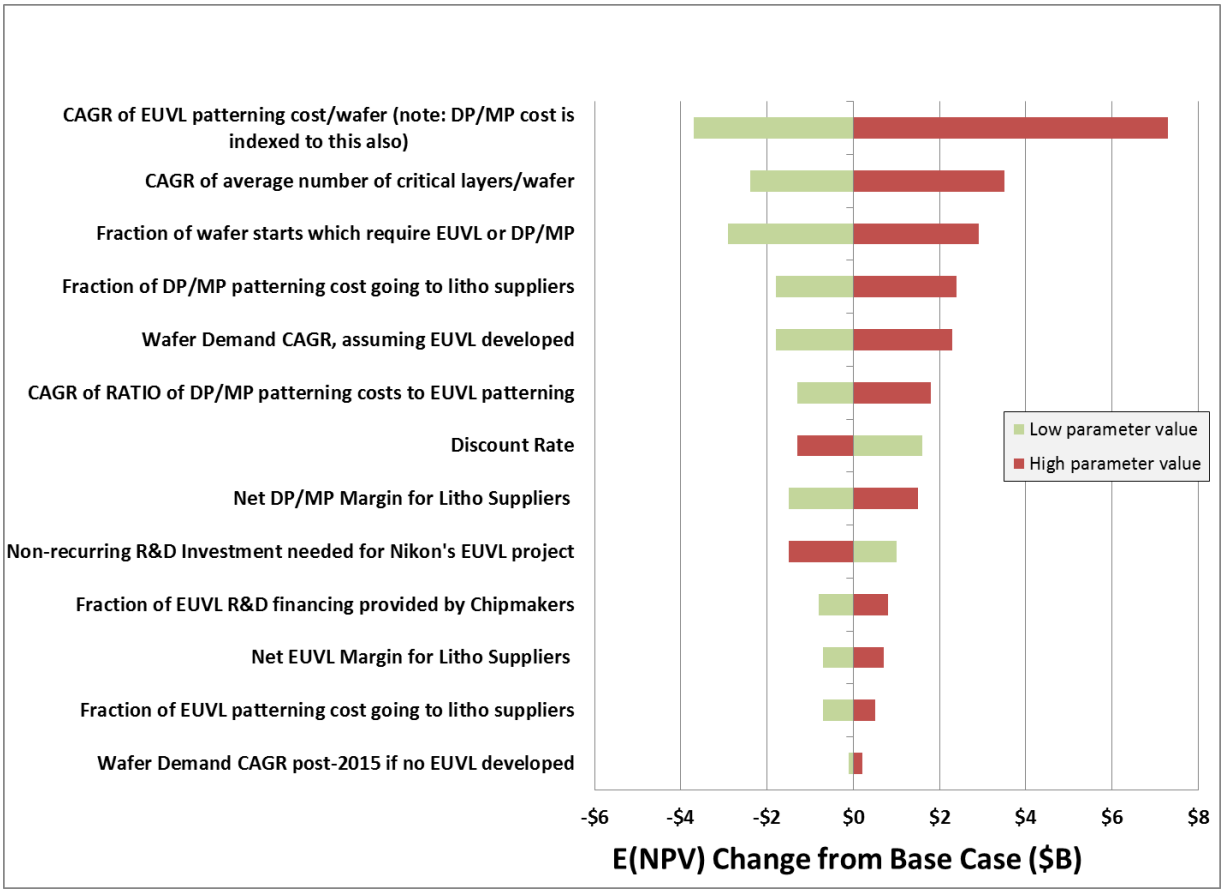


Figure 23: Sensitivity of Nikon's E(NPV) to Model Input Parameter Changes Shown in Table 9

The parameters being changed in Figure 21 through Figure 23 are ranked from highest to lowest E(NPV) impact. Clearly, these rankings should not be viewed as absolute orders of importance of parameters because the magnitude of the E(NPV) changes shown is directly a function of the low and high parameter values chosen in Table 9. However, these rankings give a general sense of which parameters have the largest impacts on the E(NPV) of each of the three players. Since the base case analysis (Section 4.5) strongly suggested the SPNE outcome of 'Finance ASML' by the Chipmakers and subsequently 'Invest' by ASML and 'Don't Invest' by Nikon, this is one natural reference point for the sensitivity analyses presented above. Using this SPNE state of the world as a reference point yielded clear and meaningful sensitivity results for the Chipmakers

and ASML (Figure 21 and Figure 22), but did not yield fully instructive results for Nikon (i.e., when Nikon does not invest in EUVL and they maintain 20% critical patterning market share [via optical DP/MP], given the simplifying assumptions of this model, there is no change in Nikon's E(NPV) to many of the EUVL-centric parameter changes evaluated [Table 9]). Thus, in order to provide more instructive parameter sensitivity analysis for Nikon's E(NPV), the base case E(NPV) reference point for Figure 23 was chosen to be the state of the world corresponding to ('Finance Both', 'Invest', 'Invest'). Otherwise, Nikon's E(NPV) sensitivity was calculated in the same fashion as for the Chipmakers and ASML.

Here are some general take-aways from the sensitivity analysis results in Figure 21 through Figure 23:

- Certain parameters can swing the E(NPV) tremendously. Hence, estimating these parameters well is crucial. In a number of instances changes to the SPNE of the games can be induced by parameter changes as well (these shifts are analyzed further later in this chapter).
- The EUVL patterning cost per wafer CAGR is the top influencing factor in each of the three analyses (Figure 21 through Figure 23). To some extent this is driven by the fact that a frozen ratio of DP/MP 193i patterning cost to EUVL patterning cost is assumed in each year. (If interested, see Equations (A.20) through (A.22) in Appendix A.) Hence, when the EUVL patterning cost CAGR is changed it directly influences the Chipmaker costs and supplier revenues for *both* EUVL patterning and 193i DP/MP patterning. In this sense, this parameter should be thought of as an overall *critical layer* patterning cost per wafer CAGR instead of just an EUVL patterning cost per wafer CAGR.

- In contrast, the "DP/MP to EUV cost per wafer ratio CAGR" factor *only* impacts the DP/MP patterning costs – not the EUVL patterning costs. It is interesting to note that this factor ranks second in importance for Chipmakers but only sixth or seventh in importance for the two suppliers. This is consistent with the fact noted earlier that the lithography suppliers will make substantial profits supplying either lithography technology (subject to competitive pressures) while the Chipmakers' costs will go up dramatically if DP/MP optical lithography costs go up.
- The non-recurring engineering cost (for EUVL R&D) is at the bottom of the influential parameters list for the Chipmakers' and ASML's E(NPV) but is ranked significantly higher in terms of impact on Nikon's E(NPV). This is a reflection of the fact that Nikon's required R&D investment amount for EUVL is not only absolutely higher than ASML's, but it is quite substantial when compared to the smaller benefits Nikon could expect to gain from developing EUVL (because they would be expected to have a later start and a smaller market share in EUVL).
- The discount rate has a measureable impact for all three players but is near the bottom of the parameter sensitivity list for the Chipmakers and near the middle for both suppliers. This implies that discount rate (at least in the range examined, 12%-18%) is less likely to influence players' decisions than a number of the other physically-based parameters in the model.

Now that the E(NPV) impact of higher and lower parameter values has been explored in detail, let us examine (again, in a one-at-a-time fashion) the parameter cutoff values which correspond to changes from the sub-game NE in the EUVL game. First, I analyze ASML's choice to invest (given that Chipmakers play 'Finance ASML' and Nikon plays 'Don't Invest'), with results

shown in Table 10. After that, I analyze Nikon's choice to invest (given that Chipmakers 'Finance both' and ASML 'Invests') with results shown in Table 11. To allow for risk-aversion on the part of each supplier, cutoff values for the E(NPV) ratio of 1.0 (i.e., unalloyed reliance on E(NPV)), 1.1, 1.25, and 1.5 are tabulated. Within the context of this thesis, the reader is invited to use his or her own judgment to decide how risk averse the suppliers are likely to be.

Table 10: Parameter Values Cross-Overs for ASML's Decision to Invest in EUVL Technology (Assumes: Chipmakers' 'Finance ASML' and Nikon 'Doesn't Invest' and 'Uniform' EUVL Outlook)

		$\frac{E(NPV)_{ASML,Invest}}{E(NPV)_{ASML,Don't\ Invest}}$ values which are:			
Low/ Base/ High	**EUVL parameters**	**> 1.5**	**> 1.25**	**> 1.1**	**>1**
6%, **10%**, 14%	g_{wafer}: Wafer Demand CAGR, 2011-2021, assuming EUVL is ultimately developed	>14.9%	>11.3%	>8.7%	>6.8%
-5%, **0%**, 8%	$g_{wafer,\ no\ EUV}$: Annual Growth Rate in Demand for 300mm Wafer Starts (starting in 2016 if no EUVL is developed)	<-10.5%	<-2.7%	<2.6%	<6.6%
6%, **12%**, 18%	$g_{critical\ layers}$: Annual growth rate of average number of critical layers/wafer	No such parameter values	>33.2%	>2.1%	>-7.2%
-5%, **5%**, 15%	$g_{EUV\ cost}$: Annual growth of EUVL patterning cost/wafer)	No such parameter values	>24.9%	>4.2%	>-13.0%
5%, **10%**, 15%	$g_{cost\ ratio}$: Annual growth rate of *RATIO* of DP/MP patterning costs to EUVL patterning --from 2011-2021	<5.6%	<8.8%	<11.2%	<13.0%
10%, **15%**, 20%	$m_{net,\ DP/MP}$: Average Net Margin of Lithography Equipment Suppliers on DP/MP products/services	<9.4%	<13.2%	<17.2%	<21.8%
15%, **20%**, 25%	$m_{net,\ EUV}$: Average Net Margin of Lithography Equipment Suppliers on EUVL products/services	>30.8%	>22.6%	>17.7%	>14.3%

30%, **50%**, 70%	$f_{financing}$: Fraction of remaining required financing which "Chipmaker EUV Backers" must provide to ASML and/or Nikon in order to significantly accelerate their EUVL development efforts	No such parameter values (between 0% and 100%)	No such parameter values (between 0% and 100%)	>0%	>0%
30%, **50%**, 70%	$f_{leading\ edge}$: Fraction of wafer starts which are "Leading Edge" (i.e., which require DP/MP or EUV lithography technology for patterning)	No such parameter values (between 0% and 100%)	No such parameter values (between 0% and 100%)	>22.7%	>12.8%
20%, **33%**, 50%	$f_{sr,\ DP/MP}$: Fraction of overall DP/MP patterning cost which corresponds to equipment and services purchases from the lithography suppliers	<20.7%	<28.9%	<37.9%	<47.9%
50%, **68%**, 80%	$f_{sr,\ EUV}$: Fraction of overall EUV patterning cost which corresponds to equipment and services purchases from the lithography suppliers	No such parameter values (between 0% and 100%)	>76.8%	>60.1%	>48.9%
30%, **50%**, 70%	$f_{chipmaker\ profit}$: Fraction of chipmaker manufacturing cost savings (from the introduction of EUVL) which are converted to net Chipmaker profits	n.a.	n.a.	n.a.	n.a.
12%, **15%**, 18%	Discount Rate	No such parameter values (which are > 0%)	No such parameter values (which are > 0%)	<26.1%	<38.7%
$1B, **$2B**, $5B	$I_{TOTAL,\ ASML}$: Additional Non-recurring engineering (i.e., R&D) costs remaining for ASML's EUVL project completion in October 2011	$5.6B additional "external" R&D funding needed (in addition to $I_{TOTAL,\ ASML}$ provided by ASML and Chipmakers)	$1.3B additional "external" R&D funding needed (in addition to $I_{TOTAL,\ ASML}$ provided by ASML and Chipmakers)	No additional "external" R&D funding needed (in addition to $I_{TOTAL,\ ASML}$ provided by ASML and Chipmakers)	No additional "external" R&D funding needed (in addition to $I_{TOTAL,\ ASML}$ provided by ASML and Chipmakers)
$2B, **$4B**, $7B	$I_{TOTAL,\ Nikon}$: Additional Non-recurring engineering (i.e., R&D) costs remaining for Nikon's EUVL project completion in October 2011	n.a.	n.a.	n.a.	n.a.

Several overall trends are interesting to observe from this cutoff analysis. First, we can see that ASML's decision to invest is significantly dependent on variations in the parameter values. From Figure 17, we recall that ASML's E(NPV) benefit from investing in the ('Finance ASML', 'Invest', 'Don't Invest') state of the world with a 'Uniform' EUVL outlook is \$19.8B-\$16.9B = \$2.9B which constitutes an E(NPV) ratio of 1.17 (also tabulated in summary Table 6). Thus, it is tautological in Table 10 that the base case parameter values will satisfy the 1.10 ratio criterion but not the 1.25 ratio criterion. Beyond this, such analysis gives us a clear sense of how each parameter value impacts ASML's decision to invest in EUVL in this sub-game (given a 'Uniform' EUVL outlook). For some parameters the entire high-low range specified in Table 10 passes the 1.1 E(NPV) criterion hurdle (e.g., annual growth rate for number of critical layers/wafer), while for others it does not (e.g., wafer demand CAGR). Finally, notice that this type of analysis clearly allows for evaluation of additional outside financing (provided by any source except ASML itself) which would be required to bring the E(NPV) ratio up to a certain cutoff value. In this instance, \$1.3B additional dollars of external funding would be required to bring ASML's ratio up to 1.25 (because from Figure 17, (\$19.8B + \$1.3B)/(\$16.9B = 1.25)).

From this perspective, it is clear that any party interested in convincing ASML to develop EUVL should consider both direct funding and any efforts to help shoulder some risk for ASML (which can be thought of as reducing the required E(NPV) ratio). If such ASML risk mitigation can be done inexpensively, it could be more appealing than direct provision of additional funding.

Table 11: Parameter Values Cross-Overs for Nikon's Decision to Invest in EUVL Technology (Assumes: Chipmakers' 'Finance Both' and ASML 'Invests' and 'Uniform' EUVL Outlook)

		$\frac{E(NPV)_{ASML,Invest}}{E(NPV)_{ASML,Don't\ Invest}}$ values which are:			
Low/ Base/ High	**EUVL parameters**	**> 1.5**	**> 1.25**	**> 1.10**	**>1**
6%, **10%**, 14%	g_{wafer}: Wafer Demand CAGR, 2011-2021, assuming EUVL is ultimately developed	>19.1%	>11.1%	>7.2%	>4.9%
-5%, **0%**, 8%	$g_{wafer,\ no\ EUV}$: Annual Growth Rate in Demand for 300mm Wafer Starts (starting in 2016 if no EUVL is developed)	No such parameter values	No such parameter values	<62.2%	All parameter values
6%, **12%**, 18%	$g_{critical\ layers}$: Annual growth rate of average number of critical layers/wafer	>23.1%	>13.2%	>9.1%	>6.8%
-5%, **5%**, 15%	$g_{EUV\ cost}$: Annual growth of EUVL patterning cost/wafer)	>15.4%	>6.1%	>2.3%	>0.1%
5%, **10%**, 15%	$g_{cost\ ratio}$: Annual growth rate of *RATIO* of DP/MP patterning costs to EUVL patterning --from 2011-2021	<-4.3%	<7.2%	<21.8%	All (reasonable) parameter values
10%, **15%**, 20%	$m_{net,\ DP/MP}$: Average Net Margin of Lithography Equipment Suppliers on DP/MP products/services	<5.8%	<12.3%	<37.6%	All parameter values
15%, **20%**, 25%	$m_{net,\ EUV}$: Average Net Margin of Lithography Equipment Suppliers on EUVL products/services	>29.1%	>21.3%	>16.5%	>13.4%
30%, **50%**, 70%	$f_{financing}$: Fraction of remaining required financing which "Chipmaker EUV Backers" must provide to ASML and/or Nikon in order to significantly accelerate their EUVL development efforts	>82.0%	>54.4%	>37.9%	>26.9%
30%, **50%**, 70%	$f_{leading\ edge}$: Fraction of wafer starts which are "Leading Edge" (i.e., which require DP/MP or EUV lithography technology for patterning)	No values between 0% and 100%	>54.9%	>40.3%	>34.2%
20%, **33%**, 50%	$f_{sr,\ DP/MP}$: Fraction of overall DP/MP patterning cost which corresponds to equipment and services purchases from the lithography suppliers	<12.7%	<27.1%	<82.4%	All parameter values between 0% and 100%
50%, **68%**, 80%	$f_{sr,\ EUV}$: Fraction of overall EUV patterning cost which corresponds to equipment and services purchases	>99.0%	>72.3%	>56.3%	>45.6%

	from the lithography suppliers				
30%, **50%**, 70%	$f_{\text{chipmaker profit}}$: Fraction of chipmaker manufacturing cost savings (from the introduction of EUVL) which are converted to net Chipmaker profits	n.a.	n.a.	n.a.	n.a.
12%, **15%**, 18%	Discount Rate	<4.6%	<13.8%	<18.1%	<20.6%
\$1B, **\$2B**, \$5B	$I_{\text{TOTAL, ASML}}$: Additional Non-recurring engineering (i.e., R&D) costs remaining for ASML's EUVL project completion in October 2011	n.a.	n.a.	n.a.	n.a.
\$2B, **\$4B**, \$7B	$I_{\text{TOTAL, Nikon}}$: Additional Non-recurring engineering (i.e., R&D) costs remaining for Nikon's EUVL project completion in October 2011	\$1.3B additional "external" R&D funding needed (in addition to $I_{\text{TOTAL, Nikon}}$ provided by Nikon and Chipmakers)	\$0.2B additional "external" R&D funding needed (in addition to $I_{\text{TOTAL, Nikon}}$ provided by Nikon and Chipmakers)	No additional "external" R&D funding needed (in addition to $I_{\text{TOTAL, Nikon}}$ provided by Nikon and Chipmakers)	No additional "external" R&D funding needed (in addition to $I_{\text{TOTAL, Nikon}}$ provided by Nikon and Chipmakers)

Next, let us consider Nikon's decision of whether to invest in EUVL based on the analysis in Table 11 above. Recall that this analysis is referenced to the ('Finance both', 'Invest', 'Invest') state of the world assuming a 'Uniform' EUVL outlook by each of the three players. Generally speaking, I considered this the "runner up" SPNE prediction outcome based on the base case analysis, and definitely a scenario of strong interest. In this context, Nikon's E(NPV) benefit from investing is \$5.3B - \$4.4B = \$0.9B which constitutes an E(NPV) ratio of 1.20 (also tabulated in Table 6). Again, it is tautological in Table 11 that base case parameters will satisfy the 1.10 ratio criterion but not the 1.25 ratio criterion. This analysis gives us a clear sense of how each parameter value impacts Nikon's decision to invest in EUVL in this future state of the world (given a universal 'Uniform' EUVL outlook).

Conventional wisdom might suggest that a smaller and financially weaker supplier (especially one with other disjoint, viable business units) would be more risk averse than a larger and

financially stronger (pure-play lithography) supplier would be. Thus, it seems reasonable to speculate that a 1.17 E(NPV) ratio might not be sufficient to entice Nikon to invest. Also, note in the last row of Table 11 that an additional $0.2B (from outside Nikon, and above and beyond the $2B which Chipmakers are already assumed to contribute in this state of the world) would be required in this scenario to bring Nikon's ratio up to 1.25, while an additional $1.3B would be required to bring it up to a ratio of 1.5 instead. Again, any party wishing to entice Nikon to invest should consider both strategies which mitigate Nikon's risk as well as provide direct additional financing (which, of course, has some salutary effect of reducing Nikon's risk as well).

4.11 EUVL Model Variants, Limitations, and Future Work

Now that we have provided a detailed sensitivity analysis on the EUVL model outcomes, let us spend some time discussing other possible strategic situations to which modified versions of the model could be applied, factors which are not captured by the model, and potential fruitful avenues for developing this modeling work further.

4.11.1 Other Potential Variants of the EUVL Model

Test higher critical patterning market share cap for EUVL technology (i.e., above 60%)

Currently, four of the five scenarios (all except Scenario #4.1) assume that EUVL technology will reach a cap of 60% of the critical patterning market. This assumption is made in part because of the deep technological uncertainties in EUVL commercialization (especially the cost vs. wafer throughput) and ongoing learning curve improvements in 193i DP/MP technologies. This assumption could be relaxed by carefully altering the ramp rates for EUVL under various

investment scenarios to be consistent with a critical patterning MS cap above 60%. (See Appendix A for details about the base case ramp rate assumptions.)

Examine scenario in which Nikon drops out of 193i DP/MP production more easily

Currently, the four of the five scenarios (all except Scenario #4.1) assume that both suppliers remain viable players in the critical patterning market with at least 20% overall critical patterning market share. In the case that only ASML develops EUVL technology and ramps that technology to 60% of the critical patterning market share, this implies that ASML and Nikon will equally divide the remaining 40% of critical patterning using each of their versions of 193i DP/MP. *Ceteris paribus*, the chipmakers have a vested interest in having two viable lithography suppliers and thus could be expected to continue to buy equipment from Nikon in order to ensure dual supply for the industry. However, it is important to note that learning curve inefficiency (due to small equipment production) and competitive product lagging could make it less attractive for chipmakers to buy some of their equipment from Nikon over time. Scenarios where Nikon is assumed to exit the market under less financial/competitive pressure could be analyzed by carefully modifying the EUVL ramp assumptions (see Appendix A) to examine how such assumptions would change the dynamics of the EUVL R&D game developed in this chapter.

Test different levels of pricing multipliers for 193i DP/MP when ASML's EUVL attains a certain market share (even if Nikon still maintains 20% of the critical patterning market)

Related to the previous section, even if Nikon is able to maintain 20% critical patterning market share through its 193i DP/MP optical lithography offerings, chipmakers might still suffer a particularly high price for EUVL equipment. Currently, the EUVL model only applies an additional lithography equipment price multiplier (to both EUVL and DP/MP offerings) in a

binary fashion if one supplier completely exits the critical lithography patterning market. This assumption could be relaxed by applying additional lithography pricing multipliers in a more graduated fashion when EUVL penetrates the market, even if one supplier retains a small market share in DP/MP lithography.

Chipmakers make a credible "50/50" 193i DP/MP threat to ASML if slow progress is deemed to be from less than full effort on the part of ASML

It should be clear from much of the analysis in this chapter that ASML currently has a commanding market position in lithography. However, the fact that there are two suppliers of 193i DP/MP optical lithography technology (which is destined to remain a very important technology regardless of the fate of EUVL) means that even if Nikon does not develop EUVL, chipmakers still have a strong lever for influencing ASML's overall payoffs. In particular, if some subset of chipmakers consciously support Nikon's 193i franchise, this will reduce the amount of revenue ASML can expect from 193i. In particular, the impact on ASML of having 80% 193i market share (i.e., its approximate share as of 2011-2012) vs. having 50% market share is quite substantial. Hence, in addition to chipmaker financing aid (and now non-voting equity ownership, after the ASML customer co-investment program events of July and August 2012), chipmakers may still be able to credibly indicate their intentions to help Nikon gain 50% market share in 193i DP/MP technology. The EUVL model framework could provide an approximate estimate of how this scenario would impact the strategic dynamics regarding the introduction of EUVL. Although the author is not aware of any such "credible threat" being used so far by chipmakers, this should largely be viewed as a variation on the theme of the effort announced by chipmakers to support further developments of Nikon's 193i line of equipment (see Section 4.8.3).

4.11.2 Key Factors Not Accounted for in EUVL Model

Any process of using a quantitative model such as the EUVL model presented here for strategic decision making must not lose sight of the factors which the model fails to capture (or which it captures in a substantially simplified manner). In that spirit, below are some factors which have not been incorporated into the EUV model presented above.

Accurate estimation of the semiconductor chip demand reduction likely if EUV is not developed. The EUVL model developed here has a simple assumption regarding the demand impact of EUVL to chipmakers. It assumes that although the equipment suppliers may be impacted by a reduction in wafer (and hence lithography equipment) demand, the Chipmakers cost savings from EUV will be calculated as if there is no reduction in wafer demand and hence, more importantly, critical patterning chipmaker manufacturing costs. This has the impact of "compensating" the Chipmakers' profit function not by the full impact to the revenue of lost wafers, but simply by the amount it would have cost to pattern the lost wafers. This assumption allows for simplicity and transparency in the model, yet does not allow the Chipmakers' Δ E(NPV) to be augmented by a reduction in wafer demand if EUVL is not developed (an impact counter to a basic understanding of the technology transition being studied).

Gaming effects between the chipmaking companies which comprise the "Chipmaker EUV Backers". In the EUVL model, the "Chipmaker EUV Backers" have been assumed to be an amalgamated single player which could somehow avoid deleterious gaming effects among the individual firms. One inter-chipmaker gaming effect would be the impact of any market share gains made possible by access to the earliest EUVL tools. (See Manners (8/28/12) for one opinion that the three chipmakers who participated in the ASML co-investment program are likely to get early access to ASML's first EUV tools.) Other chipmaker gaming effects could

also be considered such as fast following, a phenomenon which will be discussed in much greater depth in Chapter 5 in the context of the potential industry transition to 450mm wafers.

Competitive efforts to "hurry up" EUVL development by one supplier due to the actions of the other supplier or due to the action of the Chipmakers (other than via direct financial assistance to the supplier in question). For example, it is plausible that ASML might proceed with EUVL development more quickly if there was strong evidence that Nikon was vigorously investing in EUVL or if the Chipmakers had chosen to publicly help finance Nikon's EUVL effort.

Explicit modeling of EUVL "ecosystem" impacts (e.g., the level of progress in EUVL patterning masks and defect metrology). Additional support, financial or otherwise, for these ecosystem activities would presumably speed up the potential EUVL introduction at both ASML and Nikon. As the EUVL game is currently framed, chipmakers only have the options to support ASML or Nikon directly, and indirect support of EUVL ecosystem companies is not modeled as a strategic choice.

Alternative lithography technologies (besides EUVL or 193i DP/MP) or new market entrants.

Probability distributions across individual model input parameters. Although the analysis here explicitly examines uncertainty due to the EUVL introduction timing and one-at-a-time variation of individual model parameters, it does not explicitly model stochasticity of model input parameters.

Assumptions regarding what happens in lithography after 2021. Given the extreme technological complexity, visibility of likely lithography technologies beyond 2021 is tremendously limited. However, individual assumptions regarding the possible scenarios could

be appended to the current cash flow time frame (2011-2021) to see how they might impact current EUVL strategic decision making.

Potential impact of governmental actions to aid one or more player. One could try to model the impact of governmental aid to one or more of the players in the EUVL model (e.g., Japanese government helping out Nikon, given that Japanese government-backed EUVL consortia were significant at one point in time).

4.11.3 Areas for Future Work Related to EUVL Model

Enable industry experts to scrutinize the EUVL model. They may be able to provide better input parameter estimates, point out deficiencies in the model structure, and judge the overall model for economic realism. Experts particularly familiar with the financial assumptions and data underlying semiconductor manufacturing would be most helpful. Ensuring that the model is well documented and user-friendly would clearly aid this effort.

Refine model parameter estimates/ranges from secondary data sources.

Incorporate (annual) market share assumptions for EUVL and DP/MP which are more directly responsive to chipmakers' cost minimization considerations. It is likely that simply choosing the minimum cost technology in each year will not be an optimal decision criterion due to learning curve and capacity effects for both the equipment suppliers and the chipmakers.

Explore ways to make the model more dynamic in nature (i.e., more than two stages).

Perform modeling with probability distributions assumed for the model input parameters. Currently the model uses deterministic model parameter inputs. The model could be simulated with stochastic model input parameters (e.g., using triangular or uniform probability distributions

spanning the parameter ranges shown in Table 9). One significant complication here is that within game theory models when deviations occur from the perfect information and common knowledge assumptions, calculation and interpretation of equilibria become much more complex.

Analyze relevant potential scenarios which involve changing more than one input parameter (perhaps based on known correlations between some of the parameters, when warranted by historical data). Some examples of pairs of correlated input parameters to include in such scenarios might include:

- Investment for ASML and Investment for Nikon (likely a positive correlation)
- Net margin of suppliers on EUVL and Net margin of suppliers on DP/MP (likely a positive correlation)
- Net margin of suppliers on EUVL and cost ratio between DP/MP and EUVL (likely a positive correlation)
- Net margin of suppliers on DP/MP and cost ratio between DP/MP and EUVL (likely a negative correlation)
- Net margin of suppliers on EUVL and annual growth in critical layers/wafer (likely a positive correlation)

4.12 Chapter Summary

The EUVL model predicted a large investment (approximated at $1B) by the Chipmakers in ASML's EUVL program quite robustly to changes in EUVL outlook and to many (but not all) model parameter changes within broad potential ranges. In accordance with both intuition and the assumptions embedded in the EUVL model, it only makes sense for Chipmakers to invest in

ASML's EUVL program if they expect that ASML will in fact vigorously invest its own money and effort into the technology as well. The model demonstrated that ASML does *not* have an entirely unambiguous incentive to invest vigorously in EUVL. Although from a pure E(NPV) decision criterion they have an dominant action to invest in EUVL, if a moderate amount of risk-aversion on the part of ASML is assumed, investment is no longer dominant. The model allowed us to quantify the moderate degree to which the Chipmakers investment in ASML bolstered their incentive to invest (assuming that Nikon would not invest) and highlighted the fact that any Chipmakers' effort (besides direct financial assistance) which reduced ASML's risk level should also be considered. Under a 'Uniform' EUVL outlook using the base case parameters, a $1B investment by the Chipmakers would increase ASML's incentive to invest in EUVL by $1.1B and increase their E(NPV) ratio for investment from 1.11 to 1.17 (see Table 6).

Nikon, a struggling lithography supplier with other viable business units, might be expected to exhibit somewhat greater risk-aversion than either ASML or the Chipmakers. Under this assumption, it seems likely that Nikon will choose not to invest except if they receive considerable financial assistance (from Chipmakers or others) *and* they have a quite optimistic outlook for the implementation of EUVL technology. Indeed, the "runner up" sub-game perfect Nash Equilibrium from the overall model analysis was: ('Finance both', 'Invest', 'Invest'). However, in reality, this equilibrium outcome would entail considerably greater risk for both Chipmakers and Nikon, not to mention considerable additional coordination costs among the players.

Although the model has considerable sensitivity to model input parameters and explicitly does not include some potentially strategically important considerations, it does seem to capture the real fundamental dynamics of this technology investment decision in a cognitively efficient

manner. This type of modeling would be quite useful to corporate strategists and policy makers in determining their course of action and galvanizing effort toward unified action once that course of action is selected. A more detailed analysis of the features of the EUVL transition which made it amenable to such analysis is given in the concluding chapter (Chapter 7).

Chapter 5: The 450mm Wafer Size Model

"We believe 450-mm is going to happen, but is likely to involve funding from chip companies. Equipment companies will not foot the bill alone this time."

-C.J. Muse, Industry Analyst (October 2010)
(from Lapedus, 10/25/10)

5.1 Game Structure of 450mm Model

As described earlier in Chapter 3, the 450mm wafer-size transition is one during which both chipmakers and equipment suppliers must be intimately and financially involved with new equipment development. The added complications of 450mm manufacturing technology development (over and above those experienced for EUV lithography development) stem from two key factors regarding the technology and industry structure. First, a wafer-size transition involves a much larger fraction of the semiconductor equipment supplier base than a lithography transition (even one as technologically complex as EUVL). To achieve the 450mm transition, not only must new 450mm-capable lithography equipment be developed, but so must 450mm-capable etch equipment, 450mm-capable thin films equipment, and so on. Because these different categories of equipment are often produced by distinct sets of firms (recall Figure 5), a greater number of equipment firms must be involved for 450mm than in the case of EUVL technology. Second, a wafer-size increase is desired by large chipmakers primarily for cost (per chip) reduction purposes, and not because any technologically superior chips can be intrinsically manufactured on the larger wafer size.

Both of these factors imply that wafer-size transitions, including the one currently being considered to 450mm diameter wafers, are more communal in nature than are improvements to

individual functional areas (such as the development of EUVL or other less sophisticated process-specific improvements in semiconductor manufacturing).

Because each functional area must develop equipment capable of processing 450mm wafers (the first factor highlighted above), some element of veto power resides with the viable equipment suppliers for each crucial toolset, especially those which command a high market segment share in their respective functional areas -- quite a common situation. (See Hutcheson [2013] for more details.) If those suppliers do not develop their functional area's 450mm tools, then the overall 450mm development project is likely to be delayed. Stated in economic terms, the various functional area tools for processing 450mm wafers are perfect complements of each other.

As a consequence of the second factor highlighted above, some chipmakers believe they can quickly "fast follow" those chipmakers which invest early to make 450mm wafer processing happen. That is, the fast followers believe they can (at least to some extent) avoid the large upfront 450mm investment made by early-adopting chipmakers.

The communal nature of the 450mm wafer transition makes the formulation of tightly constructed non-cooperative game theory models with a small number of players seem initially more problematic than was the case for EUVL technology (Chapter 4). Despite that apparent difficulty, this parsimonious game theoretic modeling approach was pursued fully. I describe that effort below in a manner which roughly parallels the EUVL analysis in Chapter 4, including explanations of game structure assumed, payoff estimation methodology, (tentative) model predictions, sensitivity analyses of the model predictions, and limitations encountered. At the

conclusion of this chapter, after detailing the 450mm model and analysis, I provide a brief comparison between the EUV lithography modeling effort and the 450mm wafer transition modeling effort highlighting their commonalities and differences.

The first 450mm modeling choice was to decide which players to include in the 450mm model and which strategic R&D funding choices to endow each of them. Because several (certainly four or more) equipment suppliers are necessary to generate a full, complementary set of 450mm equipment, I decided to abstract away from the individual equipment suppliers entirely and to focus on the strategic interactions among the very largest chipmakers which would be early financial backers of 450mm equipment (either through direct financing contributions or through guarantees to the equipment suppliers to purchase early versions of the 450mm equipment). To some extent, the decision to invest early in 450mm development also entails the *in situ* work of early-adopting chipmakers helping suppliers debug and optimize their equipment software, wafer handling hardware, and wafer processing recipes in the earliest 450mm wafer processing fabs (i.e., factories).

Because of the extremely high cost expected for 450mm equipment and for building efficient-scale 450mm silicon wafer fabs, when selecting strategic players I focused on the subset of very largest chipmakers – those who could afford the expense and risk involved with building such costly manufacturing plants while the 450mm technology is still in its early stages. There is a natural break in size between the three largest chip manufacturers and the rest (see Notebookcheck 3/28/13; Solid State Technology 1/23/12), so I chose to model those three chipmakers (Intel, Samsung, and TSMC) as the three strategic players who could provide early investment in 450mm processing technology. Beyond these three largest chipmakers, it is

widely believed that from one to several additional smaller chipmakers are likely to make the transition to 450mm wafers eventually, assuming 450mm does in fact get successfully developed (see McGrath 7/11/12). However, it is unlikely that these smaller chipmakers will be among the very first to finance 450mm equipment development significantly. Hence, the model described below focuses squarely on the strategic interaction for investing in 450mm technology among Intel, Samsung, and TSMC (sometimes referred to as simply IST).

The second key modeling decision is to determine the actions available to the three strategic players. Clearly, the economic reality is that funding for the 450mm wafer equipment will not be committed all at once, and there is a dynamic game occurring where the three strategic players continuously observe the overall market, semiconductor technology evolution, and each other's ongoing strategic actions as the game progresses (see Hutcheson 2006). However, at least in terms of overall economic incentives, it is possible for each firm to contemplate the steady-state desirability of investing in 450mm wafer technology given the corresponding 450mm investment decisions by each of the other two strategic players. After significant iteration, I decided upon the simplified binary choice of 'Invest' or 'Don't invest' (which is shorthand for 'Invest heavily early in 450mm' or 'Don't invest heavily early in 450mm') as the actions available to each of Intel, Samsung, and TSMC. At the time of this modeling effort (2011-2012), although Intel, Samsung, and TSMC (and a few other chipmakers) had already undertaken some 450mm-related financial investments, most of the 450mm R&D investments still lay in the future (McGrath 9/27/11; McGrath 7/11/12). Intel, Samsung, and TSMC are all quite large, and I assumed they would each would have the capability to invest significant *additional* money to accelerate the progress of 450mm equipment development, or decide not to make such investments. Consistent with the foregoing observations, I modeled the overall strategic interaction among Intel,

Samsung, and TSMC (IST) as a simultaneous (i.e., single-stage) game. These assumptions imply that the game structure which should be used is that shown in Figure 24 below.

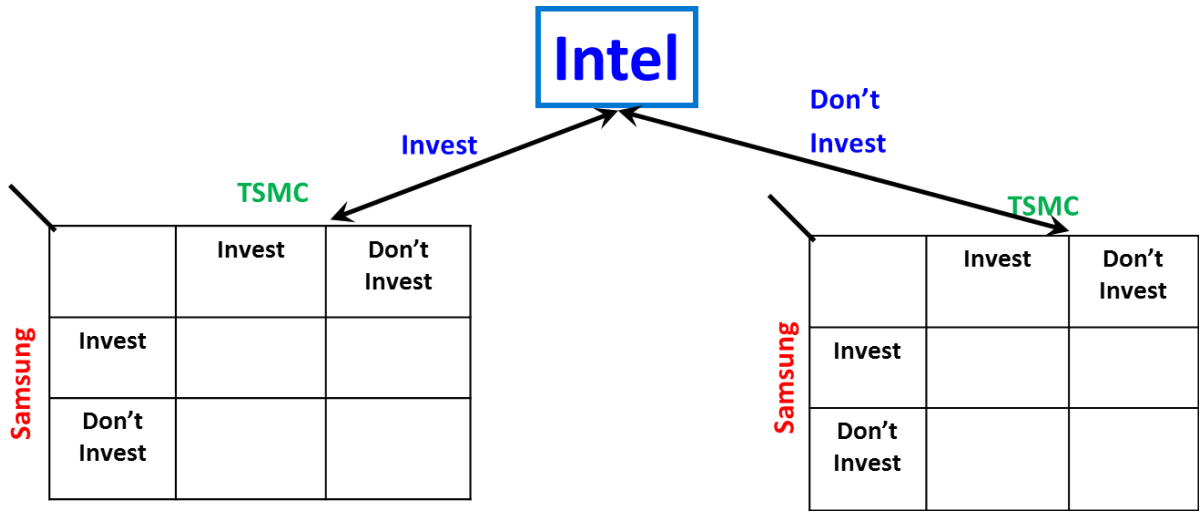


Figure 24: Game Structure for 450mm Equipment R&D Investment Game

5.2 Payoff Sub-components for 450mm Model

Given this game structure, the next modeling choice was to define a framework for calculating the 24 (=3x8) payoffs corresponding to each firm's payoff in the eight possible future states of the world shown in Figure 24. As with the EUVL model, I included only a small number of critical financial factors to ensure parsimony and transparency regarding drivers of the model outcomes.

The key financial factors incorporated into the payoff calculations for the three chipmakers were:

- *Direct expense to each chipmaker of their 450mm early equipment R&D financing efforts.*

- *Expected ramp of manufacturing cost savings when 450mm equipment becomes available.* Among Intel, Samsung, and TSMC, I assumed the firms who invested early would attain the manufacturing cost savings associated with 450mm wafers zero, one, or two years earlier than the firms who did not invest early in 450mm.
- *Market share implications (i.e., gains and losses) due to early 450mm investment.* Because these market share impacts are hard to reliably predict, I explored several different sets of assumptions ranging from no share (0%) to a moderate share (2.5%) of the overall semiconductor market revenue being contestable by the chipmakers, by virtue of their 450mm investment decisions. I also modeled scenarios in which early 450mm technology backers among Intel, Samsung, and TSMC gained contestable market share from each other (i.e., from those among IST who chose not to invest early in 450mm technology) or from the smaller chipmakers (i.e., chip manufacturers ranking fourth and smaller in size).

A summary of the assumptions underlying the nine main 450mm scenarios analyzed can be found in Table 12 through Table 14 below. Let us take some time to explain in detail the rationale behind these modeling assumptions.

5.3 Core Assumptions and Base Case Scenario Definition for 450mm Model

Just as with the EUVL model, it is vital to take care in determining the core assumptions which define the actions available to each player and how those actions translate into financially relevant variables which determine the game payoffs. In the case of the EUVL model in Chapter 4, a crucial assumption was that the chipmakers who decided to be early backers of EUVL technology would be able to coordinate their actions in some reasonably efficient manner. (This assumption was necessary to justify the modeling simplification of treating the chipmakers as

one amalgamated player.) In the 450mm wafer model it is similarly necessary to make carefully considered assumptions regarding how the chipmakers' investment actions are likely to interact with the actions of key equipment suppliers (especially because the suppliers are absent as strategic players per Section 5.1 above).

One can safely make the assumption that equipment suppliers, in addition to desiring direct financial assistance from chipmakers for 450mm equipment development, also would like to reduce their financial risk regarding the timeline for 450mm equipment development. This is the case because of:

- The negative experience of some of the equipment suppliers going through the 200mm to 300mm wafer-size transition (see SEMI 9/1/12; Hutcheson 2006).
- The understanding that smaller numbers of tools will be sold on the 450mm wafer platform than would correspondingly be sold on the 300mm platform.
- The high technological and economic risk accompanying the 450mm wafer-size transition.
- The high expense of 450mm wafer development (see McGrath 7/11/12; SEMI 9/1/12; Hutcheson 2006).

These general considerations were important as I developed the 450mm wafer model payoff assumptions summarized in Table 12 and Table 13 below (see Appendix B for a more comprehensive set of detailed assumptions and justifications on model parameters).

Table 12: Core Assumptions in 450mm Wafer Model (All Scenarios)

• Just as with the EUVL model, the 450mm model relies on relative E(NPV) analysis to compare various future states of the world. The E(NPV)s for each player are defined relative to the "status quo" in which none of the chipmakers invest and thus 450mm equipment is never developed. The E(NPV)s for each chipmaker in the status quo outcome are thus defined to be zero. Chipmaker E(NPV)s in all other states of the world are defined relative to this zero-point.
• The remaining R&D budget for 450mm wafer development (at the time of the modeling in late 2011) is estimated to be $15B USD (see Appendix B for details). • The fraction of that total investment expected to come from the Chipmakers which would ensure rapid development of 450mm equipment is approximated to be 40% (or $6B). Smaller total investment amounts from the Chipmakers would correspond to slower development of 450mm technology. • For simplicity, the base case assumption is that each chipmaker among IST would need to contribute an equal share of the total "full investment amount" of $6B (or $2B each) to benefit from being an early investor in 450mm technology.

• I estimated the manufacturing cost savings from 450mm wafer manufacturing for each of the three players as a 20% reduction in their total annual estimated COGS.
• Due to high uncertainty about growth of wafer demand and costs, for the base case, I assumed a zero growth rate for 450mm COGS for Intel, Samsung, and TSMC. The 2011 COGS numbers estimated for each firm are:
  ○ $COGS_{Intel}$ = $15.1B
  ○ $COGS_{Samsung}$ = $11.8B
  ○ $COGS_{TSMC}$ = $7.4B
• I assumed chipmakers' benefits would commence (in a binary fashion) after some delay from their one-time 450mm investments in 2011. The specific dates at which the benefits commence are shown in Table 13 below as a function of the investment decisions of the three players.

• Assumptions regarding market share impacts resulting from 450mm investment are addressed by defining scenarios with differing "time lags" experienced by fast followers and differing market share impacts for both early investors and fast followers (see Table 13 and Table 14 below).
• The 450mm wafer development project is deemed to have significant economic risk, but relatively modest technological risk. Hence, I applied an annual discount rate of 12% to each firm's expected benefit cashflows.
• Consistent with the expected long-lived nature of silicon wafer manufacturing and the widely held belief that 450mm will be the ultimate wafer size for this industry, I chose a 20-year time horizon (2011-2031) for cash flows associated with 450mm benefits/losses.

Table 13: IST 450mm Investment Amounts and Benefits Start Dates

Number of early investors (among IST) in 450mm (in 2011)	**Total Chipmaker Investment in 450mm in 2011** *($2B from each chipmaker that invests)*	**Chipmaker Benefit Start Dates**		
		Scenario #5.0 *(mfg cost savings only)*	**Scenario #5.1-#5.4** *(mfg cost savings and market share gains/losses)*	**Scenarios #5.5-#5.8** *(mfg cost savings and market share gains/losses)*
No chipmakers	$0B	Never	Never	Never
Only one chipmaker	$2B	2018: early investor 2018: lagging investors	2018: early investor 2019: lagging investors	2018: early investor 2020: lagging investors
Two chipmakers	$4B	2017: early investors 2017: lagging investor	2017: early investors 2018: lagging investor	2017: early investors 2019: lagging investor
All three chipmakers	$6B	2016: all three investors	2016: all three investors	2016: all three investors

Figure 25 below illustrates the modeling simplification for 450mm-relevant cash flows for each chipmaker. I assumed the annual benefits (both manufacturing cost savings and market share gains/losses) are a fixed cash flow commencing according to the date specified in Table 13 and finishing in 2031 (i.e., at the end of the 20-year time horizon). The cash flows are fixed because I assumed no growth in COGS (feeding into the calculation of manufacturing cost savings) and no growth in overall semiconductor market revenue (feeding into the calculation of the permanently assumed market share shifts due to 450mm investment). Sensitivity to these assumptions will be addressed in Section 5.5 after we analyze the base case model results.

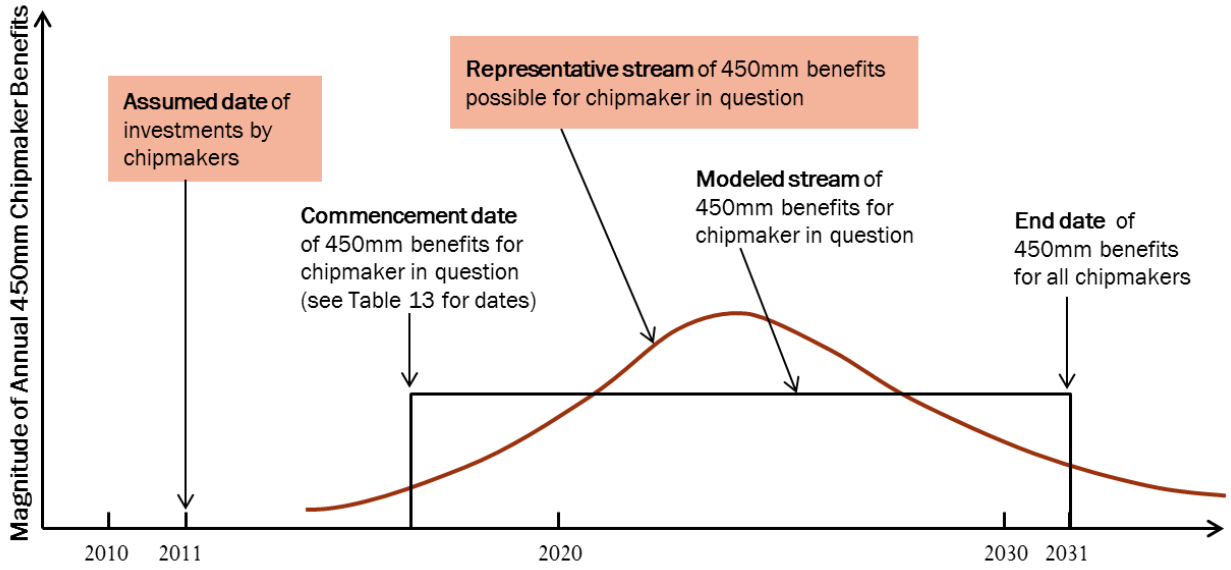


Figure 25: Conceptual Schematic of 450mm Benefit Cash Flows Assumed for Chipmakers

Now let us examine the assumed market share implications for each chipmaker of investing or not investing in 450mm technology, the final differentiating factors which distinguish the nine "base case" scenarios defined to analyze the strategic interactions among the three players. These market share assumptions are shown in Table 14 below.

Table 14: Market Share Changes Due to 450mm Investment Associated with Scenarios #5.0 through #5.8

Scenario Considered	Chipmaker Investment Choices	Semiconductor MS impact (% change)	***Scenario Considered***	Chipmaker Investment Choices	Semiconductor MS impact (% change)
Scenario 5-0: *- 0 Year Time Lag - 0% MS Contestable*	IST All Invest	IST: No Change			
	Two of IST Invest	IST: No Change			
	One of IST Invest	IST: No Change			
	None of IST invest	IST: No Change			
Scenario 5-1: *- 1 Year Time Lag - 0% MS Contestable*	IST All Invest	IST: No Change	***Scenario 5-5:*** *- 2 Year Time Lag - 0% MS Contestable*	IST All Invest	IST: No Change
	Two of IST Invest	IST: No Change		Two of IST Invest	IST: No Change
	One of IST Invest	IST: No Change		One of IST Invest	IST: No Change
	None of IST invest	IST: No Change		None of IST invest	IST: No Change
Scenario 5-2: *- 1 Year Time Lag - 1.5% MS Contestable - Competition Among IST*	IST All Invest	IST: No Change	***Scenario 5-6:*** *- 2 Year Time Lag - 2.5% MS Contestable - Competition Among IST*	IST All Invest	IST: No Change
	Two of IST Invest	Dual Investors: +0.75% Sole Laggard: -1.5%		Two of IST Invest	Dual Investors: +1.25% Sole Laggard: -2.5%
	One of IST Invest	Single Investor: +1.5% Dual Laggards: -0.75%		One of IST Invest	Single Investor: +2.5% Dual Laggards: -1.25%
	None of IST invest	IST: No Change		None of IST invest	IST: No Change
Scenario 5-3: *- 1 Year Time Lag - 1.5% MS Contestable - 50%/50% Competition Split*	IST All Invest	IST: No Change	***Scenario 5-7:*** *- 2 Year Time Lag - 2.5% MS Contestable - 50%/50% Competition Split*	IST All Invest	IST: +0.417% (=1.25%/3)
	Two of IST Invest	Dual Investors: +0.75% Sole Laggard: -0.75%		Two of IST Invest	Dual Investors: +1.25% Sole Laggard: -1.25%
	One of IST Invest	Single Investor: +1.5% Dual Laggards: -0.375%		One of IST Invest	Single Investor: +2.5% Dual Laggards: -0.625%
	None of IST invest	IST: No Change		None of IST invest	IST: No Change
Scenario 5-4: *- 1 Year Time Lag - 1.5% MS Contestable - IST Competition with Smaller Chipmakers*	IST All Invest	IST: No Change	***Scenario 5-8:*** *- 2 Year Time Lag - 2.5% MS Contestable - IST Competition with Smaller Chipmakers*	IST All Invest	IST: +0.833% (=2.5%/3)
	Two of IST Invest	Dual Investors: +0.75% Sole Laggard: No Change		Two of IST Invest	Dual Investors: +1.25% Sole Laggard: No Change
	One of IST Invest	Single Investor: +1.5% Dual Laggards: No Change		One of IST Invest	Single Investor: +2.5% Dual Laggards: No Change
	None of IST invest	IST: No Change		None of IST invest	IST: No Change

5.3.1 Justification of Scenario Definitions for 450mm Model

Table 14 above summarizes differences among the nine main scenarios analyzed in the 450mm model (Scenarios #5.0 through #5.8). These scenarios differ on only three assumed factors: the time lag duration between when early investors and non-early investor (i.e., fast followers) among IST start to accrue manufacturing cost savings and experience any market share (MS) gains/losses; the fraction of the total semiconductor market (~$304B in 2011, from Table 48 in Appendix B) generated by both IST and non-IST chip manufacturers which is contestable by virtue of early investment or non-early investment in 450mm technology; and the nature of the competition determining the outcome for the semiconductor market share which is contestable by virtue of 450mm investment.

Scenario #5.0 assumes no time lag or market share effects as a result of IST's decisions about early investment in 450mm technology. This scenario is a "reference scenario" in the sense that early investors are assumed to gain no *appropriable* advantages from their early investments in 450mm technology. Thus if one of IST invests early in this scenario (i.e., spend $2B) they get the manufacturing cost saving benefits of having 450mm technology, but the non-investors receive exactly the same cost savings advantage as well (and no market share changes take place).

From Table 14 it is also easy to see that Scenarios #5.1 and #5.5 also assume no market share changes for Intel, Samsung, or TSMC as a result of their decisions about investing in 450mm technology. However in Scenario #5.1 manufacturing cost savings start to accrue one year later for fast followers, and in Scenario #5.5 savings start to accrue two years later for fast followers. (Table 13 is a guide to the exact timing.)

Scenarios #5.2 through #5.4 assume that (among IST) electing to fast follow on 450mm is only moderately impactful, corresponding to a one-year time lag for fast followers and a contestable semiconductor market share of 1.5%. The only differing factor between these three scenarios is the nature of the competition for the 1.5% contestable market share. In Scenario #5.2, the competition for this 1.5% overall semiconductor share is entirely among IST (with no IST gain in share from the smaller chipmakers). In Scenario #5.4, the competition for this 1.5% overall semiconductor share is entirely between IST and the smaller chipmakers (with no competition among IST for market share). Scenario #5.3 assumes a 50%/50% mixture of the competition types represented by Scenarios #5.2 and #5.4; a 0.75% market share is contestable among IST, and an additional 0.75% market share can be gained by IST from the smaller chipmakers. Given these assumptions about the nature of the market share competition (again, due solely to 450mm investment), the resultant market share changes as a function of all possible actions by the three players are shown in Table 14 above.

The assumption made across all 450mm scenarios is that once the 450mm benefits start to accrue for a given chipmaker the annual market share changes experienced are permanent throughout the time horizon of the analysis, 2011-2031, assumed for the base case scenarios. (Recall Figure 25 above illustrates this point schematically.) Obviously, this is quite a strong assumption given that future market share shifts are difficult to predict, and, as will be demonstrated, the assumptions one makes about market share changes are vital to determining the incentives of (and often decisive for) the chipmakers regarding investing in 450mm wafer technology.

To avoid potential confusion, it is also important to point out one small modeling simplification for calculation made regarding the market share changes – the model does allow, in some cases, for a one or two-year time lag between when an early investor experiences its market share gains

and when a fast follower experiences its market share losses. (The exact dates for market share implications for each firm are those shown in Table 13 above, and Appendix B traces a full example payoff calculation to clarify this point.) Because IST currently represents approximately one-third of the semiconductor revenue and the quite long time horizon (20 years) for benefit accrual in this model, this simplification has a very small impact on the payoff estimate calculations.

Scenarios #5.6 through #5.8 are analogous to Scenarios #5.2 through #5.4 (respectively). The only differences correspond to Scenarios #5.6 through #5.8 assuming that fast following has greater financial impact – a two-year time lag for fast followers (among IST) and a contestable market share of 2.5% of total semiconductor revenue. Note that a contestable market share of 2.5% implies that all of the market share changes under all chipmaker investment "states of the world" are a factor of 1.67 (=2.5%/1.5%) larger in Scenarios #5.6 through #5.8 than in the corresponding market share changes in #Scenarios 5.2 through #5.4 (see Table 14). Additionally, for the interested reader, all of the above market share implications for the 1.5% and 2.5% contestable market shares assumed are tabulated in the 450mm model parameter list in Table 48 in Appendix B.

5.3.2 Industry Evidence Regarding the Nature of the Competition among Chipmakers

There is considerable evidence that economic reality in the semiconductor industry now resides somewhere in between purely intra-IST competition (Scenarios #5.2 and #5.6) and purely IST-to-smaller chipmaker competition (Scenarios #5.4 and #5.8).

Recent signs indicate that some market share competition will be intra-IST in character. It seems clear that there has been significant recent encroachment of Intel, Samsung, and TSMC on each

other's previously substantially disjoint addressable markets. Specifically, smart phone and tablets have undergone blistering growth, and all three chipmakers are significant players in manufacturing the chips (especially the microprocessors) which go into these devices. Relatedly, all three players now have a significant presence in the semiconductor foundry market, even though this was in the recent past solely TSMC's domain in the recent past (McGrath 8/21/12; Merritt 2/26/13). The latest vivid example of this market domain collision among IST are indications that Apple may be planning to split its next generation A7 processor (used in iPhones and iPads) chip production three ways between Intel, Samsung, and TSMC (DigiTimes 3/12/13).

There is also strong evidence that some of the competition for contestable market share (driven specifically by 450mm adoption) will be between IST and smaller chipmakers. In particular, wafer-size transitions in the past have led to significant chipmaker consolidation and are expected by industry analysts and participants to lead to further consolidation if 450mm comes to fruition (e.g., see Mack 8/20/12; Hutcheson 2013; Shilov 12/10/12).

It is uncertain exactly where the competition will really fall along this spectrum between intra-IST competition and IST-to-smaller-chipmaker competition. However, these two cases should bracket the actual reality and 50%/50% mix scenarios (Scenarios #5.3 and #5.7) are considered here for completeness.

5.4 Base Case Scenario Game Trees and Equilibrium Analysis

Given the assumptions made for payoff calculations, it is relatively straightforward to obtain estimates of chipmaker payoffs (again, measured in expected NPVs) of each player in each of the nine scenarios under each of the eight possible future states of the world. (For the interested reader, the full details of the firm payoff estimates including an example calculation can be found

in Appendix B). Figure 26 through Figure 34 below contain the payoffs calculated for Scenarios #5.0 through #5.8. The equilibrium results from these nine base case scenarios are also summarized in Table 15 below the nine game tree figures. For convenience, Intel is designated as Player 1, Samsung is designated as Player 2, and TSMC is designated at Player 3. Hence, when a strategy profile or payoff triplet of the three players is considered (e.g., ('Invest', 'Don't Invest', 'Invest') or ($4.7B, $3.2B, $1.3B)) the first entry in the triplet corresponds to Intel and so on.

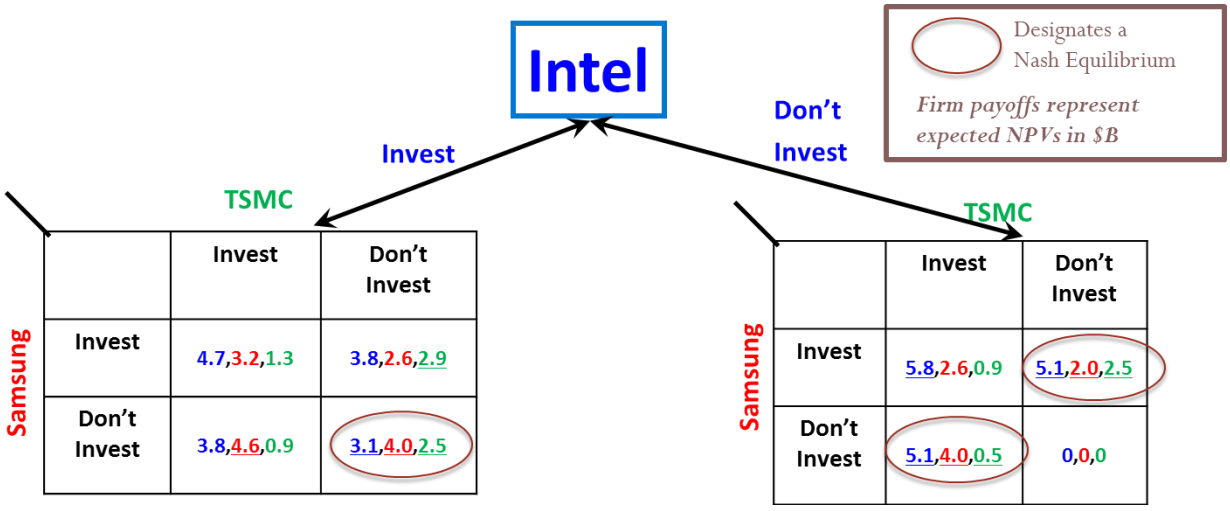


Figure 26: Game Tree for Scenario #5.0 (0 Year Time Lag; No Market Share Shifts)

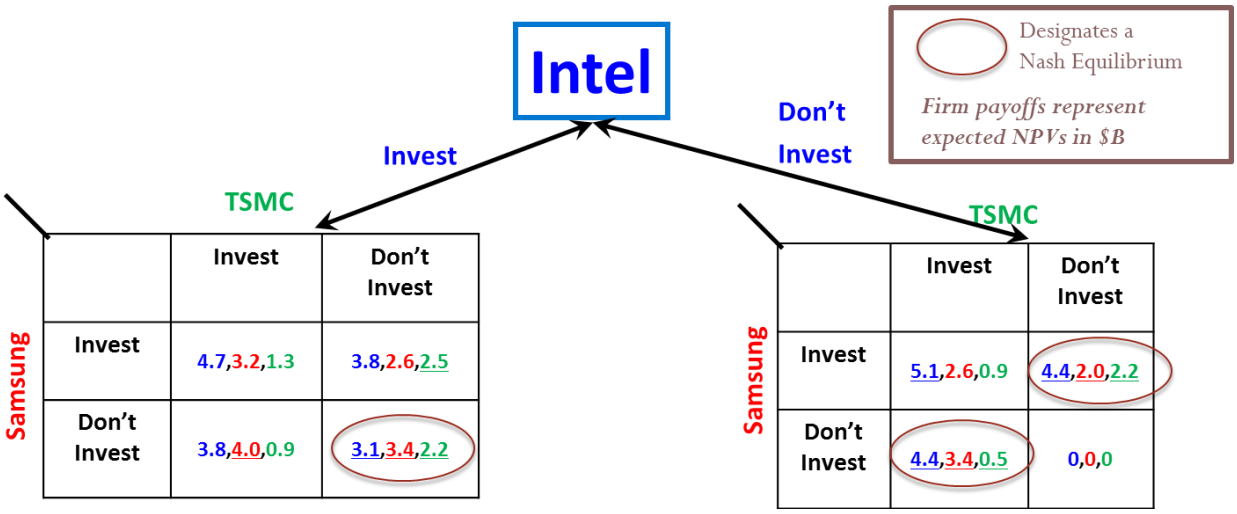


Figure 27: Game Tree for Scenario #5.1 (1 Year Time Lag; No Market Share Shifts)

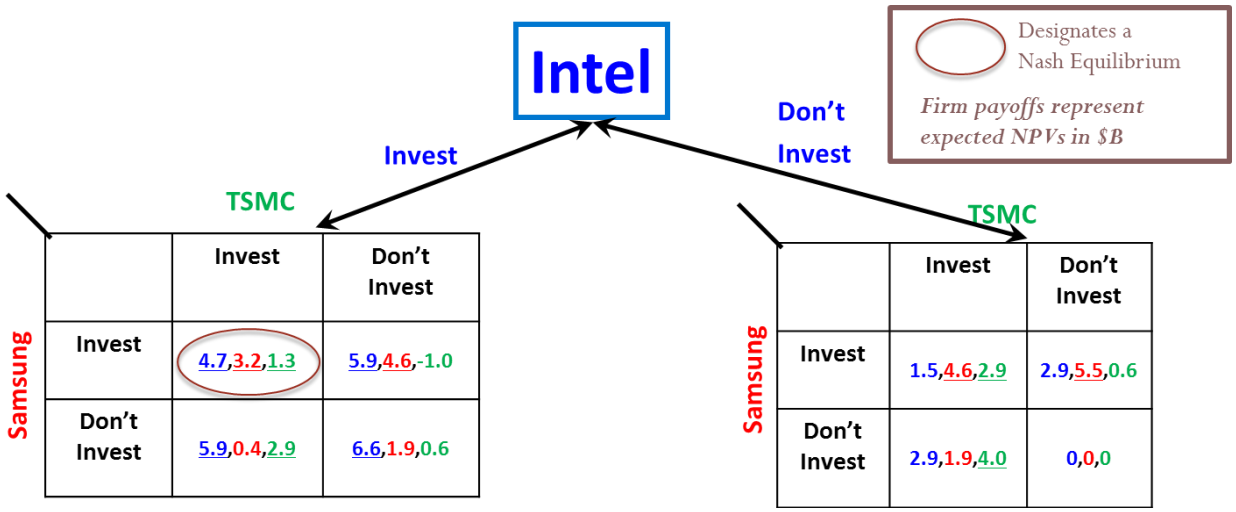


Figure 28: Game Tree for Scenario #5.2 (1 Year Time Lag; 1.5% Contestable Market Share; Competition Among IST)

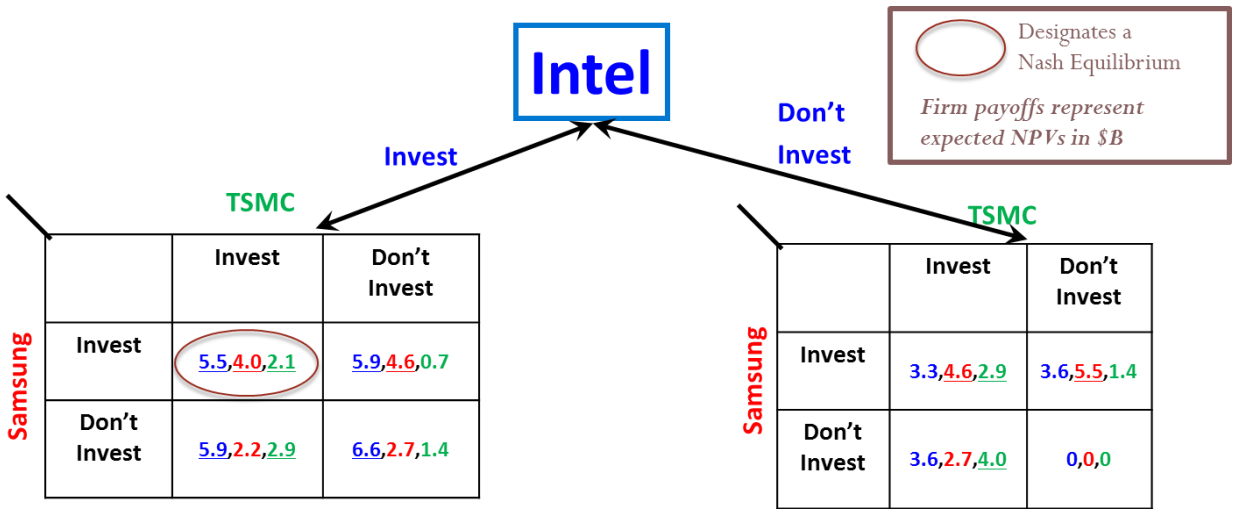


Figure 29: Game Tree for Scenario #5.3 (1 Year Time Lag; 1.5% Contestable Market Share; 50/50 Competition Split)

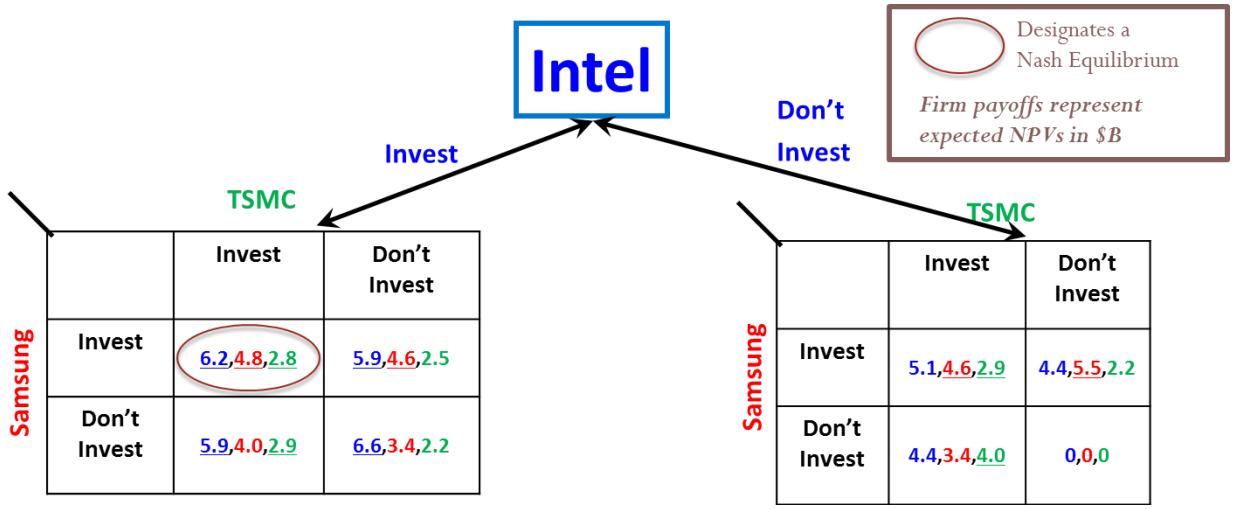


Figure 30: Game Tree for Scenario #5.4 (1 Year Time Lag; 1.5% Contestable Market Share; Competition between IST and Smaller Chipmakers)

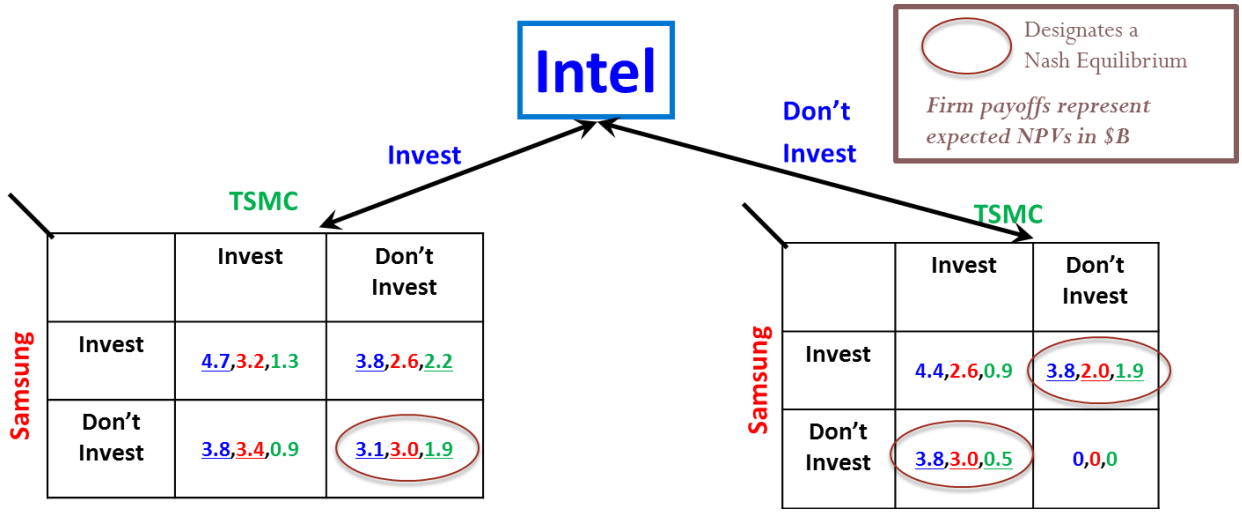


Figure 31: Game Tree for Scenario #5.5 (2 Year Time Lag; No Market Share Shifts)

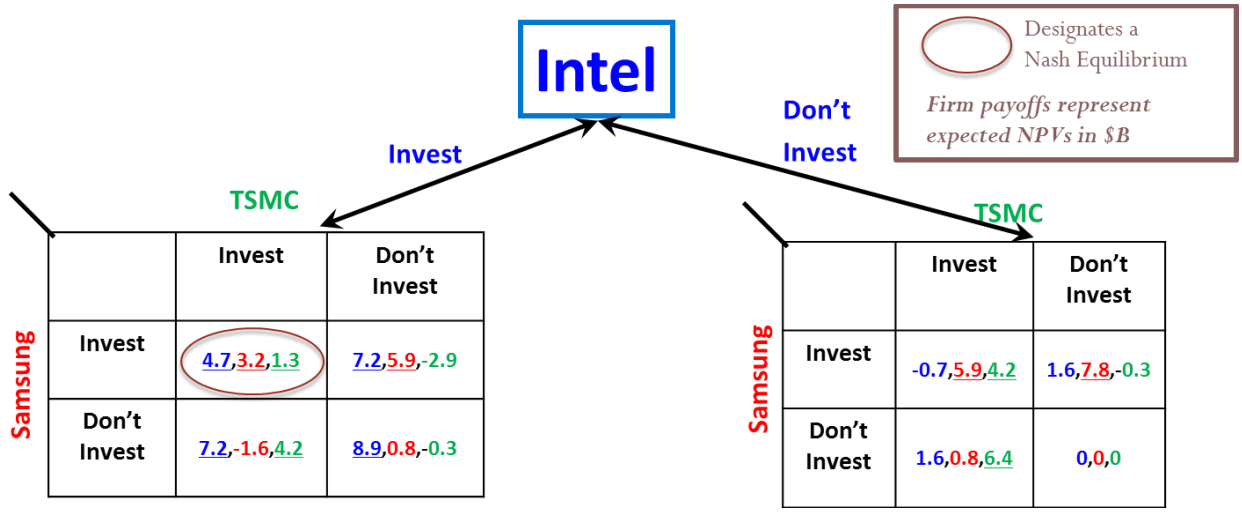


Figure 32: Game Tree for Scenario #5.6 (2 Year Time Lag; 2.5% Contestable Market Share; Competition Among IST)

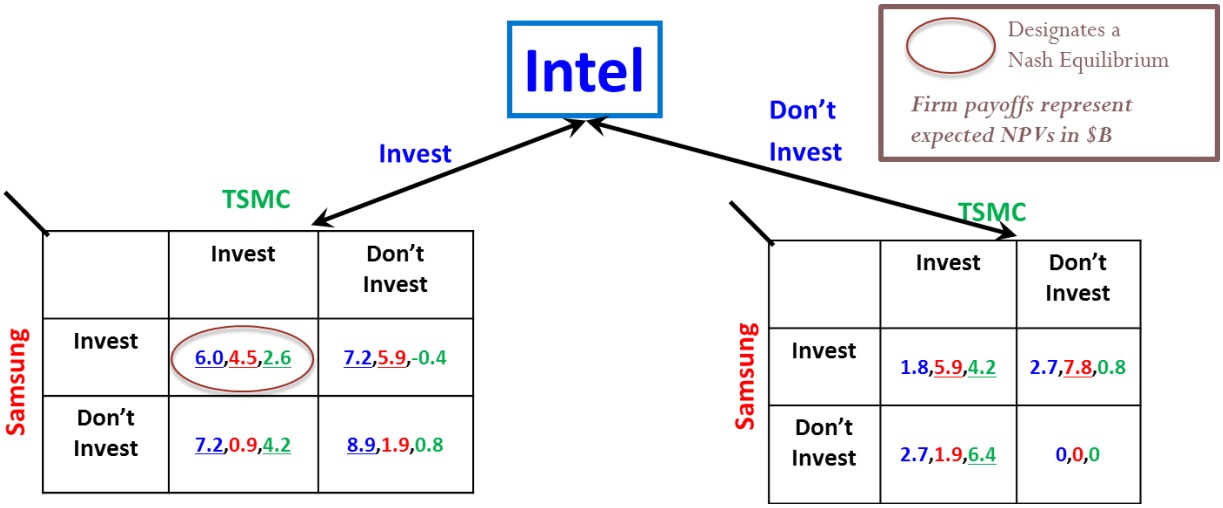


Figure 33: Game Tree for Scenario #5.7 (2 Year Time Lag; 2.5% Contestable Market Share; 50/50 Competition Split)

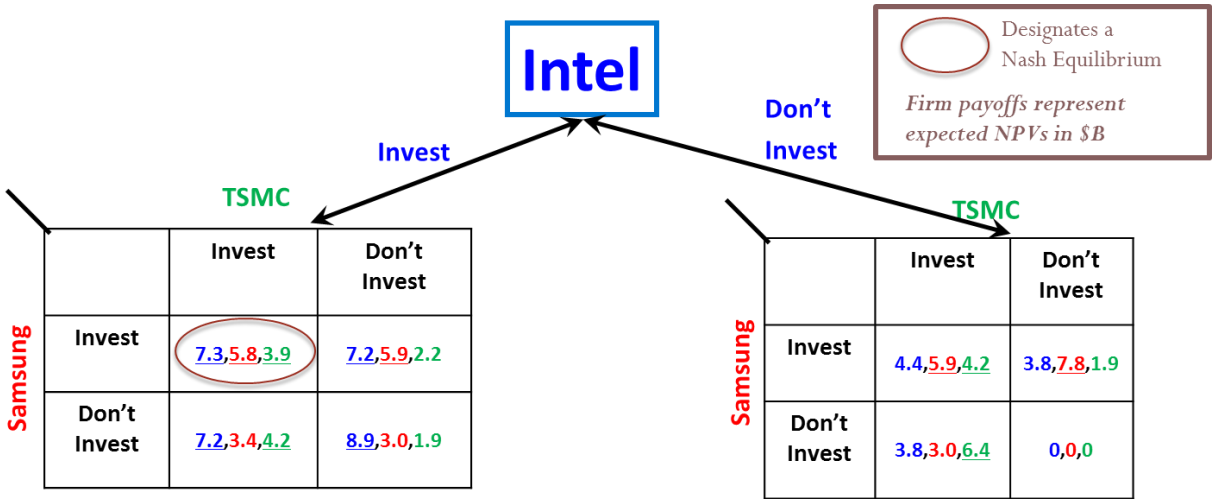


Figure 34: Game Tree for Scenario #5.8 (2 Year Time Lag; 2.5% Contestable Market Share; Competition between IST and Smaller Chipmakers)

Table 15: Summary of NE and Incentives for Chipmakers' NE Actions for Scenarios #5.0 through #5.8

Scenario:	Player	Player's Action in Nash Equilibrium (and Incentive for Individual Firms to Invest or Not Invest at the Equilibria)	Incentive to free-ride (when NE is non-unique)	Dominant Strategy? (Y/N)	*Scenario:*	Player	Player's Action in Nash Equilibrium (and Incentive for Individual Firms to Invest or Not Invest at the Equilibria)	Incentive to free-ride (when NE is non-unique)	Dominant Strategy? (Y/N)
Scenario #5.0: *- 0 Year Time Lag - 0% MS Contestable*	Intel	Inconclusive (3 PSNE, each with 1 chipmaker investing)	$2.0B	N					
	Samsung	Inconclusive (3 PSNE, each with 1 chipmaker investing)	$2.0B	N					
	TSMC	Inconclusive (3 PSNE, each with 1 chipmaker investing)	$2.0B	N					
Scenario #5.1: *- 1 Year Time Lag - 0% MS Contestable*	Intel	Inconclusive (3 PSNE, each with 1 chipmaker investing)	$1.3B	N	***Scenario #5.5:*** *- 2 Year Time Lag - 0% MS Contestable*	Intel	Inconclusive (3 PSNE, each with 1 chipmaker investing)	$0.7B	Y (only weakly)
	Samsung	Inconclusive (3 PSNE, each with 1 chipmaker investing)	$1.4B	N		Samsung	Inconclusive (3 PSNE, each with 1 chipmaker investing)	$1.0B	N
	TSMC	Inconclusive (3 PSNE, each with 1 chipmaker investing)	$1.7B	N		TSMC	Inconclusive (3 PSNE, each with 1 chipmaker investing)	$1.4B	N
Scenario #5.2: *- 1 Year Time Lag - 1.5% MS Contestable - Competition Among IST*	Intel	Invest (+$3.2B)		Y	***Scenario #5.6:*** *- 2 Year Time Lag - 2.5% MS Contestable - Competition Among IST*	Intel	Invest (+$5.4B)		Y
	Samsung	Invest (+2.8B)		Y		Samsung	Invest (+4.8B)		Y
	TSMC	Invest (+2.3B)		Y		TSMC	Invest (+4.2B)		Y
Scenario #5.3: *- 1 Year Time Lag - 1.5% MS Contestable - 50%/50% Competition Split*	Intel	Invest (+$2.2B)		Y	***Scenario #5.7:*** *- 2 Year Time Lag - 2.5% MS Contestable - 50%/50% Competition Split*	Intel	Invest (+4.2B)		Y
	Samsung	Invest (+1.8B)		Y		Samsung	Invest (+3.6B)		Y
	TSMC	Invest (+1.4B)		Y		TSMC	Invest (+3.0B)		Y
Scenario #5.4: *- 1 Year Time Lag - 1.5% MS Contestable - IST Competition with Smaller Chipmakers*	Intel	Invest (+$1.1B)		Y	***Scenario #5.8:*** *- 2 Year Time Lag - 2.5% MS Contestable - IST Competition with Smaller Chipmakers*	Intel	Invest (+2.9B)		Y
	Samsung	Invest (+0.8B)		Y		Samsung	Invest (+2.4B)		Y
	TSMC	Invest (+0.3B)		Y		TSMC	Invest (+$1.7B)		Y

5.4.1 General Discussion of Base Case 450mm Scenario Equilibria

One simple observation stemming from Table 15 is that although the form of the NE differ from scenario to scenario (and in some case include multiple equilibria, leading to ambiguous prediction), none of the pure strategy Nash Equilibria (PSNE) in the nine base case scenarios consisted of all three players choosing not to invest (i.e., a [‘Don’t Invest’, ‘Don’t Invest’, ‘Don’t Invest’] outcome). This is consistent with the general observation in the industry that the large chipmakers are really quite unambiguous in their desire to have 450mm wafer technology come to fruition (Lapedus 1/24/11; Lapedus 4/6/11; Mack 8/20/12). The manufacturing cost savings are tremendous for those chipmakers which are able to afford the R&D and capital costs associated with the technology, not to mention any opportunity for market share gain for the large chipmakers associated with the transition.

Because the chipmaker benefits derived are asymmetric manufacturing cost savings (a fixed fraction of the asymmetric annual COGS estimates assumed for each IST chipmaker) and symmetric assumptions regarding market share gains and losses, the overall net benefit of 450mm is asymmetric between Intel, Samsung, and TSMC. Table 12 (with data sources cataloged in Table 48) shows that Intel is assumed to have the highest annual estimated COGS, while TSMC is assumed to have the lowest. Looking holistically at Figure 26 through Figure 34 and Table 15, this ordering reflects itself in the general trend that TSMC has the weakest incentives to invest in 450mm, while Intel tends to have the most robust incentives to invest in 450mm technology.

Additionally it is clear that even modest amounts of contestable semiconductor market share (especially among IST) can generate very strong incentives for each of the three players to invest. This general observation will be explored in much greater detail in the next few sections.

5.4.2 Comparison of Scenarios with No Contestable Semiconductor Market Share

The scenarios with no contestable market share, Scenarios #5.0, #5.1, and #5.5, are inconclusive in the sense that they each have three PSNE (corresponding to the three outcomes in which only one of the chipmakers chooses to invest), and thus lack a clear outcome prediction. However, it is possible to compare the outcome payoffs in each of these three "go it alone" states of the world. Given the model payoff estimates, it is clear that these equilibrium outcomes represent attempts/desires to free-ride on the part of the two chipmakers who do not invest in each of the PSNE (in the sense that a non-investing chipmaker receives a higher payoff than it would in the equilibrium in which it is the one who invests). Under the assumptions of the model, this free-riding benefit is the same for a given chipmaker regardless of which other chipmaker is the one who decides to invest (again, when we restrict our attention to the three "go it alone" PSNE outcomes). This fact is easily verifiable by checking the relevant payoff estimates in Figure 26, Figure 27, and Figure 31. Hence, I have tabulated the "incentive to free-ride" (i.e., the difference in a chipmaker's payoffs among the three PSNE when it doesn't invest vs. when it does invest) in Table 15 for each player in each of those three inconclusive scenarios.

Comparing the chipmakers' incentives to free-ride, we can see clear (and expected) trends. Firstly, in Scenario #5.0, the incentives to free ride are exactly $2.0B, the amount of each chipmaker investment assumed (see Table 13). This makes sense given that in this scenario no *additional* manufacturing cost savings or market share benefit is conferred to any chipmaker who

decides to invest $2B to help finance 450mm equipment development. However, in Scenario #5.1 , where a one-year time lag is assumed for non-investing chipmakers (with no market share shifts), the incentives to free-ride decrease to $1.3B for Intel, $1.4B for Samsung, and $1.7B for TSMC. Furthermore, in Scenario #5.5, where a two-year time lag is assumed for non-investing chipmakers (with no market share shifts), the incentives to free-ride decrease even further to $0.7B for Intel, $1.0B for Samsung, and $1.4B for TSMC. This trend is as one would expect: the bigger the penalty for not investing, the smaller the incentive to free-ride on the 450mm investment of other chipmakers.

Finally, it is interesting to note that in Scenario #5.0, the total E(NPV) surplus is maximized in any of these three "go it alone" NE where free-riding is occurring (which can be seen by comparing the sum of three players' payoffs for each outcome). This occurs because when no manufacturing cost savings fast-following lags occur, once a single IST firm invests $2B, from the standpoint of IST as a whole, the additional acceleration of the availability of 450mm equipment by one year (if one additional IST firm invests $2B) or by two years (if both additional IST firms each invest $2B) does not generate enough benefit to justify the additional investment(s). Contrariwise, in Scenario #5.1 between $0.5B and $0.9B of total E(NPV) IST surplus is being left on the table in the "go it alone" equilibria compared to the "all invest" outcome, and in Scenario #5.5 between $1.2B and $1.9B is being left on the table in the "go it alone" equilibria compared to the "all invest" outcome. These results imply that when there is a time lag penalty for manufacturing cost savings, it would be more beneficial for IST in a holistic sense to have each firm invest early in 450mm technology. (However, the "all invest" outcome is not a Nash Equilibrium.)

5.4.3 Comparison of Scenarios as Nature of Market Share Competition Changes

From Table 15, as comports with intuition, we see that as market share competition becomes more intensely intra-IST (while keeping the net fraction of semiconductor industry market share which is contestable fixed), the equilibrium incentives to invest in 450mm generally increase for the three players. This can be seen by comparing the equilibrium outcomes (and corresponding E(NPV) incentives) across Scenario #5.2 through #5.4 and separately by comparing the equilibrium outcomes and E(NPV) incentives across Scenario #5.6 through #5.8. In both comparisons, although the NE outcome of the game remains all three players investing, when the nature of the competition becomes more intensely IST-to-smaller chipmakers (i.e., Scenarios #5.4 and #5.8), the incentive for each of the IST companies to invest weakens dramatically. This is a straightforward consequence of the fact that although the net semiconductor market share fraction which is contestable is held fixed, the amount of share potentially at stake for each player is higher in the scenarios where the competition is oriented *among* Intel, Samsung, and TSMC (see Table 14 for details). A straightforward and practical consequence of this trend is that the more that each IST player believe that significant market share among the three players is at stake, the more likely it is that each IST player will decide to invest early in 450mm technology (while keeping in mind that other players beliefs about the nature of the competition is relevant too).

One can also compare the NE outcomes across the scenarios in left and right halves of Table 15. These comparisons are based on the differences in the linked assumptions regarding time lag and contestable market share (keeping the relative composition of the contestable market share competition fixed) as described in Section 5.3 above. As one would expect, these comparisons indicate a greater incentive to invest as time lags for fast followers (i.e., non-investors) and the

amount of contestable semiconductor market share increase. Clearly, these two factors represent greater "penalties" for non-investors in 450mm technology. One strategic implication here is that early investing firms *might consider* employing those mechanisms which increase the penalties for non-investors (such access to the first 450mm equipment produced for early investors and, perhaps, a proprietary "lock out" period for non-investors). I hasten to add that such strategies must be carefully scrutinized because the calculations in this model do not incorporate learning curve cost reductions at the equipment suppliers (based on cumulative 450mm equipment sales/production). It is not difficult to see that forgone learning curve cost reduction benefits for equipment suppliers, if large enough, could overwhelm the early-adopter chipmaker benefits from a proprietary "lock out" period for access to 450mm equipment.

5.5 Parameter Sensitivity Analysis for 450mm Model

Now that we have gone through a detailed analysis of the base case 450mm model analysis scenarios, let us explore these outcomes and strategic conclusions even further by performing sensitivity analyses on a number of the key model parameters. I performed the sensitivity analysis somewhat differently for the 450mm model results than for the EUVL model because of the inherent differences in players, game structures, and payoff calculations. Because there is less financial and positional asymmetry among the three players than in the EUVL model, I have focused less on the implications of $E(NPV)_{invest}$ vs. $E(NPV)_{don't\ invest}$ difference and ratio analysis in the 450mm model. Additionally, in lieu of the low-medium-high parameter evaluation and parameter cutoff analysis performed for the EUVL model in Chapter 4, here I have swept key parameters (one-at-a-time) through broad ranges to evaluate how the NE are impacted. The results of these sensitivity analyses are shown in Table 16 through Table 22 below.

Table 16: Impact of 'Chipmaker Investment Amount' on NE of 450mm Game Outcomes

Amount of 450mm R&D investment required by (each) Chipmaker ($B)	**Pure Strategy Nash Equilibria (all other parameters at Base Case values) for Scenario:**								
	#5.0	***#5.1***	***#5.2***	***#5.3***	***#5.4***	***#5.5***	***#5.6***	***#5.7***	***#5.8***
0.5	(I,I,D)	(I,I,I)	(I,I,I)	(I,I,I)	(I,I,I)	(I,I,I)	(I,I,I)	(I,I,I)	(I,I,I)
1.0	(I,D,D); (D,I,D); (D,D,I)	(I,I,D)	(I,I,I)	(I,I,I)	(I,I,I)	(I,I,I)	(I,I,I)	(I,I,I)	(I,I,I)
1.5	(I,D,D); (D,I,D); (D,D,I)	(I,D,D); (D,I,D); (D,D,I)	(I,I,I)	(I,I,I)	(I,I,I)	(I,I,D)	(I,I,I)	(I,I,I)	(I,I,I)
2.0	***(I,D,D); (D,I,D); (D,D,I)***	***(I,D,D); (D,I,D); (D,D,I)***	***(I,I,I)***	***(I,I,I)***	***(I,I,I)***	***(I,D,D); (D,I,D); (D,D,I)***	***(I,I,I)***	***(I,I,I)***	***(I,I,I)***
2.5	(I,D,D); (D,I,D)	(I,D,D); (D,I,D)	(I,I,I)	(I,I,I)	(I,I,D)	(I,D,D); (D,I,D)	(I,I,I)	(I,I,I)	(I,I,I)
3.0	(I,D,D); (D,I,D)	(I,D,D); (D,I,D)	(I,I,I)	(I,I,I)	(I,I,D)	(I,D,D); (D,I,D)	(I,I,I)	(I,I,I)	(I,I,I)
3.5	(I,D,D); (D,I,D)	(I,D,D); (D,I,D)	(I,I,I)	(I,I,D)	(I,D,D); (D,I,D); (D,D,I)	(I,D,D); (D,I,D)	(I,I,I)	(I,I,I)	(I,I,I)
4.0	(I,D,D)	(I,D,D); (D,I,D)	(I,I,I)	(I,D,D)	(I,D,D); (D,I,D); (D,D,I)	(I,D,D)	(I,I,I)	(I,I,I)	(I,I,D)
4.5	(I,D,D)	(I,D,D)	(I,I,I)	(I,D,D); (D,I,D); (D,D,I)	(I,D,D); (D,I,D); (D,D,I)	(I,D,D)	(I,I,I)	(I,I,I)	(I,I,D)
5.0	(I,D,D)	(I,D,D)	(I,D,D); (D,I,D); (D,D,I)	(I,D,D); (D,I,D); (D,D,I)	(I,D,D); (D,I,D); (D,D,I)	(I,D,D)	(I,I,I)	(I,I,D)	(I,D,D)

Table 17: Impact of 'Fraction of 450mm Wafer COGS Savings' on NE of 450mm Game Outcomes

Fraction of COGS savings as a result of 450mm wafer processing	**Pure Strategy Nash Equilibria (all other parameters at Base Case values) for Scenario:**								
	#5.0	***#5.1***	***#5.2***	***#5.3***	***#5.4***	***#5.5***	***#5.6***	***#5.7***	***#5.8***
5%	(D,D,D)	(D,D,D)	(I,I,I)	(I,I,I)	(I,I,D); (I,D,I); (D,I,I)	(D,D,D)	(I,I,I)	(I,I,I)	(I,I,I)
10%	(I,D,D)	(I,D,D)	(I,I,I)	(I,I,I)	(I,I,D)	(I,D,D)	(I,I,I)	(I,I,I)	(I,I,I)
15%	(I,D,D); (D,I,D)	(I,D,D); (D,I,D)	(I,I,I)	(I,I,I)	(I,I,I)	(I,D,D); (D,I,D)	(I,I,I)	(I,I,I)	(I,I,I)
20%	***(I,D,D); (D,I,D); (D,D,I)***	***(I,D,D); (D,I,D); (D,D,I)***	***(I,I,I)***	***(I,I,I)***	***(I,I,I)***	***(I,D,D); (D,I,D); (D,D,I)***	***(I,I,I)***	***(I,I,I)***	***(I,I,I)***
25%	(I,D,D); (D,I,D); (D,D,I)	(I,D,D); (D,I,D); (D,D,I)	(I,I,I)	(I,I,I)	(I,I,I)	(I,I,D)	(I,I,I)	(I,I,I)	(I,I,I)
30%	(I,D,D); (D,I,D); (D,D,I)	(I,D,D)	(I,I,I)	(I,I,I)	(I,I,I)	(I,I,D)	(I,I,I)	(I,I,I)	(I,I,I)
35%	(I,D,D); (D,I,D); (D,D,I)	(I,D,D)	(I,I,I)	(I,I,I)	(I,I,I)	(I,I,D)	(I,I,I)	(I,I,I)	(I,I,I)
40%	(I,D,D); (D,I,D); (D,D,I)	(I,D,D)	(I,I,I)	(I,I,I)	(I,I,I)	(I,I,I)	(I,I,I)	(I,I,I)	(I,I,I)

Table 18: Impact 'Ending Date of Analysis' on NE of 450mm Game Outcomes

Ending Date for analysis (i.e., for 450mm benefit flows)	**Pure Strategy Nash Equilibria (all other parameters at Base Case values) for Scenario:**								
	#5.0	***#5.1***	***#5.2***	***#5.3***	***#5.4***	***#5.5***	***#5.6***	***#5.7***	***#5.8***
2021	(I,D,D)	(I,D,D)	(I,I,I)	(I,I,I)	(I,I,D)	(I,D,D)	(I,I,I)	(I,I,I)	(I,I,I)
2026	(I,D,D); (D,I,D)	(I,D,D); (D,I,D)	(I,I,I)	(I,I,I)	(I,I,I)	(I,D,D)	(I,I,I)	(I,I,I)	(I,I,I)
2031	***(I,D,D); (D,I,D); (D,D,I)***	***(I,D,D); (D,I,D); (D,D,I)***	***(I,I,I)***	***(I,I,I)***	***(I,I,I)***	***(I,D,D); (D,I,D); (D,D,I)***	***(I,I,I)***	***(I,I,I)***	***(I,I,I)***
2036	(I,D,D); (D,I,D); (D,D,I)	(I,D,D); (D,I,D); (D,D,I)	(I,I,I)	(I,I,I)	(I,I,I)	(I,D,D)	(I,I,I)	(I,I,I)	(I,I,I)
2041	(I,D,D); (D,I,D); (D,D,I)	(I,D,D); (D,I,D); (D,D,I)	(I,I,I)	(I,I,I)	(I,I,I)	(I,D,D)	(I,I,I)	(I,I,I)	(I,I,I)

Table 19: Impact of 'Time Lag to Start of Benefits for Early Adopters' on NE of 450mm Game Outcomes

Time lag to start of benefits for early adopters (where the triplet represents results for (3 early investors, 2 early investors, 1 early investor))	**Pure Strategy Nash Equilibria (all other parameters at Base Case values) for Scenario:**								
	#5.0	***#5.1***	***#5.2***	***#5.3***	***#5.4***	***#5.5***	***#5.6***	***#5.7***	***#5.8***
(4,5,6) years	(I,D,D); (D,I,D); (D,D,I)	(I,D,D); (D,I,D); (D,D,I)	(I,I,I)	(I,I,I)	(I,I,I)	(I,D,D)	(I,I,I)	(I,I,I)	(I,I,I)
(5,6,7) years	***(I,D,D); (D,I,D); (D,D,I)***	***(I,D,D); (D,I,D); (D,D,I)***	***(I,I,I)***	***(I,I,I)***	***(I,I,I)***	***(I,D,D); (D,I,D); (D,D,I)***	***(I,I,I)***	***(I,I,I)***	(I,I,I)
(6,7,8) years	(I,D,D); (D,I,D); (D,D,I)	(I,D,D); (D,I,D); (D,D,I)	(I,I,I)	(I,I,I)	(I,I,I)	(I,D,D); (D,I,D); (D,D,I)	(I,I,I)	(I,I,I)	(I,I,I)
(7,8,9) years	(I,D,D); (D,I,D)	(I,D,D); (D,I,D)	(I,I,I)	(I,I,I)	(I,I,D)	(I,D,D); (D,I,D)	(I,I,I)	(I,I,I)	(I,I,I)
(8,9,10) years	(I,D,D); (D,I,D)	(I,D,D); (D,I,D)	(I,I,I)	(I,I,I)	(I,I,D)	(I,D,D); (D,I,D)	(I,I,I)	(I,I,I)	(I,I,I)

Table 20: Impact of 'Discount Rate' on NE of 450mm Game Outcomes

Discount rate	**Pure Strategy Nash Equilibria (all other parameters at Base Case values) for Scenario:**								
	#5.0	***#5.1***	***#5.2***	***#5.3***	***#5.4***	***#5.5***	***#5.6***	***#5.7***	***#5.8***
8 %	(I,D,D); (D,I,D); (D,D,I)	(I,D,D); (D,I,D); (D,D,I)	(I,I,I)	(I,I,I)	(I,I,I)	(I,I,D)	(I,I,I)	(I,I,I)	(I,I,I)
10 %	(I,D,D); (D,I,D); (D,D,I)	(I,D,D); (D,I,D); (D,D,I)	(I,I,I)	(I,I,I)	(I,I,I)	(I,D,D)	(I,I,I)	(I,I,I)	(I,I,I)
12 %	***(I,D,D); (D,I,D); (D,D,I)***	***(I,D,D); (D,I,D); (D,D,I)***	***(I,I,I)***	***(I,I,I)***	***(I,I,I)***	***(I,D,D); (D,I,D); (D,D,I)***	***(I,I,I)***	***(I,I,I)***	(I,I,I)
14 %	(I,D,D); (D,I,D); (D,D,I)	(I,D,D); (D,I,D); (D,D,I)	(I,I,I)	(I,I,I)	(I,I,I)	(I,D,D); (D,I,D); (D,D,I)	(I,I,I)	(I,I,I)	(I,I,I)
16 %	(I,D,D); (D,I,D)	(I,D,D); (D,I,D)	(I,I,I)	(I,I,I)	(I,I,D)	(I,D,D); (D,I,D)	(I,I,I)	(I,I,I)	(I,I,I)
18 %	(I,D,D); (D,I,D)	(I,D,D); (D,I,D)	(I,I,I)	(I,I,I)	(I,D,D)	(I,D,D); (D,I,D)	(I,I,I)	(I,I,I)	(I,I,I)
20%	(I,D,D)	(I,D,D)	(I,I,I)	(I,I,D)	(I,D,D); (D,I,D); (D,D,I)	(I,D,D)	(I,I,I)	(I,I,I)	(I,I,I)

Table 21: Impact of 'Additional Time Lag for Fast Followers' on NE of 450mm Game Outcomes

Additional time lag to start of benefits for fast followers	**Pure Strategy Nash Equilibria (all other parameters at Base Case values) for Scenario:**								
	#5.0	***#5.1***	***#5.2***	***#5.3***	***#5.4***	***#5.5***	***#5.6***	***#5.7***	***#5.8***
0 years	***(I,D,D); (D,I,D); (D,D,I)***	(I,D,D); (D,I,D); (D,D,I)	(I,I,I)	(I,I,I)	(I,I,D)	(I,D,D); (D,I,D); (D,D,I)	(I,I,I)	(I,I,I)	(I,I,I)
1 years	(I,D,D); (D,I,D); (D,D,I)	***(I,D,D); (D,I,D); (D,D,I)***	***(I,I,I)***	***(I,I,I)***	***(I,I,I)***	(I,D,D); (D,I,D); (D,D,I)	(I,I,I)	(I,I,I)	(I,I,I)
2 years	(I,D,D)	(I,D,D)	(I,I,I)	(I,I,I)	(I,I,I)	***(I,D,D); (D,I,D); (D,D,I)***	***(I,I,I)***	***(I,I,I)***	***(I,I,I)***
3 years	(I,I,D)	(I,I,D)	(I,I,I)	(I,I,I)	(I,I,I)	(I,I,D)	(I,I,I)	(I,I,I)	(I,I,I)
4 years	(I,I,D)	(I,I,D)	(I,I,I)	(I,I,I)	(I,I,I)	(I,I,D)	(I,I,I)	(I,I,I)	(I,I,I)

Table 22: Impact of 'Market Share at Stake' on NE of 450mm Game Outcomes

Fraction of overall semiconductor market share which is contestable (once 450mm cost savings commence)	**Pure Strategy Nash Equilibria (all other parameters at Base Case values) for Scenario:**								
	#5.0	***#5.1***	***#5.2***	***#5.3***	***#5.4***	***#5.5***	***#5.6***	***#5.7***	***#5.8***
0.0%	***(I,D,D); (D,I,D); (D,D,I)***	(I,D,D); (D,I,D); (D,D,I)	(I,D,D); (D,I,D); (D,D,I)	(I,D,D); (D,I,D); (D,D,I)	(I,D,D); (D,I,D); (D,D,I)	(I,D,D); (D,I,D); (D,D,I)	(I,D,D)	(I,D,D)	(I,D,D)
0.5%	(I,D,D); (D,I,D); (D,D,I)	(I,D,D); (D,I,D); (D,D,I)	(I,I,D)	(I,I,D)	(I,D,D)	(I,D,D); (D,I,D); (D,D,I)	(I,I,I)	(I,I,D)	(I,I,D)
1.0%	(I,D,D); (D,I,D); (D,D,I)	(I,D,D); (D,I,D); (D,D,I)	(I,I,I)	(I,I,I)	(I,I,D)	(I,D,D); (D,I,D); (D,D,I)	(I,I,I)	(I,I,I)	(I,I,I)
1.5%	(I,D,D); (D,I,D); (D,D,I)	***(I,D,D); (D,I,D); (D,D,I)***	***(I,I,I)***	***(I,I,I)***	***(I,I,I)***	(I,D,D); (D,I,D); (D,D,I)	(I,I,I)	(I,I,I)	(I,I,I)
2.0%	(I,D,D); (D,I,D); (D,D,I)	(I,D,D); (D,I,D); (D,D,I)	(I,I,I)	(I,I,I)	(I,I,I)	(I,D,D); (D,I,D); (D,D,I)	(I,I,I)	(I,I,I)	(I,I,I)
2.5%	(I,D,D); (D,I,D); (D,D,I)	(I,D,D); (D,I,D); (D,D,I)	(I,I,I)	(I,I,I)	(I,I,I)	***(I,D,D); (D,I,D); (D,D,I)***	***(I,I,I)***	***(I,I,I)***	***(I,I,I)***
3.0%	(I,D,D); (D,I,D); (D,D,I)	(I,D,D); (D,I,D); (D,D,I)	(I,I,I)	(I,I,I)	(I,I,I)	(I,D,D); (D,I,D); (D,D,I)	(I,I,I)	(I,I,I)	(I,I,I)
3.5%	(I,D,D); (D,I,D); (D,D,I)	(I,D,D); (D,I,D); (D,D,I)	(I,I,I)	(I,I,I)	(I,I,I)	(I,D,D); (D,I,D); (D,D,I)	(I,I,I)	(I,I,I)	(I,I,I)

	#5.0	#5.1	#5.2	#5.3	#5.4	#5.5	#5.6	#5.7	#5.8
4.0%	(I,D,D); (D,I,D); (D,D,I)	(I,D,D); (D,I,D); (D,D,I)	(I,I,I)	(I,I,I)	(I,I,I)	(I,D,D); (D,I,D); (D,D,I)	(I,I,I)	(I,I,I)	(I,I,I)
4.5%	(I,D,D); (D,I,D); (D,D,I)	(I,D,D); (D,I,D); (D,D,I)	(I,I,I)	(I,I,I)	(I,I,I)	(I,D,D); (D,I,D); (D,D,I)	(I,I,I)	(I,I,I)	(I,I,I)
5.0%	(I,D,D); (D,I,D); (D,D,I)	(I,D,D); (D,I,D); (D,D,I)	(I,I,I)	(I,I,I)	(I,I,I)	(I,D,D); (D,I,D); (D,D,I)	(I,I,I)	(I,I,I)	(I,I,I)

5.5.1 Discussion of 450mm Model Parameter Sensitivity Analysis

Scrutinizing the sensitivity analyses shown in Table 16 through Table 22 above gives rise to several general observations regarding the 450mm model outcomes.

First, across almost all of the broad parameter variations considered here, the observation made in Section 5.4.1 that the base case scenarios never lead to the "No Investment" equilibrium outcome (i.e., ['Don't Invest', 'Don't Invest', 'Don't Invest]) is upheld under virtually all circumstances. In fact, the only exception to this can be found when the COGS savings due to 450mm manufacturing is pushed all the way down to 5% *and* no market share is assumed contestable. Individually, these two assumptions are unlikely, and jointly they are extremely unlikely. Thus, the sensitivity analysis predicts that one or more large chipmaker is likely to invest in 450mm technology given the other modeling assumptions made.

Second, the observation made in Section 5.4.3 that the intra-IST competition for MS (driven differentially by 450mm technology) is a strong lubricant for investment is further strengthened by the sensitivity analysis results. For a number of model parameters the ('Invest', 'Invest', 'Invest') equilibrium outcome was obtained across the whole parameter range evaluated when intra-IST competition prevailed (e.g., Scenarios #5.2 and #5.6).

In addition to those general observations, observations specific to each of the sensitivity analyses for each model parameter examined are shown in Table 23 below.

Table 23: Summary of Sensitivity Analyses across Key Model Parameters

Parameter varied:	**Observations**
(Individual) Chipmaker Investment Amount	• The magnitude of the chipmaker investment has a strong impact on the NE outcomes. With intense intra-IST competition, the (I,I,I) equilibrium is maintained for high chipmaker investment amounts, but as competition becomes more fully IST-to-smaller chipmakers, greater ambiguity arises regarding which chipmakers are likely to invest early in 450mm technology.
Fraction of 450mm Wafer COGS Savings	• Only parameter which produces (D,D,D) outcome within the ranges analyzed (and only for the 5% COGS reduction number) • As expected, a higher COGS savings percentage induces more certain chipmaker investment • Any significant intra-IST competition induces the (I,I,I) NE outcome
Ending Date of Analysis	• Virtually no impact on the NE outcomes (in fact the only impacts to the NE outcome show up for the very short time horizon of 10 years, corresponding to an end of the analysis in 2021)
Time Lag to Start of Benefits for Early Adopters	• Relatively modest impact on the NE outcomes (for those scenarios with non-zero contestable market share, shorter durations induce more certain investment by all three chipmakers)
Additional Time Lag for Fast Followers	• Moderate impact on the NE outcomes (A longer time lag induces more certain chipmaker investment). Most of the NE in the non-zero market share scenarios are (I,I,I), however Table 15 clearly illustrates the significant increases in the incentive against being a laggard as the time lag lengthens.
Discount Rate	• Moderate impact on the NE outcomes. As expected, higher discount rates corresponds to incentives for chipmaker investment. In Scenarios #5.3 and #5.4 Samsung and TSMC have their incentive to invest vanish at some of the higher discount rates, while Intel's incentive to invest remains positive through the entire range of discount rates evaluated (8%-20%).
Contestable Market Share at Stake	• Strong impact of contestable market share on the NE outcomes. As expected, larger contestable market share leads to more certain chipmaker investment. Greater intra-IST competition has the strongest impact on NE outcomes.

5.6 450mm Model Variants, Limitations, and Future Work

Now that we have provided a detailed sensitivity analysis on the 450mm model outcomes, let us spend some time discussing other possible strategic situations to which modified versions of the model could be applied, factors which are not captured by the model, and potentially fruitful avenues for developing this modeling work further.

5.6.1 Other Potential Variants of the 450mm Model

Examine asymmetrically-sized investments by the chipmakers (e.g., investments proportional to the chipmakers "effective revenues" which would still total $6B if all three chipmakers chose to invest heavily early). If one maintains the same assumptions regarding the start dates of chipmakers' benefits (see Table 13 above), one might argue that larger financial amounts from chipmakers should have more influence on the timing of 450mm development. However, Intel, Samsung, and TSMC are all large chipmakers (in some sense, they currently represent very roughly equally sized market opportunities for the equipment suppliers, with perhaps TSMC being a bit smaller than the other two [see Notebookcheck 3/28/13]), and each chipmaker among IST choosing to invest will send a strong signal of earnestness to the equipment supplier regarding the large chipmakers' desire for a timely introduction of 450mm technology. Thus, introducing somewhat asymmetrical IST investment amounts while maintaining symmetric IST timing impacts on 450mm HVM equipment availability is a scenario worthy of examination. One expects that such analysis would even out the net incentives for Intel, Samsung, and TSMC to invest in 450mm, perhaps shifting the equilibrium outcomes found toward more (but likely not fully) symmetric investment outcomes. Early attempts were made to test out a model with fixed total chipmaker investment in 450mm technology assuming at least one chipmaker chose to invest (along with fixed HVM equipment introduction dates), but this approach was deemed less

realistic in terms of the actual possibilities of chipmaker financial support for 450mm technology (not to mention inducing shifts in the investment magnitude for each chipmaker depending on the actions of the others, a dubious assumption in a game which is formulated as fully simultaneous).

Assume non-zero revenue growth rate for the size of the (450mm-fabricated) semiconductor market. This growth is hard to predict, and thus was not incorporated into the current model. In addition to this concern, given the other model assumptions, similar effects on investment equilibria of an increased semiconductor revenue growth rate can be expected from varying other model parameters which also would increase chipmaker benefits from 450mm technology (e.g., increasing the percentage of COGS savings from 450mm technology or increasing the length of the time horizon used for the 450mm benefit analysis).

Assume differing revenue and/or COGS growth rates among the three chipmakers. Again, these growth rates are hard to predict. However, one could test out differing assumptions of market demand predictions for each of the three chipmakers. One simple possibility would be to assume that the three chipmakers would progress to become relatively symmetric players in the semiconductor market (in terms of market shares, profit margins, COGS, etc.). If so, then the equilibrium outcomes of the 450mm model would become symmetric with respect to the three chipmakers as well.

Examine scenarios involving more complex bundles of model input parameters. For example, although I have (in the base case analysis in Section 5.4) examined scenarios with correlated pairs of assumptions for the time lag for fast followers and the size of contestable semiconductor market share, one might suspect that the percentage of COGS reduction also co-varies along with

these two parameters. One's expectations might be: the longer the lag for fast followers (along with higher contestable market share), the harder 450mm technology is to implement, thus implying a lower overall reduction in COGS for chipmakers once 450mm technology is implemented. These more complex bundles of parameter changes could become quite nuanced and should be pursued only after the base case analyses have been more fully vetted by industry experts.

5.6.2 Key Factors Not Accounted for in the 450mm Model

Macroeconomic uncertainty and future levels of consolidation among chipmakers. It could be cogently argued that these two factors will have more influence on the timing of 450mm introduction than they will on the timing of EUVL introduction (Chapter 4), since 450mm is more purely a cost reduction technology and EUVL is both a performance improvement and cost reduction technology. Generally speaking, one would expect that if macroeconomic conditions are good, both the availability of R&D money and the demand for 450mm wafer technology will be high. Conversely, if macroeconomic conditions are poor, both of those factors will weaken. One could also expect that the future level of consolidation among chipmakers would influence the level of chipmaker 450mm R&D investments (with higher consolidation leading to higher chipmaker 450mm R&D financing). One might expect that macroeconomic uncertainty and level of industry consolidation would be correlated with each another (with higher consolidation more likely under poorer macroeconomic conditions). Because these factors counteract one another to some extent, they were not included in the 450mm model developed here. However, if justifiable estimates exist for both factors, they could be seamlessly incorporated into the model's payoff calculations.

More careful accounting of the "veto power" wielded by certain key equipment suppliers. As described in Section 5.3 above, the impact of suppliers' economic incentives regarding 450mm timing has been incorporated in the model in a generalized manner through the variable 450mm benefit timing dates described in Table 13. However, several individual equipment suppliers (notably ASML and Applied Materials) are important enough that perhaps their decisions need to be modeled with greater care, by adding them as separate strategic players (which would complicate the game theory model and equilibrium analysis significantly) or by making more detailed estimates of how their actions could slow down or speed up the overall 450mm development project. In particular, lithography suppliers (i.e., ASML and Nikon) have especially strong influence on wafer transition timing because their equipment tends to have the longest R&D lead time, and hence lithography has been the equipment bottleneck during previous wafer-size transitions (see Hutcheson 2006).

Possibility of significant early investment by chipmakers other than IST. As mentioned earlier, other chipmakers beyond IST may invest in 450mm technology in large enough magnitudes to impact the overall incentives of IST calculated in this model. For example, GlobalFoundries, the second largest semiconductor foundry behind TSMC, is one such potential player. Although an American company, one of the largest shareholders in GlobalFoundries is Advanced Technology Investment Company (ATIC) which is owned by the Mubadala Development Company (a sovereign wealth fund for Abu Dhabi) which may have the deep and patient pockets necessary to support the large investments required for significant 450mm development and implementation (Mishkin 4/11/13). Such a thrust by Global Foundries could have impacts on both the costs and benefits for IST calculated in this model.

Potential impact of geopolitical financial or regulatory changes. For example, there is currently a strong push by the U.S. government to revitalize manufacturing, especially of strategic high technology products. Any unanticipated U.S. government funding for semiconductor technology may impact the 450mm investment balance among industry firms.

Similar considerations would apply to any unanticipated moves made by the Korean, Taiwanese, or Japanese (still a powerhouse in the semiconductor equipment industry) governments. Finally, the European governments are in the midst of deciding their strategic approach to 450mm wafer technology (Mokhoff 2/27/12) given that their prominence among chip manufacturers has declined to the point that no major chipmakers with a home base in Europe are likely to substantially influence initial 450mm development. However, ASML, a semiconductor photolithography equipment supplier based in the Netherlands, will have a very large influence on the overall transition process.

5.6.3 Areas for Future Work Related to the 450mm Model

Engage industry experts in scrutinizing the 450mm model. Such experts can provide better input parameter estimates, point out any deficiencies in the model structure, and test it out for economic realism. Industry experts particularly familiar with the financial data from semiconductor manufacturing and demand forecasting will be most helpful. Ensuring that the model (currently a Microsoft Excel-based model) is well-documented and user-friendly will aid this effort.

Consider alternative game theory frameworks which more closely map the 450mm wafer transition incentives. We have applied a parsimonious, simultaneous, and finite-action game structure to understand the strategic interaction among the largest chipmakers regarding 450mm

wafer R&D expenditures. However, there are a number of alternative game theory frameworks which might turn out to more closely match the 450mm situation. Two promising ideas are "weakest link" games (e.g., Knez and Camerer 1994; Riedl et al. 2011) and cooperative game theory models (e.g., Peters 2008). The same basic approach taken here of iteratively triangulating all secondary data with industry experts (recall Figure 2) could be applied within the framework of one of these alternative game structures. It is also possible that a dynamic game could be formulated which more closely aligns to the 450mm situation. Confirming whether such an alternative model is an improvement over the model presented here would require further detailed parameter estimation and data collection (likely both in the form of secondary data sources and industry expert interviews).

Incorporate non-financial factors into the estimated payoffs of the players. Clearly other factors besides the simple E(NPV) payoffs used in this model are likely to be incorporated into the players' decision-making criteria. This could take the form of estimating risk-aversion of one or more players or of incorporating more sophisticated utility function modifications from behavioral or organizational economics. Clearly, one must be careful as one attempts such modifications to ensure that they represent improvements over the analysis presented here both because these modifications are difficult to pin down and because such modifications make the model more opaque to the relevant decision makers. One example of such a non-financial modification from the field of behavioral economics will be explored fully in Chapter 6 in the context of the 450mm investment game described in this chapter.

5.7 Discussion of Model Equilibria

By applying the iterative modeling approach described in Chapter 2 (and employed robustly in the EUVL context in Chapter 4), I have been able to derive a reasonably cohesive model which

engenders some face validity, but also which gives rise to some skepticism. The model sheds light on the action/reaction dynamics among Intel, Samsung, and TSMC regarding investment in 450mm technology using a relatively simple model framework (and hence, importantly, one which is transparent to the relevant decision makers). Within this strategic environment, the model provides insight into which assumptions and parameters are most crucial for chipmakers' involvement, highlighting when all three chipmakers are likely to invest versus when only one or two is likely to do so (recall that Figure 26 to Figure ***34*** and Table 15 to Table ***23*** summarize these results). The individual chipmaker R&D investment amount, the fraction of COGS savings from 450mm technology, the time lag for fast followers, the contestable semiconductor market share (due to 450mm), and the intra-IST market share competition among chipmakers all had quite strong effects on the Nash Equilibrium predictions from the 450mm model. In contrast, the ending date of the analysis (and thus *duration* of the 450mm cost savings benefits and market share impacts), the time lag to the start of benefits for early investors, the discount rate, and competition between IST and smaller chipmakers all had only mild to moderate impacts on the chipmaker investment predictions from the 450mm model.

However, despite these observations, the 450mm model must be judged as relatively inconclusive when it comes to making specific outcome predictions. Because of the numerous parameters with high uncertainty, many model scenarios were run. Expert judgment/opinion is required to decide which scenarios are expected to correspond most closely to the real-world outcome. In addition to the difficulty stemming from parameter uncertainty, a number of the scenarios yielded three PSNE, making the model's prediction in those scenarios inconclusive (although in the base case scenarios, the multiplicity of PSNE always corresponded to a single chipmaker investing – i.e., a "go it alone" outcome by one of IST).

Let us recapitulate again here briefly the biggest impediments to model prediction found during the 450mm modeling effort. The uncertain factors which seemed the most troubling were:

1. Market share implications of early investment in 450mm wafers
2. Uncertain capability of fast following by each of the IST firms
3. Heavy influence wielded by the largest equipment suppliers in the timing of 450mm development and the collective influence of the smaller suppliers and chipmakers (some of whom are ambivalent to or opposed to the 450mm wafer-size transition)
4. Influence of industry-wide consortia in directing activity related to the 450mm development program
5. Behavioral and organizational characteristics/tendencies specific to each firm which are not typically incorporated into standard E(NPV) financial analyses

The first two factors above were dealt with by considering a broad range of scenarios across these factors. The third and fourth factors were only dealt with in a partial manner through the chipmaker benefit timing assumptions embedded in the model. Finally, the fifth factor was not at all incorporated into the 450mm model, despite the fact that there is considerable evidence that these factors can influence strategic decisions heavily.

Because the fifth factor above has not been the focus of the 450mm analysis so far, I will provide a simple description of how such organizational tendencies could impact decision-making. Chapter 6 will explore a detailed example of how one might go about justifying and incorporating this fifth factor in the context of the 450mm technology model developed in this chapter.

According to this 450mm model analysis above, Intel has the most incentive to invest in 450mm, while TSMC has the least incentive. As explained earlier in Section 5.3, this is a consequence of the relative ordering of the COGS of the three chipmakers which directly impact the manufacturing cost saving portion of the benefits for each chipmaker. Thus, if one believes that manufacturing COGS among these three chipmakers might switch over time, then the ordering of incentives for investment in 450mm technology (Intel>Samsung>TSMC) could be re-ordered. For example, if the manufacturing costs (as measured by COGS) equilibrate for these three companies, as some industry watchers think is possible given current growth rates of foundry semiconductor revenues, then the asymmetric investment incentives (and NE in many of the sensitivity analyses) seen in this chapter's analysis would also disappear. However, clearly other factors besides simply financial E(NPV) calculations also play into firms' strategic decisions. In particular, it is interesting to speculate regarding when and how the Asian companies (i.e., Samsung and TSMC) will shift *psychologically and organizationally* to a point where they are early adopting leaders (a mantle which Intel, and previously IBM, have assumed in the past) for such industry-wide "communal" R&D efforts such as 450mm wafer technology. As mentioned earlier, a detailed (qualitative and quantitative) discussion of how these organizational tendencies might be addressed will be fleshed out more fully in Chapter 6.

As of the writing of this dissertation (in early 2013), although it is clear that Intel, Samsung, and TSMC are involved via consortia in 450mm development (including in some financing actions), it is also widely acknowledged that most of the 450mm R&D expenditure which must occur still resides in the future; one analyst claimed that out of $17B of cumulative R&D expected to be spent on 450mm wafer technology development, only $2B is planned to be spent in 2012 (see McGrath 7/11/12). Thus, at a high level, no dramatic subsequent confirmatory evidence (as was

seen for the EUVL technology in the second half of 2012) has yet occurred for 450mm wafer technology. However, a few relevant 450mm financing events have already occurred. Specifically, a $700M USD portion of Intel's July 2012 investment in ASML was earmarked for 450mm lithography technology at ASML (ASML 7/9/12), presumably in large part to aid ASML's development of 193i optical lithography on 450mm wafers (e.g., see Mack 7/25/12). This single data point lends some marginal credence to the "Intel-only invests" Nash Equilibrium (i.e., ('Invest', 'Don't Invest', 'Don't Invest')) found under some scenarios and some reasonable parameter values (since this is, by far, the largest chipmaker investment to date in a single equipment supplier for 450mm technology).

In addition, a new, large consortium, G450C, has been created (announced in September 2011, see McGrath 9/27/11) to help promote 450mm wafer development technology. The $4.4B announced for its development is spread over six organizations (Intel, Samsung, TSMC, GlobalFoundries, IBM, and the State of New York) and over many years. Hence, although the total amount of money committed is relatively large, it is spread over a long period of time and is not as dramatic or clear an event as portions of the three IST investments in ASML's co-investment program which were focused on the acceleration of EUVL technology (Section 4.8.1). Thus, it currently seems likely that 450mm technology will be pushed along by smaller amounts of R&D funding distributed across a long period of time and to involve, at least to some degree, chipmakers other than Intel, Samsung, and TSMC (although IST will retain an undeniably strong influence on the nature and pace of the 450mm transition).

Historically, for the last several wafer-size transitions (i.e., from 100mm to 150mm, 150mm to 200mm, and 200mm to 300mm) it is widely believed that the firm(s) that have moved first have actually been *disadvantaged* by their early involvement (see Dan Hutcheson's comments in

Krzanich 2011). If one believes that will also be the case for the 300mm to 450mm wafer-size transition, that leads one to believe that the "no market share impact" scenarios (i.e., Scenario #5.1, or even #5.0) may be closer to the truth than are the scenarios involving a "moderate" level of contestable market share (i.e., Scenarios #5.2 through #5.4). In Scenarios #5.1 and #5.0, the strategic situation is that the largest chipmakers each want 450mm to be available soon but that each has a heavy incentive to free-ride on the early investment effort of others. This free-riding dynamic (as well as potential resistance from some equipment suppliers) seem like a reasonable explanations why chipmakers and equipment suppliers appear to be working together in a consortial fashion, perhaps at a slow pace and apparently with less wasted R&D spending (see Krzanich 2011).

Thus, considering the heavily consortial and relatively slow approach which the industry seems to be following, as well as the uncertainty regarding costs and benefits of leading vs. fast following during wafer-size transitions, the 450mm wafer model presented in this chapter should be viewed as more of an efficient guide for intuition building and learning (i.e., a "directionally correct" management flight simulator, if you will) and less a generator of highly specific outcome predictions. Clearly, considerable sensitivity analysis and deep thinking regarding the possible confounding factors considered above is crucial when interpreting and attempting to glean strategic insights from the 450mm model outcomes.

Perhaps having industry content experts and decision makers deeply engage with the model may help further refine it and engender it with more precision and fidelity. Alternatively, some structural changes may be needed, redirecting efforts toward other types of game theoretic models including the "weakest link" or cooperative game theory models (see Section 5.6.3 above).

At a minimum, I believe the 450mm model presented here (especially in concert with the more robust results and confirmatory evidence from the EUVL model) illustrates to decision makers in firms and consortia the power of game theory as an *additional* tool to provide insight and aid strategic decision-making in an important subset of highly impactful, complex strategic situations. The next two sections will explore the notion of linking the 450mm and EUVL models (Section 5.8) and will compare and contrast the two models (Section 5.9).

5.8 Possible Linkage between 450mm Model and EUVL Model

One interesting point to consider is that lithography equipment suppliers (i.e., ASML and Nikon for the most part) and large chipmakers are experiencing the 450mm transition and the EUVL transition at approximately the same time. Thus, although the two transitions have been modeled separately in this thesis, one may be tempted to think that one should create one overarching model which combines both transitions. However, part of the thrust of this dissertation has been on the development of models which can achieve high-level managerial buy-in and actually be used for strategy development. To this end, a model's transparency and traceability (and hence a reasonably parsimonious framework/approach) are needed to produce practical models (e.g., Little 2004). Said more directly, the managers who will make the $1B+ valued decisions and/or recommendations to the CEOs of large firms need to have a reasonable amount of visibility "inside the black box" of the models they use to make and to justify their decisions. This is a large part of the reason the models for EUVL and 450mm wafers were developed and presented separately despite the fact that there is quite significant overlap in the firms involved, and hence managerial viewpoints regarding both transitions.

It is certainly theoretically possible to link the two models (which would entail more complex investment decisions and compound payoff functions incorporating both 450mm and EUVL effects). However, this must be done with great care as it dramatically reduces managerial visibility and traceability of the effects of model parameters on the incentives of the various players. The philosophical approach taken in this dissertation is that each investment model must provide significant cognitive economy to the decision makers, but that there is still a central role for "managerial art" to stitch together quantitative model results to each other and to relevant qualitative factors in the decision making process.

One interesting note is that some of the investment amounts in the ASML co-investment program by the chipmakers were "earmarked" for either EUVL R&D or 450mm R&D at ASML, the largest semiconductor equipment supplier (see ASML 7/9/12; Mack 7/25/12). There is an open question about enforceability of these earmarks (i.e., around the fungibility of these chipmaker R&D financing contributions to ASML), but the earmarking reflects the fact that the EUVL and 450mm investments (and perhaps the behind-the-scenes negotiations) are viewed separately, at least to some extent, by the chipmaker participants.

5.9 Similarities and Differences between 450mm Model and EUVL Model

The 450mm wafer size and EUVL models developed in Chapters 4 and 5 are similar in some ways and different in others. As discussed above, while the 450mm model sheds light on the strategic factors influencing semiconductor R&D investments, it generated less specific predictions than were derived from the EUVL model analysis. Two big reasons for this are: 1) The 450mm wafer-size transition is more "communal" – that is, it *requires* a larger number of distinct players to be involved, and 2) Much of the 450mm technology development effort is

considerably less "appropriable" than is the case for EUVL technology (recall our discussion of these points in Section 5.3.1). Expanding on the first reason stated above, it is clear that the 450mm transition requires greater organizational complexity (but lesser technological complexity) than the EUVL transition. Even if only four key equipment suppliers were required to galvanize the semiconductor supply chain for 450mm technology development, the number of inter-firm relationships is large and the inter-organizational complexity is quite high. (See Figure 35 for a schematic view of this difference.)

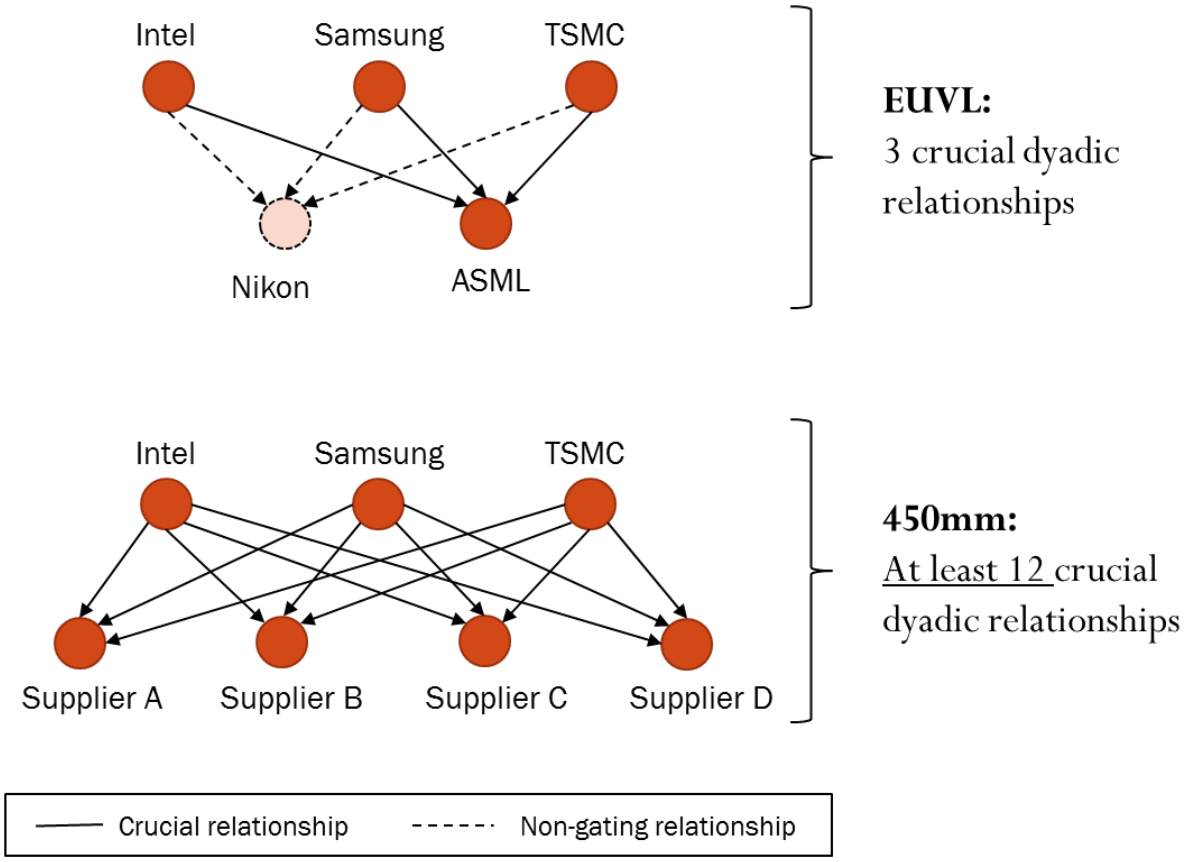


Figure 35: Schematic View of Crucial Dyadic Relationships During EUVL and 450mm Wafer-Size Transitions

As a consequence of the very high inter-organizational complexity, it was necessary to abstract away from the multiple equipment suppliers required for 450mm development, and hence the nature of the use of the 450mm model is more for learning/intuition building and less well-suited for highly specific investment prediction. Table 24 below recapitulates some of the more specific similarities and differences seen in the two models.

Table 24: Similarities and Differences Between EUVL and 450mm Models

Aspect of study	EUVL Model	450mm Model
Goal/usage of model	Focused on outcome prediction as well as learning.	Focused largely on intuition building (although could be developed in more comprehensive ways to include more specific prediction)
Core difficulties explicitly modeled	Technological difficulty of making EUVL practically useful. Difficulty of coordinating industry effort behind one or two suppliers.	Difficulty of coordinating chipmaker funding to promote 450mm wafer technology in a timely manner. Understanding how quickly fast-following chipmakers can catch up on 450mm technology.
"Critical Few" components of firm payoffs explicitly modeled	- Chipmakers' (aggregate) EUVL R&D investment expense - Manufacturing cost savings from EUVL - Lithography equipment pricing difference (1 supplier vs. 2 suppliers)	- Chipmakers' (individual) 450mm R&D investment expense. - Manufacturing cost savings from 450mm - Market share gains/losses due to 450mm
Big uncertainties evaluated (in model scenarios and/or robustness checks/ sensitivity analyses)	- Magnitude of Chipmaker financing help - Technological difficulty of EUVL - Simultaneity of chipmaker and equipment supplier investments - Market share competition among the equipment suppliers	- Magnitude of Chipmaker financing help - Time lags for early investors vs, fast followers - Amount of market share which is contestable (via 450mm wafers) and type of competition which governs this - Amount of COGS savings for chipmakers
Dynamic games considered?	Yes (2-stage)	No
3 player games considered	Yes	Yes
Number of tiers of supply chain explicitly modeled	2	1
Symmetry of players	Heavily asymmetric players	Asymmetric players

Aspect of study	EUVL Model	450mm Model
Discrete vs. Continuous action choice sets	(discrete, 2-4 actions/player)	(discrete, 2 actions per player)
Stochastic parameter inputs	No	No
Sensitivity analysis performed	Yes	Yes
Forcing functions for technological change	Competition; ITRS roadmap "requirements"	Competition; ITRS roadmap "requirements"
Risk-neutrality assumed	Yes	Yes
Exponential discounting of expected profitability	Yes	Yes
Expected Cash Flow Horizon	10 years	20 years
Primary modeling orientation	Firm strategy maker	Firm strategy maker
Explicit modeling of governmental action	No	No
Sensitivity analysis performed for key model parameters	Yes	Yes
Direct modeling of sales price of individual manufactured goods/equipment	No	No

Now that we have examined the similarities and differences between the two main case studies and modeling efforts in the dissertation, Chapter 6 will next explore how one could incorporate firm behavioral patterns to add color to and ultimately to modify the "purely economic" E(NPV) payoff estimates I have been utilizing thus far. Subsequently, Chapter 7 will conclude this dissertation with overall take-away lessons including a detailed proposal of the industry and technology characteristics which make a situation fertile (or not fertile) for the type of applied game theoretic modeling developed here.

Chapter 6: Qualitative Analysis of Samsung's Behavior and Refinements to 450mm Model Payoffs

"Samsung Electronics reminds me of a military organization. It has a clear hierarchy with orders and obedience, and there is a tension felt in the overall organization. It is an organization full of people who are ready to rush towards the frontline and sacrifice themselves with an order of a commanding officer. Chairman Kun-hee Lee is the commander in chief of this military organization."

– A high-ranking executive at Sony
(from Chang 2008, location 1656/3514)

"Samsung used to have advanced companies that served as lighthouses, but now it must venture into the open seas on its own."

– Kun-hee Lee
Chairman, Samsung Group, 2007
(from Mitchell 2010, location 4840/5615)

As discussed in Chapter 5, several potentially important factors may be lacking in the 450mm model casting some doubt on specific model predictions. Among these are:

- Does the model accurately characterize the impact of equipment suppliers' power to determine 450mm development via investment/timing assumptions?
- Does the model appropriately incorporate the non-pecuniary psychological/organizational aspects of Intel's, Samsung's, and TSMC's strategic decision-making processes?

It is this second question which will be explored in this chapter.

6.1 Behavioral Refinements to Payoff Estimates in 450mm Model

Although the modeling frameworks of Chapters 4 and 5 have been predominantly game theoretic, Faulkner and de Rond (2000) argue that more than ten different economic and non-economic lenses can be used to analyze cooperative alliances (summarized in Table 25 below),

many of which could also be used to study the coopetition among IST on early 450mm investment.

Table 25: List of Possible Lenses through which to Analyze Coopetitive Interactions (from Faulkner and de Rond, 2000)

The Economic Viewpoint	The Organization Theory Viewpoint
• Market Power Theory • Transaction Cost Theory • The Resource-based View • Agency Theory • Game Theory • Real Options Theory	• Resource Dependency Theory • Organizational Learning • Social Network Theory • The Ecosystems View • The Structurationist Perspective

The structure of the remainder of this chapter will be as follows. First, I will present a motivational divergence between one of the strategic trends predicted by the 450mm model in Chapter 5 and the apparent behavioral pattern to-date of Samsung, one of the three strategic players. Specifically, although the 450mm model indicates that Samsung has a robust incentive to invest early in 450mm technology under many conditions, Samsung's actual behavior seems to reflect a relatively apathetic approach toward doing so. Second, I will propose five plausible explanations which could help resolve this divergence. Third, I will summarize a rigorous analysis of Samsung investment decision behavioral traits, with a keener focus on those traits which have most bearing on its decision regarding early investment in 450mm technology. Finally, I will provide a detailed example of how insights from this qualitative behavioral analysis could be used to make refinements to Samsung's payoff estimates in the 450mm investment game, influencing their incentives to invest (and in a number of cases actually toggling their optimal decision). Figure 36 below presents once again the game tree from Scenario #5.3 (originally given in Figure 29 from Chapter 5), with light and dark colored stars

designating the two outcomes in which Samsung payoff estimates will be scrutinized throughout this chapter.

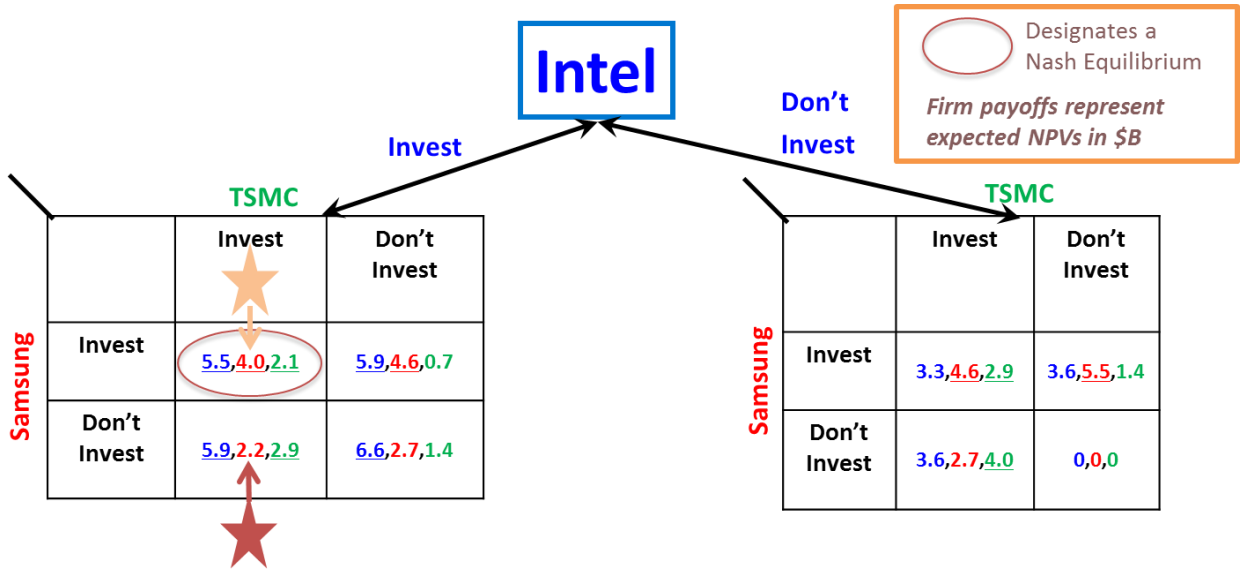


Figure 36: Scenario #5.3 Game Tree Indicating Samsung Payoffs being Studied and Refined

6.2 Five Possible Explanations of Samsung's 450mm Investment Decision Divergence

Some industry managers and analysts may experience cognitive dissonance between the general trend observed in the Chapter 5 450mm model results (i.e., Intel's incentive to invest > Samsung's incentive to invest > TSMC's incentive to invest) and their own intuition. Specifically, their opinions, also echoed by some opinions stated in the industry trade press, may be that the order of urgency for 450mm technology seems more like: Intel ≈ TSMC > Samsung (e.g., Lapedus 4/6/11; Shilov 12/10/12; Solid State Technology 3/1/11; Solid State Technology 9/27/11). Recall that Table 15 through Table ***22*** reveal Samsung's robust incentive to invest in the 450mm model. Below are five possible explanations one might consider to resolve this cognitive dissonance in industry participants' minds.

Explanation #1: Samsung could grow more slowly than Intel and TSMC in the future. TSMC may eventually grow to obtain more market share than Samsung in the future. The justification for this assumption seems tenuous because Samsung is dramatically expanding their presence in the logic/foundry semiconductor segments and because they seem unflinching in their desire to expand their semiconductor business overall.

Explanation #2: Delays to 450mm will hurt Samsung less than Intel and TSMC. Even assuming Samsung grows healthily and remains significantly larger than TSMC in value of semiconductor production (and hence in COGS which is reduced via 450mm technology), perhaps IST players believe that delays to 450mm will hurt Samsung less than they will hurt Intel and TSMC. This could be due to differing market dynamics assumed in the memory chip market, Samsung's currently largest semiconductor market segment.

Explanation #3: There are minimal market share implications for 450mm and Samsung is betting that Intel and/or TSMC will invest first. The universal industry view may be that Scenario #5.0 or #5.1 approximates reality and thus Samsung is relying on confidence in their ability to quickly fast follow on 450mm and on Intel's and/or TSMC's self-interest in investing early in 450mm technology. If true, this becomes a coordination game akin to the game of chicken (e.g., Dixit et al. 2009) in which Samsung is betting that Intel and/or TSMC will move first to invest early in 450mm technology.

Explanation #4: Samsung can fast-follow more quickly than Intel and/or TSMC. In this explanation, the overall industry view (either universally or among all except Samsung) is that reality is somewhat like Scenarios #5.2 through #5.4 or #5.6 through #5.8, with the exception that Samsung has the ability to more quickly fast-follow on 450mm fabrication than Intel or

TSMC. This might imply that Samsung has an incentive to drag its feet on its own contributions to 450mm development.

Explanation #5: Samsung may simply have a higher level of financial impatience and/or impulsiveness than Intel and TSMC for its 450mm investment. Samsung may deem early investment 450mm (perhaps for some of the reasons above) as nonessential to their corporate strategic plans. Perhaps EUVL technology is seen by Samsung Electronics as a strategically crucial technology, while 450mm is seen as significantly less so. Such a view might be supported by two relevant facts: 1) Samsung Electronics has quite large and growing product groups apart from semiconductors (while Intel and TSMC do not) and 2) Samsung has a long and successful history of ramping factories swiftly and effectively (e.g., Chang 2008; Kim 1997). The first fact implies that Samsung does not have all of its eggs "in the semiconductor basket", and that it might be willing to roll the dice by not investing in 450mm early, since early leadership in 450mm is less crucial than early leadership in EUVL for maintaining its formidable and growing position in the broader electronics industry. The second fact implies that even if 450mm (and the cost benefits associated with it) were to somehow become more strategically important, it has the relatively certain back-up option of rapidly accelerating its 450mm ramp efforts at a later date.

If Samsung holds such a strategic view of 450mm technology, this may lead them to require a higher expected return (i.e., to discount the future benefits more heavily) than Intel or TSMC do for any early investment in 450mm technology. Two flavors of such heavier financial discounting – impatience and impulsiveness – will be defined and explored further in the following sections of this chapter.

Although Explanation #1 seems relatively unlikely, the other four explanations all have the ring of some plausibility and could be impactful to Samsung's decision. The purpose of the analysis in the remainder of this chapter is not to definitively disambiguate among the four remaining explanations; it is to show in some level of detail (extending the 450mm case study and model in Chapter 5) how one can use detailed rigorous qualitative analysis of the a firm's behavior to make educated guesses about model refinements that might be appropriate to Samsung's payoff estimates for early 450mm investment and how to implement and interpret such refinements.

Let us now proceed with a brief examination of the modeling implications of each plausible explanation.

6.3 Modeling Implications of Samsung's 450mm Investment Decision Divergence

The actual reason for the partial divergence between the analysis in Chapter 5 and Samsung's 450mm behavioral indications to-date could be some combination of Explanations #2 through #5. I will briefly explore below the modeling implications for each of these explanations; the implications run the gamut from straightforward modifications of existing payoff estimates within the framework of the complete information games presented in Chapter 5 to more complex implications which move us into the realm of games of incomplete information. Later in the chapter, I will expand in considerable detail on the modeling implications of Explanation #5.

If Explanation #2 (*i.e., Samsung is hurt less from 450mm delay*) is correct, then the modeling implications are relatively clear: the impacts of asymmetric 450mm cost reductions can be calculated for (and by) each of the three players and incorporated into the commonly-known payoff estimates for each player. Given the level of rough agreement among demand forecasters

in the semiconductor industry it seems likely that there is a reasonable level of common knowledge (in the game theoretic sense of the term) among IST regarding future market demand and manufacturing costs for the large semiconductor segments. This type of 450mm-impact asymmetry will not be modeled explicitly in this dissertation.

If Explanation #3 (*i.e.*, *Samsung betting Intel or TSMC will move first*) is correct then the game theory modeling implications are relatively clear; they indicate that the prediction from the game is ambiguous due to the existence of multiple equilibria. In each of Scenarios #5.0 and #5.1 there are three PSNEs, each corresponding to the "go it alone" investment outcome where only one chipmaker (among IST) invests early on 450mm. To disambiguate among the multiple equilibria, economics has two nascent approaches which could be relevant (evolutionary game theory and experimental economics), however these approaches are beyond the scope of this dissertation.

If Explanation #4 (*i.e.*, *Samsung can fast-follow more quickly than others*) is correct, then the modeling implications can remain quite simple or become considerably more complex depending on the assumption of the three players beliefs regarding how quickly Samsung can fast-follow on 450mm technology. If it is common knowledge (among IST) that Samsung can fast follow more quickly than the others, the model analysis remains a game of complete information, and thus relatively simple to analyze. For instance, one could assume a one-year time lag for Samsung vs. a two-year time lag for Intel and TSMC and recalculate the payoffs accordingly. (This is the most natural assumption in the context of the 450mm model in Chapter 5 given the yearly cash flow buckets used.) If, however, Samsung alone believes it can fast-follow more quickly than Intel and TSMC, this corresponds to a game of imperfect/incomplete information where beliefs about the payoffs of the various players differ among the three players. In these situations the

appropriate equilibrium concept in this context becomes the Bayesian Nash Equilibrium (see Gibbons 1992). Given one believes and has rigorously validated the 450mm model framework as derived in Chapter 5, one could extend this model to such a game of incomplete information. However, this possibility will not be explored in this dissertation.

If Explanation #5 (*i.e.*, *Higher Samsung financial impatience/impulsiveness*) is correct, then depending on the state of the players' beliefs, the modeling implications could again be relatively simple or quite complex. Specifically, if we maintain the assumption of full common knowledge of the discounting behavior of all players (including knowledge of one's own discounting behavior), then the equilibrium analysis remains quite simple as this implies that each player can calculate with certainty all of the players' ultimate payoffs (including its own) in each of the possible outcomes of the game. If one deviates from this assumption, then one (once again) enters the realm of incomplete information game analysis.

In the absence of knowing which explanation or which combination of these four remaining explanations is correct, it is difficult to pin down deviations from the simpler complete information model covered in Chapter 5. However, it is possible to push the analysis forward and show what the payoff implications of these explanations would be, were strong evidence found to support them.

As an illustration of how such model payoff refinements can be incorporated into the simpler game frameworks, the remainder of this chapter will quantitatively analyze Samsung's behavioral patterns regarding strategic decision making and subsequently incorporate distillations of those patterns into Samsung's payoff estimates. Specifically, I will focus on incorporation of Explanation #5 (impatience/impulsiveness) into Samsung's payoff estimates.

Further, I will limit the analysis here to games of complete information. If more complex assumptions were justified by additional data collection within this industry context, one could incorporate refinements corresponding to those assumptions using the full set of tools available in modern game theory.

6.4 Detailed Qualitative Behavioral Analysis of Samsung

Given the motivation described earlier for studying Samsung's investment behavior in depth, the process used in this study was to examine a broad swath of secondary data sources on Samsung's behavioral patterns (see comments in Yin 2009 on triangulation among various data sources in a case study). The secondary data sources studied included relevant academic papers, books examining the history and strategy of Samsung Electronics, and germane trade press articles.

Additionally, Samsung's behavioral traits were analyzed at the following levels of analysis: Korea (national), Samsung Group (*chaebol*, a Korean business conglomerate largely directed by one person, the chairman), Samsung Electronics (corporate entity), and Samsung Semiconductor (division), with a particular focus on the last three levels of analysis.

A high-level distillation of the findings about Samsung's behavior can be found in Table 26 below.

Table 26: Summary of Samsung's Behavioral and Strategic Traits

Dimension of Strategy/Behavior	Samsung Group & Samsung Electronics	Samsung Semiconductor Division
Fast following vs. leading	***Past :*** Fast follower ***Present :*** Transitioning toward more leadership (for both products and processes)	***Past :*** Consummate fast follower (copy product/process and ramp chip factories quickly) ***Present:*** Hybrid Leader/fast follower in memory chip space (process and product). Still fast-following in foundry space although catching up quickly (i.e., using IBM and Common Platform Alliance as partners)
Short-term vs. long-term investment horizon	Both viewpoints co-exist. (Short-term competition among business groups + longer-term viewpoint imparted from "top-down")	Short-term projects driven by financial results orientation. Long-term demonstrated by pattern of aggressive investment in semiconductor fabrication capacity.
Vertical integration vs. outsourced capabilities	Generally believe that vertical integration and economies of scope are good (for both Group and Electronics)	Committed to semis to support Electronics and future target markets. See participation in both memory and logic as synergistic. Desire to have Korean (or internal?) equipment suppliers.
Competing on cost vs. technology	Strong capability to compete on both	Compete on both (aggressive at price reduction now to gain market share, but also aggressive invest in strategic R&D)
Horizontal inter-firm R&D competition vs. cooperation	Willingness to choose competition or cooperation strategically (depending on the situation)	Common Platform Alliance is a prominent example of cooperation
Modular vs. integral supplier relationships	Primarily modular relationships with their suppliers	Primarily modular relationships with their suppliers. Recent investment in ASML (August 2012) signals potential change (perhaps reluctant) toward more integral relationships
Human resources: Organizational learning vs. specific skill acquisition	***Past:*** HR focused on (intelligent) fast following ***Present:*** Aware of their "creativity gap". Aggressively working to address it.	***Past:*** HR focused on (intelligent) fast following ***Present:*** Aware of "creativity gap". Strong engagement with IBM/Common Platform. Aggressive semiconductor division expansion/hiring overseas (e.g., U.S. and China)

6.5 Analysis of Samsung Behavioral Strategic Traits Most Relevant to 450mm Decision

Once a distillation of the general behavioral patterns across these categories was completed for the Samsung Group and Samsung Electronics (middle column of Table 26) and Samsung Semiconductor (right column of Table 26), I narrowed my focus to those categories of behavior which seemed most relevant to Samsung's strategic behavior regarding 450mm investment. The three categories deemed most important to Samsung's 450mm decision were: fast following vs. leading, short-term vs. long-term investment outlook, and horizontal R&D competition vs. cooperation. I will expand on the secondary data found for those three traits and behaviors in greater detail below.

6.5.1 Samsung's Fast-following vs. Leading Behavior

Linsu Kim's well-researched *Imitation to Innovation: The Dynamics of Korea's Technological Learning* (Kim 1997) recounts (with Samsung Group prominently discussed) Korean *chaebols'* pre-mid-1990s strategy of technological fast-following, which led to dramatic success in the electronics, semiconductor, and automobile industries. Kim recounts multiple examples of a deeply focused approach to technology acquisition and incorporation in which the cream of the crop of Korean engineers partnered directly with western companies (where allowed) and then brought this technology back to Korea in a more active manner than many Asian countries trying to catch up to the West. Although heavily reliant on western technology in the first one or two product versions, Korea focused on the development of deep technological human capital development within the *chaebol*. Building on this active approach to gaining technological know-how, the *chaebol* were quickly able to transition over to incremental innovation within

Korea. This put a number of the *chaebol* onto the path to economic success which they have enjoyed to the present.

Mitchell's and Chang's more recent works (Mitchell 2010; Chang 2008) clearly indicate that in portions of Samsung's business the skillful application of fast-following strategy is still alive and well (and perhaps still dominant), but that Samsung senior leadership is now deeply aware of the need to augment its strategy to include greater creativity and innovation. As early as 1993, current Samsung Group chairman Kun-hee Lee famously exhorted his senior executives to "change everything except your wife and kids" (Mitchell 2010, location 1375/5615) indicating that disruptive change in Samsung's products and strategies would be the norm and not the exception. It also exemplifies the "management by crisis" philosophy which is infused from the top-down at Samsung. This managerial philosophy is based on the notion that complete devotion to task and forceful execution are engendered by crises – even to the point that if a crisis does not exist, one should be created to help achieve the desired aims.

Clearly, if an organization is able to continually motive one's employees via crises, it is likely to be able to ramp new manufacturing technologies more quickly than those who cannot do so. "Management by crisis" seems to be an important enabler of Samsung's ongoing use of fast-following as a strategic weapon. Samsung Electronics seems to epitomize the oft-used Korean phrase "*pali*, *pali*" which means "faster, faster" (see Rim 2007), exhibiting extremely fast approaches to manufacturing and product development in DRAM/Flash memory chips (Kim 1997; Dongyoup 2006, page 89; Chang 2008, location 596/3514), mobile phones (Chang 2008, location 914/3514), and LCD TVs (Chang 2008, location 906/3514). An executive of Samsung Electronics has coined the phrase "Digital Sashimi Theory", saying "Speed is the key to all perishable commodities from sashimi to mobile phones. Even expensive fish becomes cheap in

a day or two. For both the sashimi shop and the digital industry, inventory is detrimental and speed is everything." (Chang 2008, location 729/3514). An example of how extreme devotion to company goals can form the basis of faster technology implementation can be found in the following anecdote from Chang:

> "Samsung Electronics not only put a great deal of effort into learning how to produce DRAM but also completed its first production facility in six months, rather than the industry norm of two to three years. Samsung managers managed the plan, design, and construction of the facility -- all at the same time. Samsung's managers and engineers stayed in barracks during the construction period, returning to their homes only once a week to change their clothes. When it began its initiative in DRAM technology, Samsung Electronics was about five years behind its Japanese competitors; the early completion of its first facility narrowed the gap by two years." (Chang 2008, location 898/3514).

Chang goes on to relay that Samsung has taken the same high speed approach to wafer-size transitions in the past:

> "After it began making DRAM, Samsung Electronics then caught up with its competitors by aggressively expanding its production lines. It constructed a second line that produced 6-inch diameter wafers, a size that even technologically advanced competitors such as Intel and NEC deployed only for pilot lines. Samsung's engineers worked around the clock to improve efficiency in this new plant. Samsung Electronics repeated the same formulae with 8-inch wafers in the early 1990s, and 12-inch wafers in the late 1990s." (Chang 2008, location 898/3514).

The above has been just a brief summary of the volumes of secondary data available concerning Samsung's fast following behavior, but from it the pattern emerges is that *at least historically* Samsung is a consummate fast follower -- with added emphasis on the word fast. It is also the case that Samsung Electronics is actively trying, and largely succeeding, to emerge as a leader in end-consumer-focused products (e.g., mobile phones, TVs, etc.), and they strongly believe that it is necessary for them to remain at least competitive (if not lead) in component production (e.g., semiconductors). Samsung continues to believe that such vertical integration across the supply chain is important for its overall success in consumer electronics (Tomkins 1/15/12).

Although Samsung has a strong history of investment in its own semiconductor capacity, it is unclear how much capital they are willing to invest in communal R&D efforts such as 450mm wafer development, given Samsung's demonstrated capabilities in semiconductor fast following and its ambitious aims to expand into five new capital-intensive categories in green energy and healthcare by 2020 (the Economist 10/1/11(b)). Perhaps the fact that it only took a 3% stake in ASML and their R&D contribution was earmarked for "next generation lithography", often code for technologies beyond optical lithography such as EUVL (ASML 8/27/13; McGrath 8/27/13), is a partial indication that Samsung is maintaining a fast-following strategy vis-à-vis early investment in 450mm equipment R&D. However, they are unlikely to want to fall far behind on 450mm, having benefited tremendously in the past from their relatively early adoption of new wafer sizes which gave them a competitive advantage over Japanese memory chip makers (see Chang 2008, location 898/3514; Solid State Technology 3/1/11). Regardless of their level of investment in early 450mm equipment R&D, I believe it is safe bet that once 450mm equipment reaches a certain level of maturity, Samsung will plan to invest in their own 450mm production capacity full bore and with high velocity.

6.5.2 Samsung's Short-term vs. Long-term Investment Time Horizon Behavior

Now that we have demonstrated Samsung's perhaps tempered, yet ongoing, allegiance to fast following in manufacturing, let's take a closer look at evidence regarding its managerial time horizons for investment analysis. Its time horizon for investment analysis is closely related to its approach to fast following, yet is also a distinct characteristic. Samsung seems to display evidence of both long-term and short-term financial perspectives. I will explore the evidence pertaining to both perspectives in turn and then address how to resolve the tension created by their co-existence.

6.5.2a Evidence for Long-term Financial Outlook at Samsung

Samsung clearly has some elements of long-term thinking in their approach. One big difference between Samsung and many other prominent electronics/semiconductor companies is its corporate structure and governance. Korean law and public policy have created a byzantine set of rules which govern stock ownership in that country (see Chang 2008, chapter 7). This has led to a complex and bizarre set of cross-ownership agreements that allow Samsung Group, which as of 2007 represented almost 20% of Korea's GDP (see Mitchell 2010, location 1619/5615), to be run in some ways like a family-owned business, because to a large degree it still is. (It is interesting to note here that the byzantine rules are driven largely by the fact that Samsung Group and other *chaebol* are not legal entities.) The current chairman, Kun-hee Lee, who is 71 years old and the son of founding chairman Byung-chul Lee, is grooming his son, Jae-Yong Lee, to replace him. Despite the governance weaknesses associated with a family-run business, two strengths of this arrangement are:

1) Ability for fast, military-style execution (see quote at beginning of this chapter)

2) Ability to focus on long-term investment horizons (in a manner similar to privately owned businesses in many of the world's economies)

Highlighting this second strength is a quote by Samsung Group's founder Byung-chul Lee from 1976: "The life of a man is short, but that of a corporation must never be." (Mitchell 2010, location 555/5615). This attitude also certainly applies in full force to Samsung's attitudes about the long-term strategic importance of its semiconductor division. Samsung has a history of investing in semiconductor capacity even when the semiconductor segments they compete in are not profitable. Chang (2008) provides a vivid example of this strategic viewpoint within Samsung Electronics:

> 'President Yoon-woo Lee of Samsung Electronics' Semiconductor Division described the factors that led to his division's success in the memory semiconductor business: "I think the corporate governance system in Korea was in our favor, too. For this high-risk, and high-return industry, the *chaebol* system worked well for us. Since Samsung was controlled by a charismatic leader, Chairman Lee, we could make this series of bold decisions. I think such bold decisions would not have been possible in other countries, where companies are controlled by professional managers. Memory is a business in which you cannot make a profit in the next upturn if you did not make a proper investment in the past. You need to make profits in the upturns to invest them for the next upturns. Thus, if you cannot invest properly according to a business cycle, you are not well prepared for the next one. If you miss this timing several times, then you quickly go out of business. Samsung could invest even in downturns since Samsung was a *chaebol* company." ' (Chang 2008, location 2376/3514).

Additionally, it is clear that Samsung actually follows the investment philosophy described above. Samsung invested successfully in memory chip manufacturing capacity during the midst of recession in the mid-1980s (Chang 2008, location 580/3514). It has also invested this way in several more recent instances as well. (See Handy [2012] for a general discussion of the dramatic cyclicality of manufacturing capacity investment in the memory chip market.)

Despite the longer-term outlook afforded to managers of Korean *chaebols* (including Samsung), some western observers have been quick to highlight the downsides of weak external oversight of managerial decisions within Samsung. This weak governance structure has enabled Samsung management's legal abuses of power and its ill-fated and expensive foray into the automobile industry (The Economist 2/11/12).

6.5.2b Evidence for Short-term Financial Outlook at Samsung

Several quotes from Chang (2008) and Mitchell (2010) call out the short-term financial outlook often present within Samsung. Regarding incentives to employees and business divisions Chang states:

> "At Samsung Electronics however, the variable portion of employees' annual compensation has sometimes been higher than the fixed portion is. In this respect, Samsung Electronics is managed more like U.S. firms, which often pay large financial incentives to their employees. Samsung Electronics is unusual in Korea where most firms emphasize equity over performance. It is not clear whether Samsung Electronics can avoid keeping its business divisions from being silos so long as it provides strong financial incentives based on short-term performance. In this way, Samsung Electronics

> may discourage long-term investment and interdivisional cooperation." (Chang, 2008, location 2068/3514).

In Jong-yong Yun, the former CEO of Samsung Electronics, Samsung had an advocate of western management philosophies (especially those of Jack Welch). Mitchell states that "Yun introduced cash-flow principles to Samsung Electronics and emphasized profits over market share." (Mitchell 2010, location 916/5615). Later, Mitchell goes on to convey that Yun also subscribed to management by crisis:

> 'Yun, who repeatedly described himself as "the chaos maker," said he "tried to encourage a sense of crisis to drive change. We instilled in management a sense that we could go bankrupt any day." ' (Mitchell 2010, location 916/5615).

6.5.2c Synthesis/Resolution of Long-term vs. Short-term "Paradox"

Clearly, evidence of both long-term and short-term investment horizons can be seen in Samsung's past behavior, and Samsung's decision-making process involves additional factors besides maximizing E(NPV) (e.g., Korean national pride, proclivities of its chairman, etc.).

The resolution of the long-term vs. short-term "paradox" seems to lie in the simultaneous top-down, long-term strategic vision driven largely from the chairman married with short-term, cost-focused financial controls exerted by middle managers on lower levels of the company. I believe that Samsung's goal has been not only to grow (by expanding their existing businesses and by entering new businesses), but also to become a world leader in a more psychological sense (echoes of this theme can be found throughout Mitchell 2010). For Samsung, the path to growth and to becoming a world leader has largely been to enter new customer-facing markets and to expand its global brand (see Mitchell, 2010, chapter 4). Hence, non-customer-facing

investments that keep it on the leading edge of product performance are *starting* to take strategic priority over those process innovations that simply lower unit costs.

Overall, Samsung still appears to be content with fast following on industry-wide, communal cost-related process innovations. If Samsung faces a tradeoff is between investing money into expansions into a rapidly growing new areas where the strategic price of delay is very high and investing in industry-wide, not highly appropriable, cost-saving technologies (such as 450mm wafer technology), it is reasonable to argue that Samsung would tend to favor the former. If so, Samsung could be modeled as having heavier financial discounting profiles for 450mm technology (recall Explanation #5 earlier in this chapter), a possibility which will be explored in greater detail in the second half of this chapter.

A crystallization of the resolution of the long-term vs. short-term tensions within Samsung is given by Chang:

> "For example, presidents of Samsung Electronics' business divisions compete fiercely with each other to show higher performances. According to Samsung insiders, price negotiation across business divisions, for instance between Digital Media Division producing MP3 players and the Semiconductor Division producing flash memory, is so tough and even hostile that it is hard to believe that they belong to the same company. Sometimes the only way to resolve conflicts between them is to bring up the issues to the Group Secretary Office and eventually to Chairman Lee. It looks as if the synergy among Samsung's divisions depends entirely upon Chairman Lee and his Secretary Office." (Chang, 2008, location 2507/3514)

6.5.3 Samsung's Inter-firm Horizontal R&D Competition vs. Cooperation Behavior

Samsung shows clear evidence of being able to cooperate in R&D and capital-intensive settings in both semiconductors and other divisions when it is believes that such cooperation is in its best interest. However, it is clear that Samsung is cagey in its strategic evaluations regarding when this is in its best interests and in its negotiations and strategy execution.

First of all, it should seem natural that Samsung can effectively cooperate in some R&D situations because that is the basis for its success in acquiring technology as a fast follower (see the discussion in Section 6.5.1 above). However, Samsung has also demonstrated its ability and willingness to cooperate with other firms in situations of greater symmetry where both partners bring useful and distinct knowledge assets to the partnership.

One vivid example of this comes from the realm of LCD TVs. In 2004 Samsung entered into a long-term joint venture agreement with Sony Corporation for the production of LCD screens for the TV market (Mitchell 2010, Chapter 7; Gnyawali & Park 2011). Samsung secured a stable source of demand for capital-intensive LCD screen production and Sony secured technological advantage and a secure source of supply (see Mitchell 2010, location 3802/5615). Ultimately though, Samsung got the better end of the deal garnering more than 60% market share in large TV panels and displacing Sony for first place in overall TV market share by 2007 (see Mitchell 2010, location 3829/5615). This episode confirms Samsung's willingness to cooperate in large ventures and its cagey instincts in such situations.

Further afield from traditional electronics markets, we can see that Samsung is still (despite its tremendous size and prominence) partnering with companies which can help it ramp quickly in its ambitious pushes into new technology market arenas. For example, Samsung is partnering

with Bosch to help quickly ramp its expertise in Li-ion batteries for electric vehicles (The Economist 10/1/11(b)).

In semiconductor manufacturing there is also clear evidence that Samsung is willing to partner horizontally to share resources and speed R&D development. Samsung has been deeply involved in cross-company R&D for semiconductor manufacturing for a number of years with IBM and GlobalFoundries in the so-called "Common Platform Alliance". This horizontal alliance provides Samsung with manufacturing technology it would not have access to if it were not in an R&D alliance. In contrast, Samsung has tended to play a smaller financial role in alliances which help fund R&D among the equipment suppliers (e.g., it provided smaller funding amounts in very early stage EUVL development in the 1990s [Linden et al., 2000]). In such situations Samsung seems willing to partner to enhance its learning in semiconductors, but it seems determined to do so only at a minimum of cost. One could speculate that Samsung's decision to invest last among IST players and to take a smaller stake in the ASML co-investment program (ASML 8/27/13) is an indication of their approach to cost minimization and hard-fought negotiations in dealing with suppliers. Chang provides further evidence for Samsung's cost-sensitive approach to relationships with upstream suppliers: "Samsung Electronics' parts suppliers, including other Samsung Group affiliates, are also under great pressure to comply with Samsung Electronics' demands to lower costs and meet delivery deadlines." (Chang 2008, Location 2556/3514). While adopting partnering when unambiguously necessary/strategically prudent, there seems to be a relatively strong "go it alone" streak within the Samsung corporate psyche (especially relative to other Korean and East Asian firms) as illustrated by a quote from Kun-hee Lee in 2005: "Now, other companies will no longer teach or lend us their technologies. That means Samsung must now do everything on its own, from technology development to

establishing management systems. That process will be a lonely race." (Chang 2008, Location 2523/3514).

6.6 450mm R&D Investment Implications of the Samsung Behavioral Analysis

Clearly, many interesting behavioral trends can be uncovered through a detailed analysis of players' patterns of past action. One can use these types of qualitative behavioral observations as an *additional* tool to complement the game theory models presented in Chapters 4 and Chapter 5, as a stand-alone qualitative analysis and/or as a way to quantitatively refine payoff estimates for the players being modeled.

Given the evidence of Samsung's continued allegiance to a fast following strategy, strong elements of short-term financial control, and reticence and cost-sensitivity around semiconductor equipment R&D funding, it is reasonable to propose that financial impatience/impulsiveness might be *one of the reasons* behind the divergence discussed at the beginning of this chapter (i.e., Explanation #5 in Section 6.2 above). This does not rule out the possibility of the other explanations for which there is also some evidence in the qualitative analysis explored above, it simply creates a strong case that Explanation #5 is part of the overall explanation for the motivating divergence given at the beginning of this chapter. With that in mind, I will spend the remainder of this chapter explaining how this observation would translate into modifications (a.k.a. refinements) of Samsung's payoffs from the 450mm model developed in Chapter 5. Let us first explain more precisely what is meant by financial impatience and impulsiveness in this context.

6.7 Financial Impatience/Impulsiveness and Hyperbolic Discounting

One overarching conclusion from the qualitative analysis seems to be that Samsung's behavior patterns would require it to achieve especially high financial returns (i.e., E(NPV)) in order to justify investment in "strategically optional" situations, such as its choice to become involved early in 450mm equipment R&D funding. (However, this is entirely consistent with Samsung's strong and relentless approach to invest heavily in semiconductor capital/capacity expenditures – a "strategically crucial" set of investments in Samsung's eyes.) From the point of view of Samsung's 450mm investment decision in the existing (Chapter 5) model, this requirement of a high financial return translates into the assumption of a relatively high discount rate used to calculate E(NPV)s.

The most straightforward way to modify Samsung's payoffs given it requires a greater return on investment is to assume a higher discount rate universally across the time horizon of the model analysis (2011-2031). This assumption shall be termed greater Samsung "impatience" because it corresponds to a greater level of impatience across the time horizon to receive a high return on its investment. Note that this refinement is not directly analogous to the sensitivity analysis performed on the discount rate in Chapter 5 (Table 20) because that analysis assumed a changing discount rate common to all three players, whereas in the current analysis the discount rate is being increased for only Samsung.

Another possible way to refine Samsung's payoffs comes from the realm of behavioral economics. Instead of a universal increase in the annual discount rate across time, many studies of individuals indicate that they often discount the short-term very heavily (on an annual basis) and that they discount the long-term much less heavily (again on an annual basis). This

phenomenon is called hyperbolic discounting in the academic literature (e.g., see Ho et al. 2006). Within the applied context of Samsung's decision to invest early in 450mm, if Samsung is assumed to exhibit this behavior, I term it "impulsiveness". The difference between impatience and impulsiveness is illustrated in Figure 37, Figure 38, and Table 27 below.

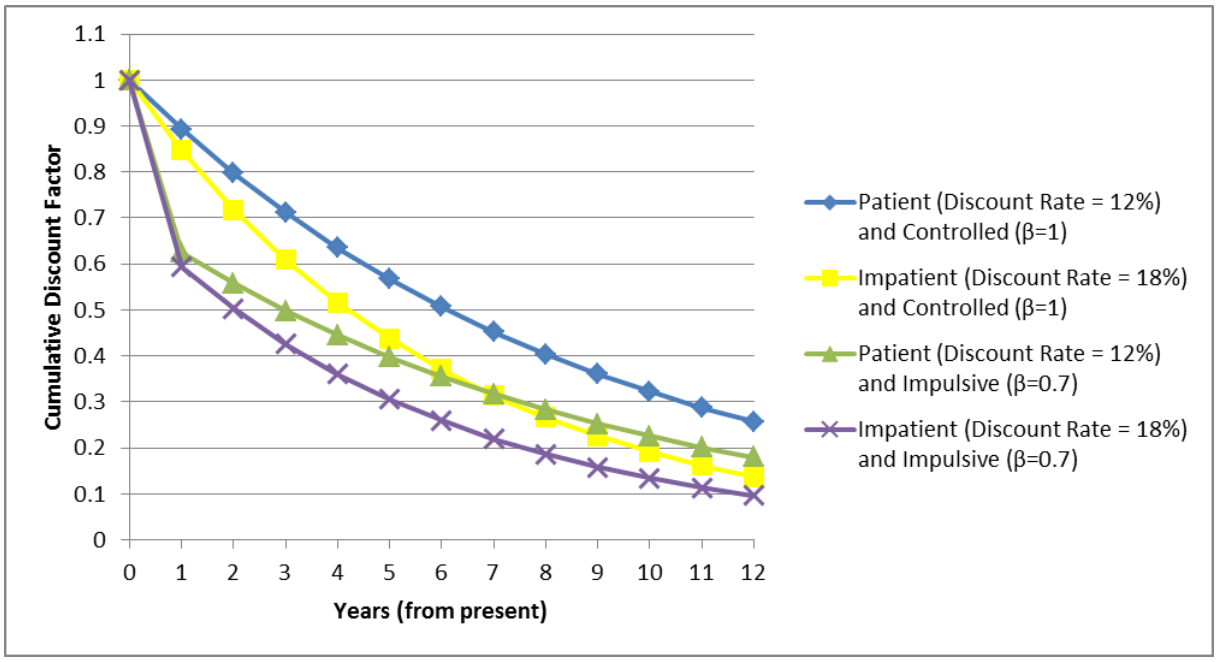


Figure 37: Cumulative Annual Discount Factor as Function of Discounting Behavior

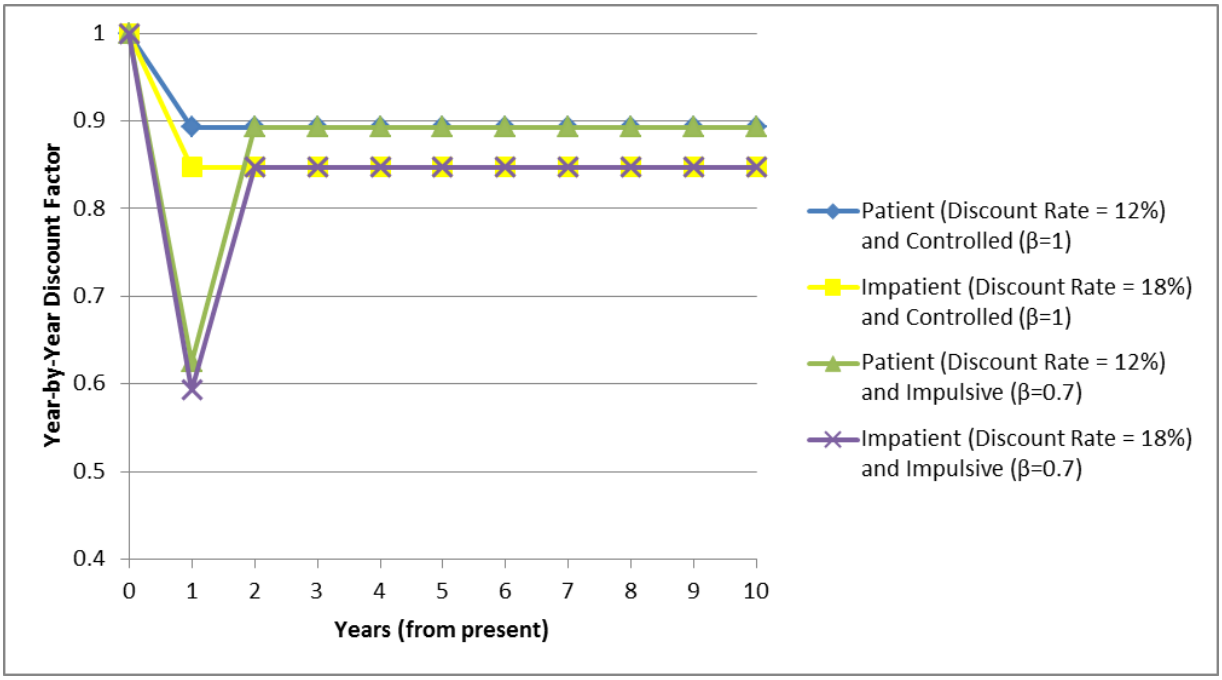


Figure 38: Year-by-Year Annual Discount Factor as Function of Discounting Behavior

Table 27: Characterization of Impatience and Impulsiveness Based on Discount Rates

		***Near Term* Discount Rate**	
		Low	**High**
***Overall/Average* Discount Rate**	**Low**	Controlled and Patient	Impulsive
	High	Impatient	Impatient and Impulsive

Figure 37 and Figure 38 above illustrate differences between exponential discounting (the typical assumption underlying E(NPV) analyses) and so-called quasi-hyperbolic discounting (the mathematical form used most frequently to approximate hyperbolic discounting behavior). Figure 37 shows that exponential discounting corresponds to a smoothly decreasing curve of the cumulative discount factor, whereas the quasi-hyperbolic curve has a noticeable kink in the cumulative discount factor curve in Year 1 (i.e., one year from the present, or t=1). Mathematically, the quasi-hyperbolic discounting is described by a "beta-delta" model in which the discount factor in year t (for $t \geq 1$) is given by:

$$Discount\ Factor_{Beta-delta,t} = \beta\delta^t \tag{6.1}$$

where β and δ are both parameters lying between 0 and 1. The implications of this can be most easily seen in Figure 38. The annual discount factor in Year 1 is $\beta \cdot \delta$ while the annual discount factor in all subsequent years is δ. This gives rise to so-called "time inconsistent" preferences since as time progresses it is possible (even if no additional information is received) for a decision maker to change his or her mind regarding the wisdom of an investment. This reversal of a decision is something which cannot mathematically occur in exponential discounting (again

assuming no additional information is received). An individual that displays hyperbolic discounting is also said to exhibit a "present bias" due to the steep drop off in the discount factor immediately after the present. Table 27 provides a high-level summary of how the terms impatient and impulsive map onto near-term and overall (i.e., average across the analysis horizon) discount rates.

Although it is difficult to empirically distinguish between these two forms of "heavier" discounting (i.e., impatience and impulsiveness) which might characterize Samsung's behavior, it is theoretically possible with careful analysis to do so. (See Angeletos et al. 2001 for a discussion of the empirical measurement of hyperbolic discounting for individuals. Ho et al. [2006] contend that the same kind of analysis is also applicable to firms as well.) In the context of this dissertation, I am not going to try to determine which of these two types of heavier discounting better characterizes Samsung's 450mm behavior; I am simply going to demonstrate, for completeness of illustration, the implications for Samsung's payoffs and the game's Nash Equilibria of moderate levels of both types of discounting.

6.7.1 Empirical Studies of Quasi-Hyperbolic Discounting

Table 28: Sample of Empirically Measured Literature Beta and Delta Parameters

Beta	Delta	Subjects Studied	Article	Authors	Journal/Date
0.48 - 0.61	Not reported	Representative US National sample (N=2,914)	Estimating discount rates for **environmental quality** from utility-based choice experiments	Viscusi et al.	Journal of Risk and Uncertainty, 2008
0.7	0.957	Authors' choice based on empirics of **US savings behaviors**	The Hyperbolic Consumption Model: Calibration, Simulation, and Empirical Evaluation	Angeletos et al.	The Journal of Economic Perspectives, Summer 2001
0.63-0.88	0.957-0.962	Authors' choice based on empirics of **US savings behaviors**	Estimating Discount Functions with Consumption Choices over the Lifecycle	Laibson et al.	American Economic Review (2007)
0.5-0.8	Not reported	**Credit card customers** in the US (N= ~5000)	Time Inconsistency in the Credit Card Market	Shui & Ausubel	Working Paper, 2005
0.338	0.88	**Single women with children** from the National Longitudinal Surveys (1979)	Time-inconsistency and Welfare Program Participation: Evidence from the NLSY	Fang and Silverman	International Economic Review (Nov. 2009)

Table 28 above summarizes beta and delta values gleaned from the nascent (but growing) set of empirical studies of humans' time discounting preferences. One can see that the beta and delta values vary quite a bit (as do the nature of the subjects studied).

I used this range of values to inform the choice of discount rates illustrating how impulsiveness could impact Samsung's 450mm investment decision. In particular, to ensure modeling conservatism given the "mixed" nature of the traits of Samsung described above, I applied only the more moderate levels of impulsiveness (i.e., quasi-hyperbolic discounting) to Samsung's

decision. Specifically, I considered values such that $0.7 \leq \beta \leq 1.0$ (note from Equation 6.1 that $\beta=1$ corresponds to "normal" exponential discounting).

I also only entertain moderate hyperbolic discounting for Samsung because it is a large, sophisticated company that uses cash flow and NPV analysis (see Chang 2008, location 2058/3514). However, Samsung does have a centrally controlled organizational structure that can lead to questionable decision making (e.g., see Lee and Lee [2007] for a discussion about Samsung's ill-advised and ill-fated extended foray in automobile manufacturing).

It is almost certain that for a \$2B investment decision (recall that $I_{Samsung}$ = \$2B in Table 12), the decision will rest with the Samsung Group Chairman (currently Kun-hee Lee), lending more credence to the notion that Samsung's investment behavior, for very large strategic issues, can be reasonably conceived of as if the decision were being made by an individual person (and hence, at least on this basis, could be construed as consistent with the empirical quasi-hyperbolic discounting studies summarized in Table 28 above).

6.8 Refinements to Samsung's Payoffs Due to Impatience/Impulsiveness

Recall that Figure 36 in Section 6.1 highlights the two Samsung payoffs under scrutiny here. Note that because Intel and TSMC have dominant strategies in this game (assuming no behavioral adjustments to Intel's or TSMC's payoffs), we do not need to look for NE in areas other than the two outcome boxes (I,I,I) and (I,D,I). Regardless of Samsung's payoffs, one of these two outcomes (assuming no strict equalities among Samsung's payoffs) will be the unique NE of the game. Of course, given the simultaneous nature of the game as formulated, the same discounting practices (i.e., the same level of impatience/impulsiveness should be applied to all eight of Samsung payoff estimates for consistency). Table 29 through Table 33 below provide a

detailed exploration of the impact that a moderate amount of impatience and/or impulsiveness by Samsung would have on its incentive to invest early in 450mm (assuming that it believes that Intel and TSMC intend to invest). For ease of reference, I label these five analyses as Analysis #6.1 through Analysis #6.5.

Table 29: Analysis #6.1: Samsung's Incentive to Invest in 450mm, Given Intel and TSMC Invest and Exponential Discounting (With Base Case 12% Discount Rate)

		E(NPV) in $B USD					
Scenario assumptions:		**All competition among I,S, and T**	**Δ**	**50/50 mix of competition types among chipmakers**	**Δ**	**All competition between I,S, and T and the smaller chipmakers**	**Δ**
1 year time lag 1.5% MS contestable	$E(NPV)_{Samsung,\ Invest}$	3.2	**2.8**	4.0	**1.8**	4.8	**0.8**
	$E(NPV)_{Samsung,\ Don't\ Invest}$	0.4		2.2		4.0	
2 year time lag 1.5% MS contestable	$E(NPV)_{Samsung,\ Invest}$	3.2	**2.8**	4.0	**2.1**	4.8	**1.4**
	$E(NPV)_{Samsung,\ Don't\ Invest}$	0.4		1.9		3.4	
2 year time lag 2.0% MS contestable	$E(NPV)_{Samsung,\ Invest}$	3.2	**3.8**	4.3	**2.9**	5.3	**1.9**
	$E(NPV)_{Samsung,\ Don't\ Invest}$	-0.6		1.4		3.4	
2 year time lag 2.5% MS contestable	$E(NPV)_{Samsung,\ Invest}$	3.2	**4.8**	4.5	**3.6**	5.8	**2.4**
	$E(NPV)_{Samsung,\ Don't\ Invest}$	-1.6		0.9		3.4	

Table 30: Analysis #6.2: Samsung's Incentive to Invest in 450mm, Given Intel and TSMC Invest and Exponential Discounting (18% Discount Rate)

		E(NPV) in $B USD					
Scenario assumptions:		**All competition among I,S, and T**	**Δ**	**50/50 mix of competition types among chipmakers**	**Δ**	**All competition between I,S, and T and the smaller chipmakers**	**Δ**
1 year time lag 1.5% MS contestable	$E(NPV)_{Samsung,\ Invest}$	1.1	**0.9**	1.6	**0.4**	2.1	**-0.1**
	$E(NPV)_{Samsung,\ Don't\ Invest}$	0.2		1.2		2.2	
2 year time lag 1.5% MS contestable	$E(NPV)_{Samsung,\ Invest}$	1.1	**0.9**	1.6	**0.6**	2.1	**0.3**
	$E(NPV)_{Samsung,\ Don't\ Invest}$	0.2		1.0		1.8	
2 year time lag 2.0% MS contestable	$E(NPV)_{Samsung,\ Invest}$	1.1	**1.4**	1.8	**1.1**	2.4	**0.6**
	$E(NPV)_{Samsung,\ Don't\ Invest}$	-0.3		0.7		1.8	
2 year time lag 2.5% MS contestable	$E(NPV)_{Samsung,\ Invest}$	1.1	**2.0**	1.9	**1.4**	2.7	**0.9**
	$E(NPV)_{Samsung,\ Don't\ Invest}$	-0.9		0.5		1.8	

Table 31: Analysis #6.3: Samsung's Incentive to Invest in 450mm, Given Intel and TSMC Invest and Mild Quasi-Hyperbolic Discounting (β=0.9, and δ corresponding to 18% Discount Rate)

		E(NPV) in $B USD					
Scenario assumptions:		**All competition among I,S, and T**	**Δ**	**50/50 mix of competition types among chipmakers**	**Δ**	**All competition between I,S, and T and the smaller chipmakers**	**Δ**
1 year time lag 1.5% MS contestable	$E(NPV)_{Samsung,\ Invest}$	0.8	**0.6**	1.3	**0.2**	1.7	**-0.3**
	$E(NPV)_{Samsung,\ Don't\ Invest}$	0.2		1.1		2.0	
2 year time lag 1.5% MS contestable	$E(NPV)_{Samsung,\ Invest}$	0.8	**0.6**	1.3	**0.4**	1.7	**0.1**
	$E(NPV)_{Samsung,\ Don't\ Invest}$	0.2		0.9		1.6	
2 year time lag 2.0% MS contestable	$E(NPV)_{Samsung,\ Invest}$	0.8	**1.1**	1.4	**0.7**	2.0	**0.4**
	$E(NPV)_{Samsung,\ Don't\ Invest}$	-0.3		0.7		1.6	
2 year time lag 2.5% MS contestable	$E(NPV)_{Samsung,\ Invest}$	0.8	**1.6**	1.5	**1.1**	2.2	**0.6**
	$E(NPV)_{Samsung,\ Don't\ Invest}$	-0.8		0.4		1.6	

Table 32: Analysis #6.4: Samsung's Incentive to Invest in 450mm, Given Intel and TSMC Invest and Moderate Quasi-Hyperbolic Discounting (β=0.7, Discount Rate =18%)

		E(NPV) in $B USD					
Scenario assumptions:		**All competition among I,S, and T**	**Δ**	**50/50 mix of competition types among chipmakers**	**Δ**	**All competition between I,S, and T and the smaller chipmakers**	**Δ**
1 year time lag 1.5% MS contestable	$E(NPV)_{Samsung, Invest}$	0.2	**0.0**	0.5	**-0.4**	0.9	**-0.6**
	$E(NPV)_{Samsung, Don't Invest}$	0.2		0.9		1.5	
2 year time lag 1.5% MS contestable	$E(NPV)_{Samsung, Invest}$	0.2	**0.1**	0.5	**-0.2**	0.9	**-0.4**
	$E(NPV)_{Samsung, Don't Invest}$	0.1		0.7		1.3	
2 year time lag 2.0% MS contestable	$E(NPV)_{Samsung, Invest}$	0.2	**0.4**	0.6	**0.1**	1.1	**-0.2**
	$E(NPV)_{Samsung, Don't Invest}$	-0.2		0.5		1.3	
2 year time lag 2.5% MS contestable	$E(NPV)_{Samsung, Invest}$	0.2	**0.8**	0.7	**0.4**	1.3	**0.0**
	$E(NPV)_{Samsung, Don't Invest}$	-0.6		0.3		1.3	

Table 33: Analysis #6.5: Samsung's Incentive to Invest in 450mm, Given Intel and TSMC Invest and Moderate Quasi-Hyperbolic Discounting (β=0.7, Discount Rate =16%)

		E(NPV) in $B USD					
Scenario assumptions:		**All competition among I,S, and T**	**Δ**	**50/50 mix of competition types among chipmakers**	**Δ**	**All competition between I,S, and T and the smaller chipmakers**	**Δ**
1 year time lag 1.5% MS contestable	$E(NPV)_{Samsung, Invest}$	0.6	**0.4**	1.0	**0.0**	1.4	**-0.5**
	$E(NPV)_{Samsung, Don't Invest}$	0.2		1.0		1.9	
2 year time lag 1.5% MS contestable	$E(NPV)_{Samsung, Invest}$	0.6	**0.4**	1.0	**0.1**	1.4	**-0.2**
	$E(NPV)_{Samsung, Don't Invest}$	0.2		0.9		1.6	
2 year time lag 2.0% MS contestable	$E(NPV)_{Samsung, Invest}$	0.6	**0.9**	1.1	**0.5**	1.6	**0.0**
	$E(NPV)_{Samsung, Don't Invest}$	-0.3		0.6		1.6	
2 year time lag 2.5% MS contestable	$E(NPV)_{Samsung, Invest}$	0.6	**1.4**	1.2	**0.8**	1.9	**0.3**
	$E(NPV)_{Samsung, Don't Invest}$	-0.8		0.4		1.6	

Table 34 below summarizes the results from the five analyses presented in Table 29 through Table 33. Specifically, we can see that these assumptions about the type of discounting behavior and the values of specific discounting parameters can toggle Samsung's investment decision from a robust incentive to invest (Analysis #6.1) to a tenuous incentive to invest (Analysis #6.2, #6.3, and #6.5) to a complete disappearance of any incentive to invest (Analysis #6.4). Thus, the conclusion is that Samsung's investment incentive wanes significantly if Samsung is thought to exhibit impatience, impulsiveness, or some combination of both.

Table 34: Results Summary of Table 29 through Table 33

Analysis#	**Table #**	**Discounting Type**	**Discounting Parameters**	**Summary of Samsung's Incentive to Invest:**
6.1	Table 29	Exponential	Disc. Rate = 12%	Robust incentive to invest across all possible situations ($0.8B-$4.8B)
6.2	Table ***30***	Exponential	Disc. Rate = 18%	Tenuous incentive to invest in many situations (especially for short time lag, low contestable market, and high IST-to-smaller chipmaker competition)
6.3	Table 31	Quasi-Hyperbolic	$\beta = 0.9$; Subsequent Disc. Rate = 18%	Even more tenuous incentive to invest than Scenario #6.2. Most situations yield incentive ≤ $0.7B.
6.4	Table 32	Quasi-Hyperbolic	$\beta = 0.7$; Subsequent Disc. Rate = 18%	Incentive to invest has disappeared. More than half of cases considered have either no incentive or have a disincentive to invest.
6.5	Table 33	Quasi-Hyperbolic	$\beta = 0.7$; Subsequent Disc. Rate = 16%	Very tenuous incentive to invest in most situations (especially for short time lag, low contestable market, and high IST-to-smaller chipmaker competition)

Given this analytical overview, let us now provide a graphical representation of how impulsiveness (a.k.a., "present bias") on the part of Samsung could toggle its decision toward not investing early in 450mm technology. Figure 39 through Figure 41 below illustrate this effect. (Note that the light and dark colored stars in these figures indicate correspondences of the Samsung payoffs being analyzed to those highlighted in Figure 36). Holding δ constant, these

figures show how Samsung's two relevant payoff estimates vary as a function of β (the "impulsiveness parameter"). In Figure 39 (corresponding to Scenario #5.3) one can see that as impulsiveness increases (within the [0.7,1] range decided upon in Section 6.7.1), Samsung's incentive to invest early in 450mm technology is reduced by more than half. In Figure 40 (corresponding to Scenario #5.4) one can see that as impulsiveness increases to β=0.7, Samsung's incentive to invest disappears completely. Finally, in Figure 41 (corresponding to Scenario #5.3, with greater impatience factored in), Samsung's incentive to invest switches to become a noticeable disincentive to invest as we assume a more impulsive Samsung.

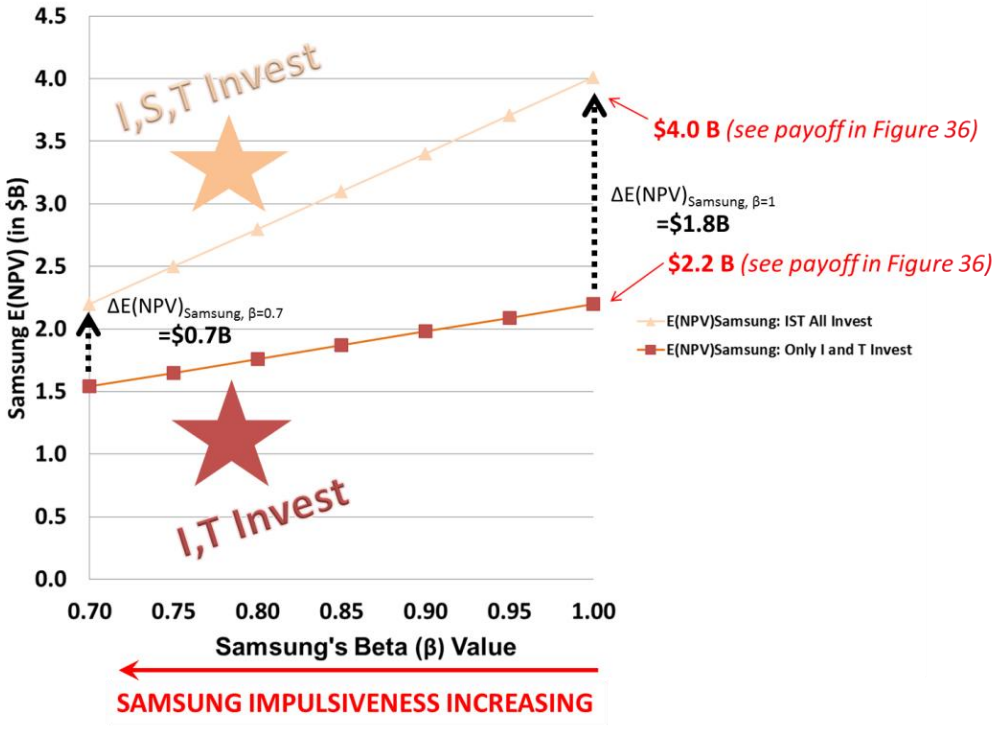


Figure 39: Impact of Samsung β-parameter on Samsung's Incentive to Invest (β=1, Corresponds to Scenario #5.3. Discount Rate = 12%)

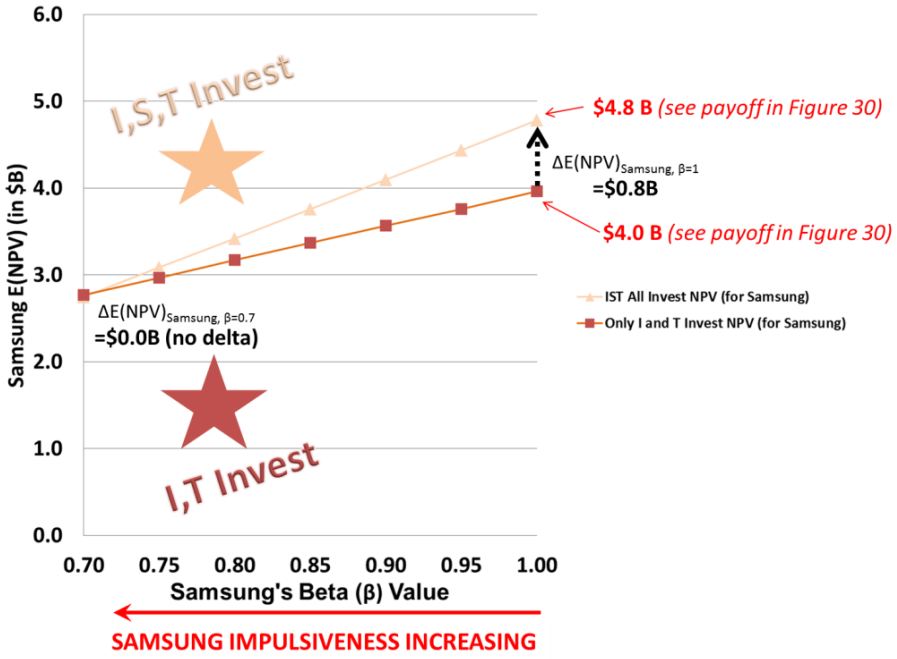


Figure 40: Impact of Samsung β-parameter on Samsung's Incentive to Invest (β=1, Corresponds to Scenario #5.4. Discount Rate = 12%)

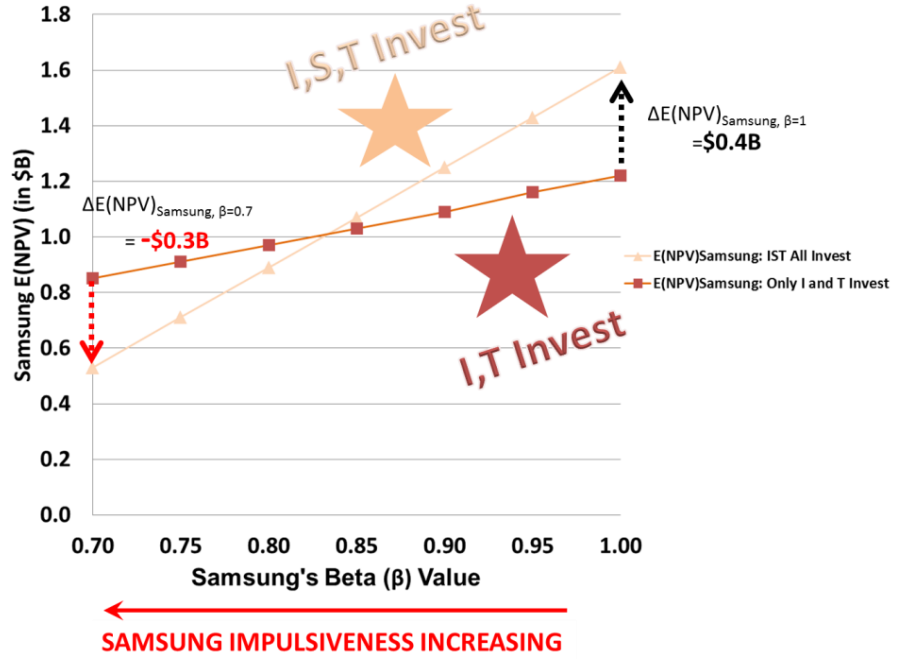


Figure 41: Impact of Samsung β-parameter on Samsung's Incentive to Invest (β=1, Corresponds to Scenario #5.3, except that Discount Rate = 18%)

6.9 Chapter Summary

To recapitulate, the qualitative analysis in Sections 6.4 through 6.6 strongly suggested that Samsung might be impatient and/or impulsive regarding their future flow of benefits from early investment in 450mm R&D. I showed (in Table 29 through Table 33 and Figure 39 through Figure 41) that whether one assumes a moderate level of impatience or a moderate level of impulsiveness (or a combination of both), Samsung's robust incentive to invest (given that Intel and TSMC are planning to invest) vanishes in many of the scenarios from Chapter 5. This provides a quantitative payoff refinement from *one possible explanation* (among several posited) to reconcile the divergence between Chapter 5's 450mm model results and the general sense that (to date) Samsung seems quite reticent to invest in early 450mm equipment R&D.

I have demonstrated the relative ease of incorporating behavioral refinements games of complete information with standard exponential discounting. One significant limitation of employing the refinements here is deciphering which refinements should and should not be incorporated into the models. Another challenge which generally intensifies with the inclusion of more nuanced payoff calculation refinements is that the model outcomes (including the equilibria) rest even more heavily on the game-theoretic assumptions of common knowledge necessary to maintain the game as one of complete information (with the attendant straightforward game predictions and interpretations).

In terms of managerial practice, another consideration for these models is that adding extra behavioral factors can either encourage a manager to accept the model results because he or she believes it captures more of the realism of the actual situation *or* adding these additional factors can dissuade a manager from using these models because the additions cause a loss of

managerial transparency and traceability which managers tend to desire for strategically important quantitative financial models (e.g., see Little 2004). Which of these forces in tension with each other wins out may be a function of a number of factors, including an organization's comfort level with using game theory analysis for strategy development (see Papayoanou 2010 for more discussion of this point).

Thus, from a practice standpoint there seem to be two modeling options for implementing rigorous behavioral analyses of the strategic players. The first option is to present the game theory analysis without any special behavioral refinements (e.g., simply as the model in Chapter 5) and summarize the rigorous qualitative analysis separately as an add-on set of stand-alone considerations. The second option is to present the quantitative game theory analysis incorporating a few justified behavioral payoff refinements with detailed managerial instruction regarding how to interpret these refinements. (In this case, retaining the add-on stand-alone qualitative analysis is likely to still be beneficial.)

In any event, whether payoff calculation refinements such as those shown in this chapter are incorporated in one's modeling efforts or not, the process for doing a detailed "outside looking in" qualitative analysis of the other firms' behaviors will often reveal new trends (or crystallize tentatively understood trends) and tendencies of the other strategic players. In all situations there will still exist a very wide latitude toward and necessity for the "managerial decision-making art" of stitching together quantitative models (Chapters 4 and 5), rigorous qualitative analysis (this chapter), and hard won managerial context and intuition.

The next chapter will summarize the overall findings of the dissertation, including attempting to identify the broad industry and technology characteristics which determine when parsimonious game theoretic modeling will be most fruitful for strategic decision-making.

Chapter 7: Final Conclusions and Summary of Contributions

7.1 Summary of Research Contributions

7.1.1 Methodology Contribution: Decision-Making Tool for Oligopolistic Business Strategy

This dissertation makes a contribution to the application of game theory by developing and documenting an iterative procedure for game theoretic quantitatively-grounded strategy development. Specifically, it illuminates the process of parsimoniously choosing players, their available actions, and the payoff sub-components for inclusion in strategic models. This work demonstrates how triangulation among various secondary data sources can be iteratively married with realism checking by industry experts to arrive at validated game structures and payoffs. It also adds to the managerial practice literature by clarifying the tradeoff between model completeness and model simplicity in such contexts (in the spirit of Little 2004).

Within such parsimonious game theory models, the dissertation illustrates how robustness checks (i.e., simultaneous vs. sequential game reformulation in Section 4.9) and sensitivity analysis (i.e., NE shift cutoffs in Sections 4.10 and 5.5) can be effectively performed. Finally, the dissertation shows how rigorous qualitative analysis of a firm's behavioral patterns can be melded into quantitative payoff estimation (Section 6.8).

7.1.2 Domain Contributions: Supply Chain R&D Strategy

This dissertation also sheds new light on the conditions under which large manufacturers should invest in R&D performed at their equipment suppliers during large tightly-coupled technology transitions. It provides a detailed real-world case of when it is in the best interests of

manufacturers to embrace a single supplier in technology transitions in concentrated industries, even when there is a possibility of two suppliers, given extreme technological difficulty of the transition (EUVL – Chapter 4). This work has also shown in a contextually-realistic manner the interplay of economic incentives experienced by multiple large manufacturers during large "communal" technology transitions (450mm – Chapters 5 and 6). I have demonstrated, based on the nature of competition and the level of difficulty encountered by fast following firms, that the incentives could support universal early investment (Scenarios #5.2 to #5.4 and #5.6 to #5.8) or free-riding on the early investments of others (Scenarios #5.0, #5.1, and #5.5).

7.1.3 Domain Contributions: Ongoing Semiconductor Manufacturing Transitions

Specifically within the industrial domain of semiconductor manufacturing, this dissertation provided strategic insight for the ongoing EUV and 450mm wafer transitions. It added quantitative rigor to the body of qualitative studies of the economic and technological evolution of the photolithography equipment industry, a well-studied industry at the very heart of Moore's Law technology improvements (Chapter 4). Similarly, this dissertation contains among the first detailed attempts at the detailed quantification of the strategic interactions at play during wafer-size transitions, a very important process in the ongoing cost-reductions for global semiconductor production (Chapters 5 and 6).

7.2 Research Motivation, Methodology, and Industry Context

In this dissertation I explored applying game theoretic models to the domain of R&D investments for large, complex technology transitions. Technology transitions that are tightly-coupled (across firm boundaries) occurring in highly concentrated industries lend themselves to the identification of a small number of key strategic players, each with a relatively delimited set

of "general strategies". These traits suggest that such industrial technology transitions may be ripe for the application of relatively simple game theoretic models to generate and clarify strategic insight.

While these types of models could be applied to a number of different industries (as discussed in Chapter 1), I focused on two current semiconductor industry technology transitions (EUV lithography and 450mm diameter wafers) for deep study and model development, as motivated in Chapter 3. I have also described in greater detail the multi-data source methodology employed in this research which iteratively triangulated toward quantitative strategic models with increasing levels of fidelity (Chapter 2). The bulk of the modeling and analysis was then provided in Chapters 4 through 6.

7.3 EUVL Model Conclusions (Chapter 4)

The EUVL model predicted that the wisdom of investment (approximated at $1B) by the Chipmakers in ASML's EUVL program is quite robust to changes in EUVL outlook and robust to many (but not all) model parameter changes within plausible ranges. The model allowed me to quantify the moderate degree to which the Chipmakers' investment in ASML bolstered ASML's incentive to invest (assuming that Nikon would not invest) and highlighted the fact that any efforts (besides direct financial assistance) which reduced ASML's risk level should also be considered.

According to the model, it seems likely that Nikon will choose not to invest unless they receive considerable financial assistance (from Chipmakers or others) *and* they have a quite optimistic outlook for the implementation timeline of EUVL technology. Hence, the clear prediction (i.e., SPNE) of the model was ('Finance ASML', 'Invest', 'Don't Invest'). The "runner up" SPNE

outcome from the overall model analysis was ('Finance both', 'Invest', 'Invest'). However, in reality, this equilibrium outcome would entail a very high degree of technological optimism about EUV lithography technology and considerably greater risk for both Chipmakers and Nikon, not to mention considerable additional coordination costs among the players (recall these discussions in Sections 4.5.2 and 4.7.1).

A series of five publicly announced lithography investment decisions in 2012 were solidly consistent with the ('Finance ASML', 'Invest', 'Don't Invest') equilibrium outcome predicted by the model (Section 4.7.2). This correspondence between model and reality is one of the main results of the dissertation; it suggests some measure of predictive power for the types of parsimonious models presented. Although the model has considerable sensitivity to model input parameters and explicitly does not include some potentially strategically important considerations, it does seem to capture the underlying economic dynamics of this technology investment decision in a cognitively efficient manner that fosters intra-firm and inter-firm communication and decision-making as well.

7.4 450mm Model Conclusions (Chapter 5)

In this dissertation I also developed a contextually-realistic game theory model which illuminates the action-reaction dynamics among Intel, Samsung, and TSMC regarding early investment in 450mm technology. The model framework was relatively simple, making it reasonably transparent to the relevant decision makers in order to encourage its practical industrial use.

Rooted in the strategic industrial context, the model provides insight into which assumptions and parameters are most crucial for the largest chipmakers' early 450mm involvement, highlighting when all three are likely to invest and when only one or two is likely to do so. The model

indicates that assuming virtually all reasonable model parameters, there is an incentive for at least one of Intel, Samsung, and TSMC to invest early in 450mm technology. However, the overall modeling outcome is not entirely conclusive. Although the "All Invest" outcome is the most common equilibrium outcome of the various scenarios examined, for scenarios which assume weak (or no) market share impacts from early investment in 450mm, the game often has multiple equilibria in which not all three chipmakers choose to invest early. Despite this, the model does have moderate face validity and it crystallizes managerial thinking about the economic incentives of the three largest chipmakers.

As of the writing of this dissertation (in early 2013), the bulk of the 450mm spending is still in the future (McGrath 7/11/12), and thus no stark confirmatory/disconfirmatory evidence (as was seen for EUVL) yet exists. So far, it appears that the industry is taking a highly consortial approach (heavily centered around the new consortium, G450C) which seems to be advancing 450mm technology in a relatively slow and sure-footed way without dramatically large outlays on the part of either the chipmakers or the equipment suppliers (Krzanich 2011).

The 450mm model developed in Chapter 5 illustrates (especially in concert with the more robust results and confirmatory evidence from the EUVL model) to decision makers in firms and consortia the power of game theory as an *additional* tool to provide insight and aid strategic decision-making in an important subset of highly impactful, complex business situations. A number of alternative game theoretic formulations (beside the well-understood 3-player simultaneous game model developed in Chapter 5) could be explored in future research efforts to achieve a higher level of modeling fidelity.

7.5 Behavioral Analysis and Payoff Refinement Conclusions (Chapter 6)

Psychological and organizational factors within firms not accounted for in the player payoff estimates in Chapter 5 seem to be clearly relevant to the 450mm R&D decisions. These factors motivated a detailed analysis of Samsung's historical behavioral traits (especially as they might impact their decision to invest early in 450mm technology) and related possible modifications to Samsung's payoffs, topics explored in depth in Chapter 6.

I analyzed Samsung's behavior at multiple levels of the organization (e.g., Samsung Group, Samsung Electronics, and Samsung Electronics's semiconductor division). The analysis focused most intensely on three factors most relevant to Samsung's 450mm investment decision: fast-following vs. leading, short-term vs. long-term investment horizon, and horizontal inter-firm R&D competition vs. cooperation. The overarching conclusion was that Samsung likely had some moderate level of "financial impatience/impulsiveness" regarding early investment in 450mm. These two terms were defined more precisely, and methods of quantifying their impact (drawn from the behavioral economics literature) were developed. I demonstrated that assuming moderate levels of such impatience/impulsiveness could toggle Samsung's economic incentives for early investment in 450mm technology from "robust investment" to "ambivalence" to even "moderate disincentive to invest". My analysis showed that *one possible explanation* (among several posited) could plausibly reconcile the divergence between Chapter 5's 450mm model results and Samsung's (initial) apparent reticence to invest early in 450mm equipment R&D.

It is relatively easy to incorporate such behavioral refinements into the complete information game frameworks developed in Chapters 4 and 5. One should be cautious however when mustering evidence regarding which refinements should and should not be incorporated into the

models. In terms of managerial practice, the inclusion of such refinements is a double-edged sword. On the one hand, they may encourage more managerial buy-in to the model (due to greater model fidelity). On the other hand, they may discourage buy-in (due to a loss of managerial transparency and traceability).

Whether payoff calculation refinements such as those developed in Chapter 6 are incorporated in one's modeling efforts or not, the process for performing detailed qualitative (and allocentric) analysis often reveals or crystallizes behavioral trends and tendencies of the other key firms. Regardless of the inclusion or non-inclusion of behavioral refinements in the quantitative payoff estimates, there remains ample room for hard won experience-based managerial insight and intuition.

7.6 Characteristics of Technology Transitions Conducive to Parsimonious Game Theoretic Modeling

This dissertation started off with a general research question of whether useful quantitative strategic models could be developed productively under a set of loosely delineated criteria regarding industry structure and technology conditions (see Section 1.1). After having labored to iteratively develop quite detailed game theoretic models in Chapters 4 through 6 in a single industrial setting, it is now productive to revisit these criteria anew in light of the difficulties encountered and experience gained. In this vein, Table 35 and Figure 42 and Figure ***43*** below propose a more complete set of criteria which help specify the scope of generalizability of this approach to other strategic R&D financing contexts.

Table 35: Factors Determining the Usefulness of Parsimonious Game Theory Analysis

Condition within industry and technology and/or technology transition:	***Usefulness of Parsimonious Game Theory Models***	
	Higher	***Lower***
R&D intensity of transition (e.g., technology's R&D costs/annual industry profits)	High	Low
Number of (maximally distilled) strategic players or coalitions	2 or 3	1, 5+
Number of tiers of value chain containing strategic players	1-2	3+
Difficulty of new market entry	High	Low
Maturity of industry	High	Low
Technology is "monolithic"? (i.e., consists of a well-delineated cross-industry production platform)	Yes	No
Appropriability of technological innovations	Medium/High	Low
Technology development is fundamentally "communal" in nature?	No	Yes
Industry's heritage includes highly of data-driven strategic decisions?	Yes	No

Table 35 above augments the criteria outlined in Chapter 1 by adding: the modeling sweet spots in terms of number of key strategic players and value chain tiers considered, whether the technology is "monolithic" or not, the appropriability of the technological innovations, and the industry's heritage in making data-driven strategic decisions. These criteria did not spring obviously to mind at the start of the research project, yet they became clear through the course of the modeling effort. Focusing on the first two rows of Table 35, the diagram in Figure 42 below is a proposal for the approximate conditions under which various quantitative strategic modeling approaches seem most tractable and useful. Parsimonious game theoretic modeling (of the type developed in this thesis) occupies the region with two or three strategic players and with relatively high R&D intensity of the technology transition. The possibility when more than three

players are considered (discussed briefly in Section 5.6.3) include weakest link and cooperative game theory models. Within the context of this modeling roadmap, it is interesting to consider where the EUVL and 450mm transitions (and their historical predecessors) reside. Figure 42 below shows this, highlighting the possibility that a 450mm model with greater fidelity might be developed in the future if more strategic players are modeled.

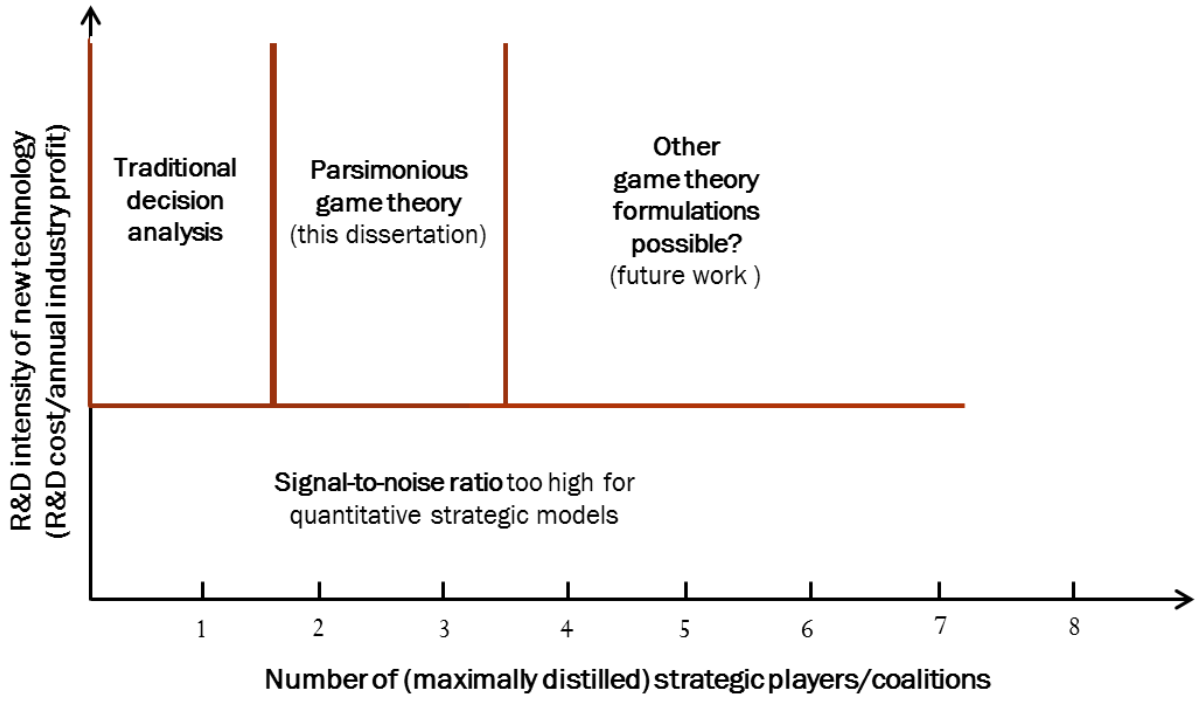


Figure 42: Proposed Conditions for Usefulness of Parsimonious Game Theory Models

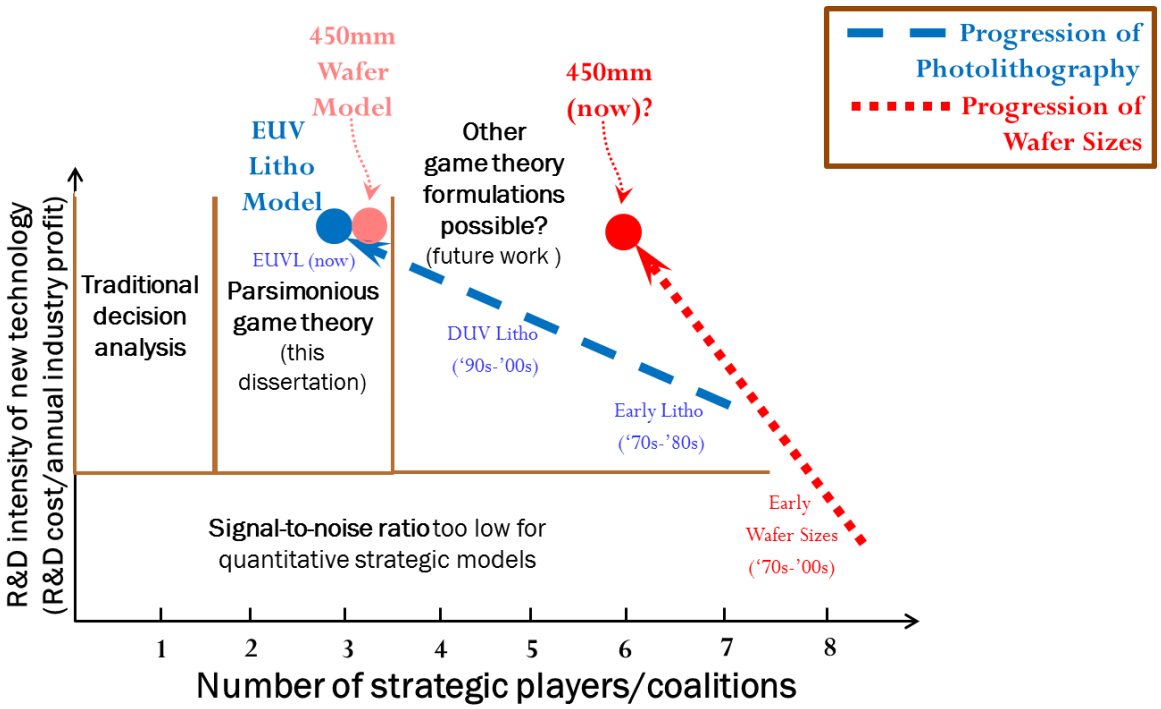


Figure 43: Schematic Historical Trajectories of Photolithography and Wafer-Size Transitions

7.7 Benefits of Parsimonious Game Theoretic Modeling for Managerial Practice

In addition to their predictive value, parsimonious game theory models have a number of significant benefits when viewed from the standpoint of managerial practice. Although some of these have been mentioned throughout the course of the dissertation, it is worth distilling them into one list for future reference. These benefits are summarized in Table 36 below.

Table 36: Summary of Benefits of Parsimonious Game Theoretic Modeling for Managerial Practice

Benefits of Parsimonious Game Theoretic Modeling for Managerial Practice
• *Clarity of strategic thought.* Forges internal consensus and motivates execution around it.
• *Avoidance of strategic myopia.* Helps strategist "See the whole picture" guiding the strategic interactions of interest.
• *Cognitive economy.* Conveys large amounts of information in a compact manner.
• *Ease of sensitivity analysis.* Enables deep insight regarding which conditions might change a player's decision.
• *Tool to enable "changing the game".* Creates clear starting point for analysis of strategic options which entail fundamentally changing the rules or structure of the game as currently conceived.
• *Ability to reason clearly with other firms about industry transitions.* Provides a shared space for productively discussing cooperation. These models also tend to effectively highlight the need for realism in industry-wide roadmaps.

7.8 Limitations of Parsimonious Game Theoretic Modeling

When appropriately constructed, parsimonious game theory models help predict outcomes and provide the managerial practice benefits noted above. However, there are clearly a number of important limitations of these models as well. Although some of these have been mentioned throughout the course of the dissertation, it is worth distilling them into one list for future reference. These limitations are summarized in Table 37 below.

Table 37: Summary of Limitations of Parsimonious Game Theoretic Modeling

Limitations of Parsimonious Game Theoretic Modeling
• *Over-reliance on "common knowledge" for outcome predictions.* There is a long-standing debate among economic researchers about how important common knowledge assumptions are. The reality is that this depends on the specific context of the decision. Models which do not rely on common knowledge are possible, but they add significant complexity.
• *Non-uniqueness of Nash Equilibria.* In some situations, parsimonious game theory of the type developed in this dissertation does not yield a unique prediction.
• *Signal-to-noise ratio.* In many situations there is simply not high enough signal-to-noise to make these models work. Suitable situations can be found by applying the suitability criteria outlined in Table 35 and Figure 42. However, one should avoid succumbing too easily to signal-to-noise limitations on game theory's applicability to strategic issues.

• *Difficulty of defining appropriate model boundaries.* Care must be taken to model the strategic situations in a manner which retains the essential economic character of the interactions. Often, business strategists encounter a "game within a game" or "linked games"; in such situations, it can be difficult to draw the boundaries to retain both model realism and model parsimony. This also applies to the time horizons chosen for the model analysis, as interactions are seldom lacking in future strategic consequences.
• *Unaccounted for behavioral and organizational factors.* By definition, such models are highly stylized views of reality, and they tend to emphasize quantifiable physical and financial variables over less quantifiable ones. However, it is possible to estimate the impact of such "soft factors" within the context of game theory models (Chapter 6 contained one such analysis).
• *Difficulty obtaining initial funding and managerial buy-in.* Unfamiliar and unproven decision science tools can be difficult to sell in environments of limited time and fiscal budgets. Practically, this means that pockets of acceptance should be nurtured diligently, as this may lead to a virtuous cycle of expanding managerial knowledge and acceptance of this method within an organization or industry.

7.9 Areas for Future Research

There are a number of areas for future research which stem from the models and analysis in this dissertation.

Model Refinement: Industry Participant "Reality Checking". One way to further refine these models is to have industry participants and analysts scrutinize the two core models developed here more deeply, validating the game structures and payoff estimates developed. Specifically, these content experts could help bolster and refine the assumptions made regarding semiconductor demand, supply, and cost estimates.

Model Refinement: More Sophisticated Uncertainty Analyses. As further model parameter refinements are incorporated from input by industry content experts, it would also become appropriate to incorporate more sophisticated uncertainty analyses within the models. For instance, content experts could be interviewed to provide their best guesses of probability

distributions for key input parameters, which could, in turn, be used to simulate a fully stochastic range of E(NPV) outcomes for each player.

Model Refinement: Risk-aversion and Behavioral Economics. One could also push further on the incorporation of risk-aversion and other behavioral economics refinements (in a manner similar to that demonstrated in Chapter 6). For instance, one could use the methods of experimental economics to try to measure the risk aversion (e.g., the Arrow-Pratt measure of risk aversion) of one or more players. Coupled with fully stochastic simulation modeling suggested above, one could refine the payoff estimates of the players accordingly. Such efforts would still be subject to the same caveats of such payoff refinements described in Section 6.9.

Alternative Formulations for > 3 Players. One could pursue the alternative formulations which have been suggested (in Chapter 5 and Figure 42) for modeling strategic interaction among more than three players. Such efforts might involve models similar to the existing non-cooperative models which become tractable by assuming greater symmetry among the players than was assumed in the models in this dissertation. However, they could also involve use a fundamentally different type of model such as weakest link or cooperative game theory models. One advantage of cooperative game theory models is that they could plausibly extend the analysis to more than two tiers of the supply chain. The electronics OEMs (e.g., Apple, Samsung, HP, etc.) could be modeled in such a three-tiered scenario.

Replicate in Other Industries. One could bolster the generalizability of the methodological conclusions presented here by applying this analysis approach to technology transitions in other industries besides the semiconductor industry. This analysis could be of ongoing transitions (as was the case in this dissertation) or in appropriate historical contexts (e.g., see the historical

technology transition examples given in Chapter 1 from the aerospace and automotive industries).

Public Policy Implications. Throughout this dissertation the primary focus has been on individual firm strategy. However, there are clearly a number of profound policy issues which could also be addressed with models such as those presented here. One such effort already exists regarding environmental policy questions in the aerospace industry (see Morrison et al. 2012). One straightforward application stemming from this dissertation is that one could apply such models to inter-governmental alignment and collaboration within large, monolithic public-private R&D arrangements in the semiconductor industry (see Linden et al. 2000, for evidence of the importance of inter-governmental alignment on early EUVL research funding).

7.10 Dissertation Wrap-up

This research was conducted very much in the spirit of maintaining a simultaneous focus on the contextual realism of real-world problems (two technology transitions in semiconductor manufacturing) and on theoretical frameworks for understanding strategic interaction (non-cooperative game theory). This dual focus engendered a creative tension which allowed building a bridge where a gap previously existed. The research was conducted in the "go to the gemba" spirit which guided much of the work of the Alfred P. Sloan Foundation's Industry Studies Program and its descendent, the Industry Studies Association (ISA).

One observation is that parsimonious game theoretic models seem to be most fruitful when technology transitions reach a certain stage of maturity where the technological outlines of the transition become relatively clear to virtually all players involved. This "state of modeling grace" allows a small set of key players and their actions to be well defined; it also strengthens

the assumptions of common knowledge necessary for the models developed in this dissertation. In such well-defined situations, the type of analysis in this dissertation can be quite powerful. It is clear there is considerable managerial art involved with recognizing these opportunities, developing the associated models, interpreting their results, and executing an R&D investment strategy accordingly.

One theme which has emerged from this dissertation is the dual purposes of parsimonious game theory models for strategy: prediction and learning. We have seen confirmation that parsimonious game theory models for business strategy can be somewhat predictive (e.g., Section 4.8). These game theory models also allow decision makers to explore the relevant strategic possibility space in a dramatically more cognitively compact manner than many other tools allow. We have seen that the models can yield useful strategic insight even when the predictions of the model cannot be precisely pinned down (e.g., Sections 5.4.2 and 5.4.3).

I will end with Robert Noyce's timeless and inspiring quote: "Be unencumbered by history. Go off and do something wonderful." For me this applies not only to the creation of the new and amazing technologies which humans have been able to develop (and are yet going to develop), but also to the creation of new mental models they employ to facilitate the effective collaboration and competition which are necessary preconditions for those technological creations. Viewed in this light, my dissertation is simply the start of an exciting journey out into the vast unknown.

Appendix A: EUVL Model Payoff Calculation Details

Chapter 4 includes discussion regarding the following aspects of the EUVL R&D model: conceptual game-theoretic framework, essential assumptions, values of payoffs estimates, and sensitivity analyses to changes in model input parameters. This appendix (Appendix A) is meant to provide a much more comprehensive explanation of how the Chipmaker EUV Backers and photolithography equipment supplier payoff estimates are derived. It also provides full traceability for the equipment supplier payoff estimates in Figure 11 through Figure *15* for those who are interested. This appendix follows a logical sequence of steps to achieve this aim.

First, a complete list of EUVL model acronyms, variables, and parameters used in the payoff calculations is provided for ease of cross-reference (Table 38 and Table 39). Second, complete expressions of the game-theoretic objective functions (a.k.a., payoff functions) and optimization formulations of the Chipmaker EUV Backers and equipment suppliers are provided and discussed (Section A.2). Third, a full set of algebraic equations is given which links the model parameters to the ultimate payoff estimates (Section A.3). Fourth, all EUVL model input parameter estimates are tabulated, with data source attribution and the author's reasoning about the estimates (Table 40). Finally, an example calculation is performed (Section A.5) to provide the full traceability to the equipment supplier payoff estimates shown in Figure 11 through Figure *15*.

Table 38: Table of Model Terms, Acronyms, and Symbols for EUVL Model (Chapter 4)

Terms/Acronyms/Symbols	Meaning
193i	"193-immersion", a sub-category of Deep Ultraviolet (DUV) photolithography using 193nm light and optical system immersed in water (a high index of refraction liquid)
A	ASML (larger photolithography equipment supplier)
C	"Chipmaker EUV Backers", sometimes referred to as Chipmakers for brevity
CAGR	Compound Annual Growth Rate
critical patterning	Photolithographic patterning of those semiconductor processing layers with such small features that they require either EUVL or the especially intensive use of current optical lithography, the so-called "double or multiple 193i patterning" (DP/MP 193i)
DP/MP (or DP/MP 193i)	Generic term for Double Patterning/Multiple Patterning using 193i optical photolithography
E_0	Expectation operator given information at time 0
EUV	Extreme Ultraviolet (or sometimes Extreme Ultraviolet Lithography)
EUVL	Extreme Ultraviolet Lithography
HVM	High Volume Manufacturing
leading edge wafers	Those wafers which require critical patterning
MSNE	Mixed Strategy Nash Equilibrium
N	Nikon (smaller photolithography equipment supplier)
NE	Nash Equilibrium
NGL	Next Generation Lithography
PSNE	Pure Strategy Nash Equilibrium
SPNE	Sub-game Perfect Nash Equilibrium
wafer start	A unit of silicon physical production (or capacity) representing the initial start of wafer fabrication of one silicon wafer
WSPW	Wafer Starts Per Week (measure of actual production or capacity at a silicon manufacturer)
WSPY	Wafer Starts Per Year (measure of actual production or capacity at a silicon manufacturer)

*A.1 Complete Reference List of EUVL Model Input Parameters, Decision Variables, and Other "Intermediate" Model Variables**

*Note: Table 39 below is meant to contain a comprehensive list (for ease of reference) of: model input parameters, decision variables, "intermediate" payoff variables, and other miscellaneous model inputs. The (direct) model input parameter (base case) estimates can be found in Table 40. A fuller description of the decision variables can be found in Section A.2. The equations which link "intermediate variables" with the model input parameters to calculate sub-components of the player payoff estimates are given in Section A.3 below.

Table 39: Input Model Parameters, Intermediate, and Payoff Variables for EUVL Model (Chapter 4)

Variable(s)/Parameter(s)	Description	Type
δ	Discount factor (annual). $\delta = 1/(1+r)$, where r is the annual discount rate assumed.	parameter
$\pi_{c,t}$	Untransformed (i.e., un-zero adjusted) E(NPV) payoff function for Chipmaker EUV Backers	intermediate
$\pi'_{c,t}$	Transformed (i.e., zero adjusted) E(NPV) payoff function for Chipmaker EUV Backers. These are the Chipmaker payoffs which show up in Figures 12 and 13.	payoff var.
$\pi_{i,t}$	Comprehensive E(NPV) payoff function for equipment supplier i in year t	payoff var.
$\pi_{i,t,\ DP/MP}$	Margin E(NPV) dollars for supplier i in year t from DP/MP equipment stream	intermediate
$\pi_{i,t,\ EUV}$	Margin E(NPV) dollars for supplier i in year t from EUV equipment stream	intermediate
$c_{0,\ EUV}$	Average cost of patterning a critical layer(across all leading edge product categories) at year 0 (2011).	parameter
$C_{c,t}$	Other costs (i.e., All costs which are not patterning or EUVL R&D financing related) collectively incurred by Chipmakers in Year t (excluding direct investments)	parameter
c_t	Average cost for patterning one critical layer in year t (given the actual mix of EUV and DP/MP processing utilized in the industry)	intermediate
$c_{t,\ DP/MP}$	Average cost for patterning one critical layer in year t via DP/MP 193i	intermediate
$c_{t,\ EUV}$	Average cost for patterning one critical layer in year t via EUV lithography	intermediate
$f_{chipmaker\ profit}$	Fraction of chipmaker manufacturing cost savings (from EUVL) which are converted to net Chipmaker profits	parameter
$f_{financing}$	Fraction of remaining required financing which "Chipmaker EUV Backers" must provide to ASML and/or Nikon in order to significantly accelerate their EUVL development efforts	parameter
$f_{leading\ edge}$	Fraction of wafer starts which are "Leading Edge"	parameter

Variable(s)/Parameter(s)	Description	Type
$f_{sr,\ DP/MP}$ (sr = supplier revenue)	Fraction of overall DP/MP patterning cost which corresponds to equipment and services purchases from the lithography suppliers	parameter
$f_{sr,\ EUV}$ (sr = supplier revenue)	Fraction of overall EUVL patterning cost which corresponds to equipment and services purchases from the lithography suppliers	parameter
$g_{cost\ ratio}$	Annual growth rate of *ratio* of EUVL patterning costs to DP/MP patterning (from 2011-2021)	parameter
$g_{critical\ layers}$	Annual growth rate of critical layers/wafer	parameter
$g_{EUV\ cost}$	Annual rate of overall EUV patterning cost/layer increase	parameter
g_{wafer}	Annual growth rate in demand for 300mm wafer starts	parameter
$g_{wafer,\ no\ EUV}$	Annual growth rate in demand for 300mm wafer starts (starting in 2016 if no EUVL is developed)	parameter
i	Arbitrary equipment supplier (i.e., either ASML or Nikon)	miscellaneous
$I_{c,0}$	Nonrecurring EUVL investment by Chipmakers in Year 0	intermediate
$I_{i,0}$	Nonrecurring EUVL investment by Supplier i in Year 0	intermediate
$I_{TOTAL,\ ASML}$	Additional non-recurring engineering (i.e., R&D) costs remaining for ASML's EUVL project completion (in October 2011)	parameter
$I_{TOTAL,\ Nikon}$	Additional non-recurring engineering (i.e., R&D) costs remaining for Nikon's EUVL project completion (in October 2011)	parameter
$\ell_{i,t,DP/MP}$	Number of critical layers to be patterned by supplier I in year t via DP/MP 193i lithography	intermediate
$\ell_{i,t,EUV}$	Number of critical layers to be patterned by supplier I in year t via EUV lithography	intermediate
ℓ_t	Number of critical layers to be patterned in	intermediate

Variable(s)/Parameter(s)	Description	Type
	year t	
$m_{net, DP/MP}$	Average net profit margin from DP/MP revenue of the equipment suppliers	parameter
$m_{net, EUV}$	Average net profit margin from EUV revenue of the equipment suppliers	parameter
$MS_{ASML, t, DP/MP}(s_C, s_{ASML}, s_{Nikon})$	Market share of total critical patterning: ASML employing DP/MP 193i lithography (see Table 41 through Table 45 for lists of values)	parameter
$MS_{ASML, t, EUV}(s_C, s_{ASML}, s_{Nikon})$	Market share of total critical patterning: ASML employing EUV lithography (see Table 41 through Table 45 for lists of values)	parameter
$MS_{Nikon, t, DP/MP}(s_C, s_{ASML}, s_{Nikon})$	Market share of total critical patterning: Nikon employing DP/MP 193i lithography (see Table 41 through Table 45 for lists of values)	parameter
$MS_{Nikon, t, EUV}(s_C, s_{ASML}, s_{Nikon})$	Market share of total critical patterning: Nikon employing EUV lithography (see Table 41 through Table 45 for lists of values)	parameter
n_{2011}	Average number of critical layers (across *all* leading edge products) in 2011	parameter
$N_{2011}, \ldots, N_{2021}$ *(Solely nomenclature, does not enter calculations in a direct manner)*	Expected nominal semiconductor processing node (e.g., 22nm) in year t	parameter
r_{2011}	Ratio of EUVL patterning costs to DP/MP patterning in 2011	parameter
$r_{supplier pricing, t}$	Tool pricing multiplier applied if either supplier drops out of critical patterning entirely in year t	parameter
$R_{c,t}$	Chipmaker revenue in year t	parameter
$R_{i,t, DP/MP}$	Equipment supplier i revenue in year t from the 193i DP/MP stream of equipment and services	intermediate
$R_{i,t, EUV}$	Equipment supplier i revenue in year t from the EUVL stream of equipment and services	intermediate

Variable(s)/Parameter(s)	Description	Type
s_A	Decision variable for ASML. Sometimes referred to as s_{ASML} for clarity.	decision var.
S_A	Strategy set for ASML	(related to) decision var.
s_C	Decision variable for "Chipmaker EUV Backers".	decision var.
S_C	Strategy set for "Chipmaker EUV Backers"	(related to) decision var.
s_N	Decision variable for Nikon. Sometimes referred to as s_{Nikon} for clarity.	decision var.
S_N	Strategy set for Nikon	(related to) decision var.
s_x^*	Optimal strategy for player X	decision var.
t	Calendar Year: t=0 corresponds to 2011 and t=10 corresponds to 2021	miscellaneous
$W_{0,\text{ total}}$	Total 300mm-equivalent WSPY Demand in year 0 (i.e., 2011)	parameter
$W_{t,\text{ leading edge}}$	"Leading Edge" 300mm-equivalent WSPY Demand in year t	intermediate

A.2 Players' Objective Functions and Optimization Formulations (2-stage EUVL game)

A.2.1 Players' Strategy Sets

To formally represent the EUVL R&D game the strategies of each player are defined as: s_C = strategy of the Chipmaker EUV Backers, s_A = strategy of ASML, s_N = strategy of Nikon. Note per Figure 9 and the surrounding discussions in Chapter 4, the strategy sets of each player for the two-stage game (in which the Chipmakers move in Stage 1, and the two suppliers move simultaneously in Stage 2) should be defined as:

$$S_c = \{\text{'No Financing', 'Finance ASML', 'Finance Nikon', 'Finance Both'}\} \quad (A.1)$$

and

$$S_A = S_N = \{\text{IIII, IIID, IIDI, IIDD, IDII, IDID, IDDI, IDDD, DIII, DIID, DIDI, DIDD, DDII, DDID, DDDI, DDDD}\} \quad \text{(A.2)}$$

where I stands for 'Invest' and D stands for 'Don't Invest', and the sequence of the four parts of the strategy is respectively responses to the following actions by the Chipmakers: (1) 'No financing', (2) 'Finance ASML', (3) 'Finance Nikon', and (4) 'Finance both'.

A.2.2 Chipmaker EUVL Backers' Objective Function

Given the strategy sets defined above and the sub-components of profit considered (see Section 4.2) we can define the payoffs for the chipmakers to be:

$$\pi_{c,0}(s_c, s_A, s_N) = E_0\left[\sum_{t=1}^{10} \delta^t\left(R_{c,t} - \ell_t c_t(s_c, s_A, s_N) - C_{c,t}\right)\right] - I_{c,0}(s_c) \quad \text{(A.3)}$$

The expectation operator is included here for completeness, although it is unnecessary for calculating the payoffs in Figure 11 through Figure 15, given that all the Chipmaker input parameter estimates are deterministic (see Table 40). For simplicity (and ease of interpretations of the results), a "zero point" of profit (i.e., payoff) for the Chipmakers was defined (separately for each of the five scenarios defined in Table 3) as the "status quo" outcome where each of the three players invests nothing (additional) in EUVL. This implies that the smallest Chipmaker payoff in each of the five scenarios defined in Chapter 4 become -$3B (corresponding to the outcome where Chipmakers invest $3B in total in ASML and Nikon, yet where neither supplier invests in EUVL. Because of the high benefits (to Chipmakers) of EUVL, the zero-point transformation also implies that all outcomes where one or both suppliers invest in EUVL yield significantly positive outcomes for the Chipmakers. This zero point transformation makes sense because it allows the $Rc_{,t}$'s and $C_{c,t}$'s to be considered constants (which were all arbitrarily set to

zero) and thus immaterial to the ultimately calculated "transformed" Chipmaker payoff estimates. (As stated in Chapter 4, there was no explicit attempt to characterize fully how the Chipmakers *revenues* would be impacted by any of the player's decisions regarding EUVL investment or success. Of course, if reasonable estimates of such effects are available, they can be readily incorporated into the Chipmakers' payoff estimates.)

The zero-point transformation for each scenario was performed by applying Equation (A.4) below to every Chipmaker payoff. This is a positive affine transformation, and hence it will not alter any of the pure strategy NE these games. The transformed Chipmakers' payoffs (designated by primes) in *each* scenario become:

$$\pi'_{c,0}(s_c, s_A, s_N) = \pi_{c,0}(s_c, s_A, s_N) - \pi_{c,0}(\text{'No financing', 'Don't Invest', 'Don't Invest'}) \quad \text{(A.4)}$$

To recapitulate, this last term is simply a constant which gets subtracted off of each untransformed payoff, to make the resultant payoff numbers more intuitively interpretable by those employing the model.

A.2.3 Equipment Suppliers' Objective Functions

$$\pi_{i,0}(s_c, s_i, s_{-i}) = E_0\left[\sum_{t=1}^{10} \delta^t\left(\pi_{i,t,DP/MP} + \pi_{i,t,EUV}\right)\right] - I_{i,0}(s_c, s_i) = E_0\left[\sum_{t=1}^{10} \delta^t\left(m_{net,DP/MP} R_{i,t,DP/MP} + m_{net,EUV} R_{i,t,EUV}\right)\right] - I_{i,0}(s_c, s_i) \quad \text{(A.5)}$$

Where, the revenue of equipment supplier i in year t flowing from DP/MP equipment, $R_{i,t,DP/MP}$ is given by:

$$R_{i,t,DP/MP} = f_{sr,DP/MP}\ell_{i,t,DP/MP}(s_c, s_i, s_{-i})c_{t,DP/MP} \quad \text{(A.6)}$$

Similarly, the revenue of equipment supplier i in year t flowing from EUV equipment (excluding R&D expenses modeled directly in the EUVL model), $R_{i,t,EUV}$ is given by:

$$R_{i,t,EUV} = f_{sr,EUV}\ell_{i,t,EUV}(s_c, s_i, s_{-i})c_{t,EUV} \quad \text{(A.7)}$$

Because the estimates of the equipment suppliers' payoffs are actually full estimates of the equipment suppliers' profits and thus are more evenly balanced between costs and benefits for the suppliers, it was deemed that a zero-point payoff transformation (as included in the Chipmaker's payoff calculations) was unnecessary.

A.2.4 Optimization Formulations for Chipmakers and Equipment Suppliers

Given the objective functions defined above, the optimization formulations for each player are as follows. After observing the Chipmakers' action s_c, supplier i solves:

$$s_i^*(s_c, s_{-i}) = \max_{s_i \epsilon S_i} \pi_{i,0}(s_c, s_i, s_{-i}^*(s_i)) \quad \text{(A.8)}$$

Knowing the equipment suppliers optimize this way, the Chipmakers optimize via backward induction by selecting the s_c corresponding to maximum Chipmakers payoff given the expected NE of the four proper sub-games of the overall EUVL game in which both i and –i act simultaneously in Stage 2 of the game:

$$s_c^* = \max_{s_c \epsilon S_c} \pi_{c,0}(s_c, s_i^*(s_c, s_{-i}^*), s_{-i}^*(s_c, s_i^*)) \quad \text{(A.9)}$$

Now that we have defined, at a high level, the optimization approaches of each player, let us proceed to define the set of more detailed equations which link the EUVL variables and parameters to the ultimate payoff calculations.

A.3 Intermediate Payoff Calculation Sub-Equations or "Linking Equations"

Calculation of Chipmakers' Nonrecurring Investment Amounts (see Table 40 for data sources):

$$I_{c,0}(\text{'No financing'}) = 0 \tag{A.10}$$

$$I_{c,0}(\text{'Finance ASML only'}) = f_{financing} I_{total,ASML} = 0.5(\$2B) = \$1B \tag{A.11}$$

$$I_{c,0}(\text{'Finance Nikon only'}) = f_{financing} I_{total,Nikon} = 0.5(\$4B) = \$2B \tag{A.12}$$

$$\begin{aligned} I_{c,0}(\text{'Finance both'}) &= f_{financing}(I_{total,ASML} + I_{total,Nikon}) \\ &= 0.5(\$2B + \$4B) = \$3B \end{aligned} \tag{A.13}$$

Calculation of Suppliers' Nonrecurring Investment Amounts (see Table 3 for summary of these)*:

*Note: for both suppliers (i = {ASML, Nikon}) $I_{i,0}(\cdot,\cdot)$ is function of both s_c (the first argument of the function) and s_i (the second argument of the function), but is assumed *not* to be a function of s_{-i}.

$$I_{ASML,0}(\cdot, \text{'Don't Invest'}) = 0 \tag{A.14}$$

$$\begin{aligned} I_{ASML,0}(\text{'No financing'}, \text{'Invest'}) &= I_{ASML,0}(\text{'Finance Nikon only'}, \text{'Invest'}) \\ &= I_{total,ASML} = \$2B \end{aligned} \tag{A.15}$$

$$\begin{aligned} I_{ASML,0}(\text{'Finance ASML only'}, \text{'Invest'}) &= I_{ASML,0}(\text{'Finance both'}, \text{'Invest'}) \\ &= \left(1 - f_{financing}\right) I_{total,ASML} = (1 - 0.5)\$2B = \$1B \end{aligned} \tag{A.16}$$

$$I_{Nikon,0}(\cdot, \text{'Don't Invest'}) = 0 \tag{A.17}$$

$$I_{Nikon,0}(\text{'No financing'},\text{'Invest'}) = I_{Nikon,0}(\text{'Finance ASML only'},\text{'Invest'}) = I_{total,Nikon} = \$4B \quad \text{(A.18)}$$

$$I_{Nikon,0}(\text{'Finance Nikon only'},\text{'Invest'}) = I_{Nikon,0}(\text{'Finance both'},\text{'Invest'}) = \left(1 - f_{financing}\right)I_{total,Nikon} = (1 - 0.5)\$4B = \$2B \quad \text{(A.19)}$$

Supplier Competition and Annual Growth of EUV Patterning Costs:

$$c_{t,EUV} = r_{supplier\ pricing,t}\, c_{0,EUV}\left(1 + g_{EUV,cost}\right)^t \quad \text{(A.20)}$$

Ratio of DP/MP cost to EUV cost:

$$r_t = r_0(1 + g_{cost\ ratio})^t \quad \text{(A.21)}$$

193i DP/MP Patterning Costs:

$$c_{t,DP/MP} = r_t c_{t,EUV} \quad \text{(A.22)}$$

Annual Growth in Leading Edge Wafer Start Demand:

$$W_{t,leading\ edge} = f_{leading\ edge} W_{0,total}\left(1 + g_{wafer}\right)^t \quad \text{(A.23)}$$

Annual Growth in the Average Number of Critical Layers/Wafer:

$$n_t = n_0\left(1 + g_{critical\ layers}\right)^t \quad \text{(A.24)}$$

Number of Critical Layers to be Patterned in Year t:

$$\ell_t = W_t n_t \quad \text{(A.25)}$$

Number of Critical Layers to be Patterned by Supplier i in Year t via 193i DP/MP Lithography:**

$$\ell_{i,t,DP/MP}(s_c, s_{ASML}, s_{Nikon}) = MS_{i,t,DP/MP}(s_c, s_{ASML}, s_{Nikon})\ell_t \quad \text{(A.26)}$$

** Note: Complete listings of $MS_{i,t,DP/MP}$, the assumed annual critical patterning market shares for 193i DP/MP, for Scenarios #4.1 through #4.5 can be found in Table 41 through Table 45 below.

Number of Critical Layers to be Patterned by Supplier i in Year t via EUV Lithography*:**

$$\ell_{i,t,EUV}(s_c, s_{ASML}, s_{Nikon}) = MS_{i,t,EUV}(s_c, s_{ASML}, s_{Nikon})\ell_t \quad \text{(A.27)}$$

***Note: Complete listings of $MS_{i,t,EUV}$, the assumed annual critical patterning market shares for EUV, for Scenarios #4.1 through #4.5 can be found in Table 41 through Table 45 below.

A.4 EUVL Model Input Parameters and Data Sources

Table 40: Input Model Parameter Estimates for EUVL "Current Roadmap" and "Slower Roadmap" Model (i.e., Figure 11 through Figure 15 in Chapter 4)

Model Parameter Symbol	Model Parameter Name	Estimated Parameter Value	Source of Parameter Estimate
δ	Discount Factor (annual)	0.870 =1/(1+0.15)	EUV Lithography is riskier than typical R&D projects. Hence, the discount rate used should err toward the high end of typical discount rates. Hence, 15% was chosen from the typical 12%-15% range that many companies use.
$c_{0,\,EUV}$	Average Cost of Patterning a Critical Layer(across ALL leading edge products)	$66.9/layer = 46.44 euro/layer*1.44$/euro	46.44 euro/layers (from ASML 6/7/11, slide 22). 1.44 euro/dollar (average exchange rate from April 1, 2011 – August 31, 2011 retrieved from www.oanda.com).
$C_{c,t}$	Other costs (i.e., All costs which are not patterning or EUVL R&D financing related) collectively incurred by Chipmakers in Year t (excluding direct investments)	0 (All of these costs are assumed to be zero)	Because these other costs are assumed to be independent of the actions of the three game players, they can be considered constants. Because a "zero-point" of Chipmaker payoffs was assumed (see Section A.2.2), these constants are arbitrary (relative to the model payoffs). Hence, they were all set to zero.

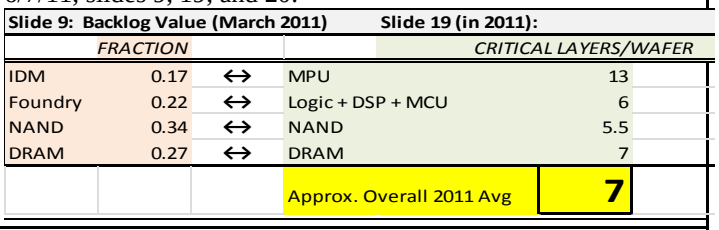
Model Parameter Symbol	Model Parameter Name	Estimated Parameter Value	Source of Parameter Estimate
$C_{i,t}$	Other costs (i.e., all costs which are not patterning or EUVL R&D financing related) incurred by equipment supplier i in year t	0 (All of these costs are assumed to be zero)	As implied in Section A.2.3, those equipment supplier costs which were not directly related to the patterning via EUVL or DP/MP were assumed to be zero.
$f_{\text{chipmaker profit}}$	Fraction of chipmaker manufacturing cost savings (from the introduction of EUVL) which are converted to net Chipmaker profits	50%	Best estimate of author. Clearly, it is reasonable to assume that not all manufacturing cost reductions will go directly to profit for the chipmakers. Various factors including inter-chipmaker competition and taxes will shave away at how 450mm manufacturing cost savings ultimately impact chipmaker profitability. Lacking precise estimates, but knowing that these factors are substantial, I used an estimate of 50%.
$f_{\text{financing}}$	Fraction of remaining required financing which "Chipmaker EUV Backers" must provide to ASML and/or Nikon to significantly accelerate their EUVL development efforts	50%	Best estimate of author. Obviously, the equipment suppliers will continue to bear a significant burden of EUVL R&D costs. However, as many industry commentators have observed, there is expected to be a sharing of R&D costs between equipment suppliers and chipmakers for large technology transitions going forward – for example 450mm wafers and EUVL. (See McGrath 7/11/12 and Lapedus 10/25/10 for expressions of this viewpoint). Previous estimates of chipmaker financing aid to suppliers has typically been less than 50% of the R&D total, but EUV is widely regarded to be significantly more challenging and expensive than prior technology transitions (e.g., see Lin 2006). Hence a larger fraction (50%) of the remaining R&D expenditures was assumed.
$f_{\text{leading edge}}$	Fraction of wafer starts which are "Leading Edge"	50%	Best estimate of author. Many worldwide silicon wafer starts have historically been "trailing edge". In fact, a rough analysis of the "World Fab Forecast" data (produced by the Semiconductor Equipment and Material International) indicates the fraction of leading edge wafers (defined as most recent three technology nodes) is approximately 20% of the total 200mm-equivalent wafer starts. As Moore's Law progresses the fraction of wafers needing EUV and/or DP/MP will increase significantly. I estimated the long-run average of this fraction to be approximately 50%.

Model Parameter Symbol	Model Parameter Name	Estimated Parameter Value	Source of Parameter Estimate
$f_{sr,\ DP/MP}$ (sr = supplier revenue)	Fraction of overall DP/MP patterning cost which corresponds to equipment and services purchases from the lithography suppliers	33%	33% fraction found in ASML 6/7/11, slide 22.
$f_{sr,\ EUV}$ (sr = supplier revenue)	Fraction of overall EUVL patterning cost which corresponds to equipment and services purchases from the lithography suppliers	68%	68% fraction found in ASML 6/7/11, slide 22.
$g_{cost\ ratio}$	Annual growth rate of *ratio* of DP/MP patterning costs to EUV patterning (from 2011-2021)	10%	Best estimate of author, based on the following logic: As time progresses it is clear that double/multiple patterning with immersion lithography will become significantly more expensive than EUV. For example, it is expected that as Moore's Law continues, multiple patterning would require quintuple patterning instead of double patterning roughly increasing the number of lithography and supporting steps by a factor of 5/2 =2.5. There are many uncertainties which make the multiple patterning solution likely to become more difficult over time; hence, it was decided to round up from 1.53*(5/2) = 3.83 to an end cost multiplier of (very) roughly 4.00. This is corresponds to a CAGR of approximately 10%.
$g_{critical\ layers}$	Annual growth rate of average number of critical layers/wafer	12%	Best estimate of author. The number of "critical layers" per wafer is growing at a rapid rate, but there are fundamental limits on how many critical layers can (economically) be patterned on a given wafer (due to defect issues, layer-to-layer overlay, etc.) In the ASML reference in the table row above (still slides 19 and 20), the growth rates of number of critical layers (from 2012 over 2011) for the four product categories range from 12.7% to 33.3% annually. Assuming a significant slowdown overall must occur (say, conservatively a 12% annual rate overall for all product categories), approximately three times number of critical layers per wafer (21=7*3) will be attained in ten years (i.e., in 2021).
$g_{EUV\ cost}$	Annual rate of overall EUV patterning cost/layer increase	5%	Best estimate of author. There are two countervailing forces at work: 1) EUV will become more difficult technologically as feature sizes continue to shrink (and hence more expensive per layer) over time and 2) The industry will move up the learning curve and hence be able to reduce EUV lithography costs (per layer). Based on a judgment regarding which force will be stronger, a moderate increase was assumed of 5% in EUV costs

Model Parameter Symbol	Model Parameter Name	Estimated Parameter Value	Source of Parameter Estimate
			each year.
g_{wafer}	Annual growth rate in demand for 300mm wafer starts	10%	A 10% annual growth in future wafer demand was recently forecast by Semico Research Corp (see Itow 9/20/12). This is roughly consistent with an 11% growth rate which the author also found using data from "World Fab Forecast" data from SEMI for the periods 1998-2000 and 2004-2006.
$g_{wafer, no EUV}$	Annual growth rate in demand for 300mm wafer starts (starting in 2016 if no EUVL is developed)	0%	Best estimate of author. If EUVL is not ultimately developed, there will almost certainly be a slowdown in the growth of demand for semiconductors (due to the increasing costs of manufacturing chips in this case). If EUVL is not eventually developed this reduction could be quite considerable. Hence an annual growth rate of 0% was assumed after 2016 if no EUVL is eventually developed (vs. the assumption of 10% annual growth if EUVL is successfully developed).
$I_{TOTAL, ASML}$	Additional non-recurring engineering (i.e., R&D) costs remaining for ASML's EUVL project completion (in October 2011)	$2B	First of all, given the technological complexity and the numerous schedule slips, all that can be ascertained is a rough estimate for this number (sensitivity analysis is performed on this parameter in Section 4.10). The cumulative magnitude of investment made by ASML into EUV technology (by the time of its HVM insertion has been estimated at 2B€ (by certain equity research analysts). At an exchange rate of about 1.45$/€, this represents a cumulative investment of approx. $2.9B. Some of this investment had been spent already, but this number does not include additional investments in supporting "ecosystem" technologies needed from other companies which the industry would also need to support to derive any benefit. Hence, combining all these factors, a rough estimate of $2B additional needed was decided upon.
$I_{TOTAL, Nikon}$	Additional non-recurring engineering (i.e., R&D) costs remaining for Nikon's EUVL project completion (in October 2011)	$4B	Best estimate of author. There are two countervailing forces at play here. One is the fact that Nikon had invested much less than ASML had at the point of the analysis (Oct. 2011). The other is that being a later entrant in a technologically uncertain environment does confer some learning benefits to the late entering firm. For example, there were two possible light source concepts (a critical and difficult component of the overall EUVL system) which were being tested out. The late entering firm would be able to observe which technology succeeded and not waste development dollars on the (presumably) less promising technology which did not win the race between the two technologies conducted by the first firm. Ultimately, a conservative estimate on the high end of expectations was chosen for the later entering lithography supplier (i.e., Nikon).
$m_{net, DP/MP}$	Average net margin of lithography equipment suppliers	15%	The average net margin for ASML from 2008 through 2012 is 14.9% per ASML's 2012 Annual Report (ASML 2012). This net margin was rounded to 15% as a long-run estimate of the profitability for DP/MP technology. Nikon's profitability on DP/MP 193i technology is harder to get from financial

Model Parameter Symbol	Model Parameter Name	Estimated Parameter Value	Source of Parameter Estimate
	on DP/MP products and services		statements because it has significant non-lithography businesses as well (while ASML is much closer to a "pure play" lithography company)
$m_{net, EUV}$	Average net margin of lithography equipment suppliers on EUVL products and services	20%	Because EUV Lithography is expected to be more cost effective for chipmakers, one can expect that equipment suppliers would achieve a significantly higher profit margin for it when it becomes available. As a long-run estimate I assumed this represents a 5% increase in net margin over the DP/MP 193i lithography solutions. This implies an estimate of 20% net margin.
$MS_{ASML, t, DP/MP}(s_C, s_{ASML}, s_{Nikon})$; $MS_{ASML, t, EUV}(s_C, s_{ASML}, s_{Nikon})$; $MS_{Nikon, t, DP/MP}(s_C, s_{ASML}, s_{Nikon})$; $MS_{Nikon, t, EUV}(s_C, s_{ASML}, s_{Nikon})$	Market share of critical patterning for both EUV and DP/MP for both ASML and Nikon (by year)	See full list of market share ramp rates in Table 41 through Table 45 below (Note that the author derived these ramp rates using his best judgment, subject to the "constraints/conditions" shown in the next several rows)	The precise profiles of ramp rates of EUV technology were ultimately the judgment of the author incorporating expected effects of: financing by the chipmakers, the inherent difficulty of bringing the EUVL HVM equipment to the market, and the expected competition between ASML and Nikon (for both 193i and EUV tools). However, a few significant features of the ramp rates were determined and applied to the predicted ramp rates under various future states of the world. Specifically, an industry analyst (see EE Times 6/23/10) states that ASML plans to ramp from preproduction tools (2010) to 13 EUV systems/year shipped two years later (in 2012). The total number of 193i lithography systems shipped per year is on the order of 100 systems/year. (This is an estimate by certain equity research analysts.) Even though there will likely be fewer EUV systems shipped per year than 193i systems, 13 EUV systems still represents a significant minority of the total available market. Hence, for Scenario #4.1 in the EUVL model (Figure 12), a period of **three years** was assumed from pre-production tools to a ≥50% critical layer penetration of EUV technology. In the more realistic/pessimistic outlooks (Scenarios #4.2-#4.4) for EUVL technology development/adoption a period of **four years** was the ramp length assumed from pre-production tools to achieve ≥50% of the ultimate EUV adoption fraction (capped at 60% of the patterning of the overall critical layer needs).
$M_{slower EUV}$ (for reference only – impact of this "parameter" is fully captured by $MS_{i,t,X}$ market share ramp rates in Table 42 through Table 45)	EUV "critical patterning" MS cap for critical patterning assumed in Scenarios #4.2 through #4.5 (Figure 12 through Figure ***15***)	60%	If there is a slower adoption of EUVL, presumably it would be because of technological difficulties. The currently agreed largest technological stumbling block to EUVL is the throughput of EUVL light sources (e.g., see Bakshi 3/7/11). This sort of throughput constraint implies that there may be certain chip markets where EUV is cost-effective and others where it is not. Giving a slight advantage to EUV technology one arrives at a reasonable guess of 60% as a cap on the EUV critical patterning MS in the event of a longstanding technological impediment to it.

Model Parameter Symbol	Model Parameter Name	Estimated Parameter Value	Source of Parameter Estimate
$M_{EUV, Nikon survivability}$ (for reference only – impact of this "parameter" is fully captured by $MS_{i,t,X}$ market share ramp rates in Table 41)	Percentage of "Critical Patterning" MS supplied by ASML **EUV** beyond which Nikon drops out of critical layer equipment production entirely	70%	Best estimate of author. It is widely reported that Nikon's largest customer (by far) is Intel (e.g., see Lapedus 4/2/12). This fact strongly suggests that Nikon's "commercial fragility" could hinge on the purchasing decisions of one or more large chipmakers. EUV (if/when it gets developed) will put considerable pressure on 193i sales. Hence, 70% of critical layer tool purchases for ASML's EUV effort would put significant strain on Nikon's 193i equipment offerings.
$\Delta t_{financing}$ (for reference only – impact of this "parameter" is fully captured by $MS_{i,t,X}$ market share ramp rates in Table 41 through Table 45)	EUVL HVM insertion date PULL-IN given chipmakers "Finance" a given supplier	1 year	Best estimate of author. Progress is hard won on EUVL technology because of its technological complexity. Hence, even with significantly larger budgets (enabled by co-financing by chipmakers), there would not be a dramatic pull-in of EUV introduction year. A one-year pull-in is consistent with the kinds of progress reported for this technology.
$t_{ASML, no financing}$ (for reference only – impact of this "parameter" is fully captured by $MS_{i,t,X}$ market share ramp rates in Table 41 through Table 45)	HVM EUVL insertion date for ASML (with no chipmaker financing)	2013	As of the time of the EUVL model development (October 2011), opinions varied regarding ASML's likely introduction year for HVM EUV, but 2013 was a common estimate (e.g., see Clarke 7/11/11).
$t_{ASML leads Nikon}$	Number of years R&D lead	3 years (=2016-2013)	Consider the quote: "ASML is pushing hard to bring EUV to the 22-nm node, but Nikon believes that the technology will not be

Model Parameter Symbol	Model Parameter Name	Estimated Parameter Value	Source of Parameter Estimate
(for reference only – impact of this "parameter" is fully captured by $MS_{i,t,X}$ market share ramp rates in Table 41 through Table 45)	in EUVL technology which ASML has over Nikon		ready until the 16- or 11-nm node.". (from Lapedus 2/28/11) Based on this, assuming that Nikon is shooting for EUV insertion one or two nodes behind ASML (assuming a continued 2-year inter-node cadence), we would expect that Nikon is perhaps 2 years to 4 years behind ASML. If they made the sizeable investment now in EUVL they would benefit from some learning as the second company to bring the technology to market. Hence, Nikon was assumed to be roughly 3 years behind ASML in EUV development.
n_{2011}	Average Number of Critical Layers (across ALL leading edge products) in 2011	7 critical layers/wafer in 2011	The calculations in the graphic below leading to the overall estimate of 7 critical layers/wafer were derived from ASML 6/7/11, slides 9, 19, and 20. 
N_{2011}, …, N_{2021} (These nodes are solely for nomenclature. They do not enter the payoff calculations in a direct manner.)	Expected semiconductor processing node in year t	22nm in 2012, 14nm in 2014, 10nm in 2016, 7nm in 2018, 5nm in 2020	There is no single agreed upon set of expected nodes for future silicon process technology. Additionally, these node dimensions are nominal and they will vary by chip category (Find the 2011 ITRS nodes by year and by product category at ITRS 2011). Simplified for nomenclatural convenience, one version of Intel's expected two-year "Tick Tock" cadence is used to designate the process technology nodes expected in each year (e.g. see Wikipedia "Intel Tick-Tock", 2/19/13; Tyson 5/15/12).
r_{2011}	Ratio of DP/MP patterning costs to EUVL patterning costs originally assumed for 2011	1.53	=(70.82 Euro/wafer)/(46.44 Euro/wafer)= 1.53. Derived from ASML 6/7/11, slide 22.
$r_{supplier\ pricing,\ t}$	Tool pricing multiplier	1.0 (if both suppliers have	Although the equipment pricing multiplier by a back-of-the-envelope gross margin calculations was determined to be

Model Parameter Symbol	Model Parameter Name	Estimated Parameter Value	Source of Parameter Estimate
	applied if either supplier drops out of critical patterning entirely in year t	positive market share in critical patterning in year t) 1.2 (if one supplier has 100% of the market share in critical patterning year t)	approximately 1.5 time more expensive for a single supplier situation vs. a two supplier situation, a more conservative multiplier of 1.2 was assumed, allowing for: switching to substitute technology (likely multiple patterning with 193i lithography) due to higher EUV costs, errors in the equipment supplier net profit margin calculation, and any EUVL pricing mitigation due to anti-trust concerns.
$R_{c,t}$	Chipmaker revenue in year t	0 (All of these annual revenues are assumed to be zero)	Because these other revenues are assumed to be independent of the actions of the three game players, they can be considered constants. Because a "zero-point" of Chipmaker payoffs was assumed (see Section A.2.2), these constants are arbitrary (relative to the model payoffs). Hence, they were all set to zero.
W_0	Annual 300mm-equivalent global wafer demand in 2011 (in WSPY)	41,700,000	The Semiconductor Industry Association Semiconductor Capacity Utilization (SICAS) Reports (http://www.sia-online.org/industry-statistics/semiconductor-capacity-utilization-sicas-reports/) indicate that wafer demand is ~2,000,000 total 200mm-equivalent WSPW in 2011 → ~100,000,000 total 200mm-equivalent WSPY in 2011 → ~ 41,700,000 total 300mm-equivalent WSPY in 2011 (i.e., a factor of 2.4 fewer of the larger wafers).

Table 41: Scenario #4.1 EUV and DP/MP Market Share Ramp Rates for Each Supplier as Function of Player Action (Corresponds to Figure 11 in Chapter 4)

Assumed actions of players	Modeling MS by year	Year (t)										
Chipmakers: No Financing		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-I, Nikon-I)	$MS_{ASML, t, DP/MP}$	80%	80%	70%	40%	20%	15%	10%	0%	0%	0%	0%
	$MS_{ASML, t, EUV}$	0%	0%	10%	40%	60%	60%	60%	70%	70%	70%	70%
	$MS_{Nikon, t, DP/MP}$	20%	20%	20%	20%	20%	15%	10%	0%	0%	0%	0%
	$MS_{Nikon, t, EUV}$	0%	0%	0%	0%	0%	10%	20%	30%	30%	30%	30%
Chipmakers: No Financing		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-I, Nikon-DI)	$MS_{ASML, t, DP/MP}$	80%	80%	70%	40%	20%	20%	20%	0%	0%	0%	0%
	$MS_{ASML, t, EUV}$	0%	0%	10%	40%	60%	80%	80%	100%	100%	100%	100%
	$MS_{Nikon, t, DP/MP}$	20%	20%	20%	20%	20%	0%	0%	0%	0%	0%	0%
	$MS_{Nikon, t, EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
Chipmakers: No Financing		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-DI, Nikon-I)	$MS_{ASML, t, DP/MP}$	80%	80%	70%	60%	50%	40%	25%	0%	0%	0%	0%
	$MS_{ASML, t, EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%

	$MS_{Nikon,\ t,\ DP/MP}$	20%	20%	30%	40%	50%	40%	25%	20%	0%	0%	0%
	$MS_{Nikon,\ t,\ EUV}$	0%	0%	0%	0%	0%	20%	50%	80%	100%	100%	100%
Chipmakers: No Financing		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-DI, Nikon-DI)	$MS_{ASML,\ t,\ DP/MP}$	80%	80%	80%	80%	80%	80%	80%	80%	80%	80%	80%
	$MS_{ASML,\ t,\ EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
	$MS_{Nikon,\ t,\ DP/MP}$	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
	$MS_{Nikon,\ t,\ EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
Chipmakers: Finance ASML Only		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-I, Nikon-I)	$MS_{ASML,\ t,\ DP/MP}$	80%	70%	40%	20%	20%	15%	10%	0%	0%	0%	0%
	$MS_{ASML,\ t,\ EUV}$	0%	10%	40%	60%	60%	60%	60%	70%	70%	70%	70%
	$MS_{Nikon,\ t,\ DP/MP}$	20%	20%	20%	20%	20%	15%	10%	0%	0%	0%	0%
	$MS_{Nikon,\ t,\ EUV}$	0%	0%	0%	0%	0%	10%	20%	30%	30%	30%	30%
Chipmakers: Finance ASML Only		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-I, Nikon-DI)	$MS_{ASML,\ t,\ DP/MP}$	80%	70%	40%	20%	20%	20%	20%	0%	0%	0%	0%
	$MS_{ASML,\ t,\ EUV}$	0%	10%	40%	60%	80%	80%	80%	100%	100%	100%	100%
	$MS_{Nikon,\ t,\ DP/MP}$	20%	20%	20%	20%	0%	0%	0%	0%	0%	0%	0%
	$MS_{Nikon,\ t,\ EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
Chipmakers: Finance ASML Only		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-DI, Nikon-I)	$MS_{ASML,\ t,\ DP/MP}$	80%	80%	70%	60%	50%	40%	25%	0%	0%	0%	0%
	$MS_{ASML,\ t,\ EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
	$MS_{Nikon,\ t,\ DP/MP}$	20%	20%	30%	40%	50%	40%	25%	20%	0%	0%	0%
	$MS_{Nikon,\ t,\ EUV}$	0%	0%	0%	0%	0%	20%	50%	80%	100%	100%	100%
Chipmakers: Finance ASML Only		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-DI, Nikon-DI)	$MS_{ASML,\ t,\ DP/MP}$	80%	80%	80%	80%	80%	80%	80%	80%	80%	80%	80%
	$MS_{ASML,\ t,\ EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
	$MS_{Nikon,\ t,\ DP/MP}$	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
	$MS_{Nikon,\ t,\ EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
Chipmakers: Finance Nikon Only		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-I, Nikon-I)	$MS_{ASML,\ t,\ DP/MP}$	80%	80%	70%	40%	20%	15%	10%	0%	0%	0%	0%
	$MS_{ASML,\ t,\ EUV}$	0%	0%	10%	40%	50%	50%	60%	70%	70%	70%	70%
	$MS_{Nikon,\ t,\ DP/MP}$	20%	20%	20%	20%	20%	15%	10%	0%	0%	0%	0%
	$MS_{Nikon,\ t,\ EUV}$	0%	0%	0%	0%	10%	20%	20%	30%	30%	30%	30%
Chipmakers: Finance Nikon		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**

Only												
(ASML-I, Nikon-DI)	$MS_{ASML, t, DP/MP}$	80%	80%	70%	40%	20%	20%	20%	0%	0%	0%	0%
	$MS_{ASML, t, EUV}$	0%	0%	10%	40%	60%	80%	80%	100%	100%	100%	100%
	$MS_{Nikon, t, DP/MP}$	20%	20%	20%	20%	20%	0%	0%	0%	0%	0%	0%
	$MS_{Nikon, t, EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
Chipmakers: Finance Nikon Only		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-DI, Nikon-I)	$MS_{ASML, t, DP/MP}$	80%	80%	70%	60%	40%	30%	15%	0%	0%	0%	0%
	$MS_{ASML, t, EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
	$MS_{Nikon, t, DP/MP}$	20%	20%	30%	40%	40%	30%	15%	0%	0%	0%	0%
	$MS_{Nikon, t, EUV}$	0%	0%	0%	0%	20%	40%	70%	100%	100%	100%	100%
Chipmakers: Finance Nikon Only		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-DI, Nikon-DI)	$MS_{ASML, t, DP/MP}$	80%	80%	80%	80%	80%	80%	80%	80%	80%	80%	80%
	$MS_{ASML, t, EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
	$MS_{Nikon, t, DP/MP}$	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
	$MS_{Nikon, t, EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
Chipmakers: Finance Both Suppliers		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-I, Nikon-I)	$MS_{ASML, t, DP/MP}$	80%	70%	40%	20%	15%	10%	5%	0%	0%	0%	0%
	$MS_{ASML, t, EUV}$	0%	10%	40%	60%	60%	60%	60%	70%	70%	70%	70%
	$MS_{Nikon, t, DP/MP}$	20%	20%	20%	20%	15%	10%	5%	0%	0%	0%	0%
	$MS_{Nikon, t, EUV}$	0%	0%	0%	0%	10%	20%	30%	30%	30%	30%	30%
Chipmakers: Finance Both Suppliers		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-I, Nikon-DI)	$MS_{ASML, t, DP/MP}$	80%	70%	40%	20%	20%	20%	20%	0%	0%	0%	0%
	$MS_{ASML, t, EUV}$	0%	10%	40%	60%	80%	80%	80%	100%	100%	100%	100%
	$MS_{Nikon, t, DP/MP}$	20%	20%	20%	20%	0%	0%	0%	0%	0%	0%	0%
	$MS_{Nikon, t, EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
Chipmakers: Finance Both Suppliers		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-DI, Nikon-I)	$MS_{ASML, t, DP/MP}$	80%	80%	70%	60%	40%	25%	15%	0%	0%	0%	0%
	$MS_{ASML, t, EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
	$MS_{Nikon, t, DP/MP}$	20%	20%	30%	40%	40%	25%	15%	0%	0%	0%	0%
	$MS_{Nikon, t, EUV}$	0%	0%	0%	0%	20%	50%	70%	100%	100%	100%	100%
Chipmakers: Finance Both Suppliers		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-DI, Nikon-DI)	$MS_{ASML, t, DP/MP}$	80%	80%	80%	80%	80%	80%	80%	80%	80%	80%	80%
	$MS_{ASML, t, EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%

	$MS_{Nikon,\ t,\ DP/MP}$	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
	$MS_{Nikon,\ t,\ EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%

Table 42: Scenario #4.2 EUV and DP/MP Market Share Ramp Rates for Each Supplier as Function of Player Action (Corresponds to Figure 12 in Chapter 4)

Assumed actions of players	**Modeling MS by year**	**Year (t)**										
Chipmakers: No Financing		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-I, Nikon-I)	$MS_{ASML,\ t,\ DP/MP}$	80%	80%	75%	70%	60%	45%	30%	20%	20%	20%	20%
	$MS_{ASML,\ t,\ EUV}$	0%	0%	5%	10%	20%	30%	40%	40%	40%	40%	40%
	$MS_{Nikon,\ t,\ DP/MP}$	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
	$MS_{Nikon,\ t,\ EUV}$	0%	0%	0%	0%	0%	5%	10%	20%	20%	20%	20%
Chipmakers: No Financing		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-I, Nikon-DI)	$MS_{ASML,\ t,\ DP/MP}$	80%	80%	75%	70%	60%	50%	35%	20%	20%	20%	20%
	$MS_{ASML,\ t,\ EUV}$	0%	0%	5%	10%	20%	30%	45%	60%	60%	60%	60%
	$MS_{Nikon,\ t,\ DP/MP}$	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
	$MS_{Nikon,\ t,\ EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
Chipmakers: No Financing		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-DI, Nikon-I)	$MS_{ASML,\ t,\ DP/MP}$	80%	80%	70%	60%	50%	45%	35%	20%	20%	20%	20%
	$MS_{ASML,\ t,\ EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
	$MS_{Nikon,\ t,\ DP/MP}$	20%	20%	30%	40%	50%	45%	35%	20%	20%	20%	20%
	$MS_{Nikon,\ t,\ EUV}$	0%	0%	0%	0%	0%	10%	30%	60%	60%	60%	60%
Chipmakers: No Financing		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-DI, Nikon-DI)	$MS_{ASML,\ t,\ DP/MP}$	80%	80%	80%	80%	80%	80%	80%	80%	80%	80%	80%
	$MS_{ASML,\ t,\ EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
	$MS_{Nikon,\ t,\ DP/MP}$	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
	$MS_{Nikon,\ t,\ EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
Chipmakers: Finance ASML Only		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-I, Nikon-I)	$MS_{ASML,\ t,\ DP/MP}$	80%	75%	70%	60%	50%	35%	20%	20%	20%	20%	20%
	$MS_{ASML,\ t,\ EUV}$	0%	5%	10%	20%	30%	40%	50%	40%	40%	40%	40%
	$MS_{Nikon,\ t,\ DP/MP}$	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
	$MS_{Nikon,\ t,\ EUV}$	0%	0%	0%	0%	0%	5%	10%	20%	20%	20%	20%
Chipmakers: Finance ASML Only		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-I, Nikon-DI)	$MS_{ASML,\ t,\ DP/MP}$	80%	75%	70%	60%	50%	40%	30%	20%	20%	20%	20%

	$MS_{ASML, t, EUV}$	0%	5%	10%	20%	30%	40%	50%	60%	60%	60%	60%
	$MS_{Nikon, t, DP/MP}$	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
	$MS_{Nikon, t, EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
Chipmakers: Finance ASML Only		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-DI, Nikon-I)	$MS_{ASML, t, DP/MP}$	80%	80%	80%	80%	80%	60%	40%	20%	20%	20%	20%
	$MS_{ASML, t, EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
	$MS_{Nikon, t, DP/MP}$	20%	20%	20%	20%	20%	30%	30%	20%	20%	20%	20%
	$MS_{Nikon, t, EUV}$	0%	0%	0%	0%	0%	10%	30%	60%	60%	60%	60%
Chipmakers: Finance ASML Only		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-DI, Nikon-DI)	$MS_{ASML, t, DP/MP}$	80%	80%	80%	80%	80%	80%	80%	80%	80%	80%	80%
	$MS_{ASML, t, EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
	$MS_{Nikon, t, DP/MP}$	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
	$MS_{Nikon, t, EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
Chipmakers: Finance Nikon Only		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-I, Nikon-I)	$MS_{ASML, t, DP/MP}$	80%	80%	75%	70%	55%	40%	20%	20%	20%	20%	20%
	$MS_{ASML, t, EUV}$	0%	0%	5%	10%	20%	30%	40%	40%	40%	40%	40%
	$MS_{Nikon, t, DP/MP}$	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
	$MS_{Nikon, t, EUV}$	0%	0%	0%	0%	5%	10%	20%	20%	20%	20%	20%
Chipmakers: Finance Nikon Only		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-I, Nikon-DI)	$MS_{ASML, t, DP/MP}$	80%	80%	75%	70%	60%	50%	35%	20%	20%	20%	20%
	$MS_{ASML, t, EUV}$	0%	0%	5%	10%	20%	30%	45%	60%	60%	60%	60%
	$MS_{Nikon, t, DP/MP}$	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
	$MS_{Nikon, t, EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
Chipmakers: Finance Nikon Only		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-DI, Nikon-I)	$MS_{ASML, t, DP/MP}$	80%	80%	70%	60%	45%	40%	40%	20%	20%	20%	20%
	$MS_{ASML, t, EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
	$MS_{Nikon, t, DP/MP}$	20%	20%	30%	40%	45%	40%	20%	20%	20%	20%	20%
	$MS_{Nikon, t, EUV}$	0%	0%	0%	0%	10%	20%	40%	60%	60%	60%	60%
Chipmakers: Finance Nikon Only		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-DI, Nikon-DI)	$MS_{ASML, t, DP/MP}$	80%	80%	80%	80%	80%	80%	80%	80%	80%	80%	80%
	$MS_{ASML, t, EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
	$MS_{Nikon, t, DP/MP}$	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
	$MS_{Nikon, t, EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%

Chipmakers: Finance Both Suppliers		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-I, Nikon-I)	$MS_{ASML,\ t,\ DP/MP}$	80%	75%	70%	60%	50%	30%	20%	20%	20%	20%	20%
	$MS_{ASML,\ t,\ EUV}$	0%	5%	10%	20%	30%	40%	45%	40%	40%	40%	40%
	$MS_{Nikon,\ t,\ DP/MP}$	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
	$MS_{Nikon,\ t,\ EUV}$	0%	0%	0%	0%	5%	10%	15%	20%	20%	20%	20%
Chipmakers: Finance Both Suppliers		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-I, Nikon-DI)	$MS_{ASML,\ t,\ DP/MP}$	80%	75%	70%	60%	50%	40%	30%	20%	20%	20%	20%
	$MS_{ASML,\ t,\ EUV}$	0%	5%	10%	20%	30%	40%	50%	60%	60%	60%	60%
	$MS_{Nikon,\ t,\ DP/MP}$	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
	$MS_{Nikon,\ t,\ EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
Chipmakers: Finance Both Suppliers		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-DI, Nikon-I)	$MS_{ASML,\ t,\ DP/MP}$	80%	80%	70%	60%	60%	50%	40%	20%	20%	20%	20%
	$MS_{ASML,\ t,\ EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
	$MS_{Nikon,\ t,\ DP/MP}$	20%	20%	30%	40%	30%	30%	20%	20%	20%	20%	20%
	$MS_{Nikon,\ t,\ EUV}$	0%	0%	0%	0%	10%	20%	40%	60%	60%	60%	60%
Chipmakers: Finance Both Suppliers		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-DI, Nikon-DI)	$MS_{ASML,\ t,\ DP/MP}$	80%	80%	80%	80%	80%	80%	80%	80%	80%	80%	80%
	$MS_{ASML,\ t,\ EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
	$MS_{Nikon,\ t,\ DP/MP}$	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
	$MS_{Nikon,\ t,\ EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%

Table 43: Scenario #4.3 EUV and DP/MP Market Share Ramp Rates for Each Supplier as Function of Player Action (Corresponds to Figure 13 in Chapter 4)

Assumed actions of players	Modeling MS by year	Year (t)										
Chipmakers: No Financing		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-I, Nikon-I)	$MS_{ASML,\ t,\ DP/MP}$	80%	80%	80%	80%	75%	70%	60%	45%	30%	20%	20%
	$MS_{ASML,\ t,\ EUV}$	0%	0%	0%	0%	5%	10%	20%	30%	40%	40%	40%
	$MS_{Nikon,\ t,\ DP/MP}$	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
	$MS_{Nikon,\ t,\ EUV}$	0%	0%	0%	0%	0%	0%	0%	5%	10%	20%	20%
Chipmakers: No Financing		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-I, Nikon-DI)	$MS_{ASML,\ t,\ DP/MP}$	80%	80%	80%	80%	75%	70%	60%	50%	35%	20%	20%
	$MS_{ASML,\ t,\ EUV}$	0%	0%	0%	0%	5%	10%	20%	30%	45%	60%	60%
	$MS_{Nikon,\ t,\ DP/MP}$	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%

	$MS_{Nikon,\ t,\ EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
Chipmakers: No Financing		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-DI, Nikon-I)	$MS_{ASML,\ t,\ DP/MP}$	80%	80%	80%	80%	70%	60%	50%	45%	35%	20%	20%
	$MS_{ASML,\ t,\ EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
	$MS_{Nikon,\ t,\ DP/MP}$	20%	20%	20%	20%	30%	40%	50%	45%	35%	20%	20%
	$MS_{Nikon,\ t,\ EUV}$	0%	0%	0%	0%	0%	0%	0%	10%	30%	60%	60%
Chipmakers: No Financing		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-DI, Nikon-DI)	$MS_{ASML,\ t,\ DP/MP}$	80%	80%	80%	80%	80%	80%	80%	80%	80%	80%	80%
	$MS_{ASML,\ t,\ EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
	$MS_{Nikon,\ t,\ DP/MP}$	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
	$MS_{Nikon,\ t,\ EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
Chipmakers: Finance ASML Only		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-I, Nikon-I)	$MS_{ASML,\ t,\ DP/MP}$	80%	80%	80%	75%	70%	60%	50%	35%	20%	20%	20%
	$MS_{ASML,\ t,\ EUV}$	0%	0%	0%	5%	10%	20%	30%	40%	50%	40%	40%
	$MS_{Nikon,\ t,\ DP/MP}$	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
	$MS_{Nikon,\ t,\ EUV}$	0%	0%	0%	0%	0%	0%	0%	5%	10%	20%	20%
Chipmakers: Finance ASML Only		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-I, Nikon-DI)	$MS_{ASML,\ t,\ DP/MP}$	80%	80%	80%	75%	70%	60%	50%	40%	30%	20%	20%
	$MS_{ASML,\ t,\ EUV}$	0%	0%	0%	5%	10%	20%	30%	40%	50%	60%	60%
	$MS_{Nikon,\ t,\ DP/MP}$	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
	$MS_{Nikon,\ t,\ EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
Chipmakers: Finance ASML Only		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-DI, Nikon-I)	$MS_{ASML,\ t,\ DP/MP}$	80%	80%	80%	80%	80%	80%	80%	60%	40%	20%	20%
	$MS_{ASML,\ t,\ EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
	$MS_{Nikon,\ t,\ DP/MP}$	20%	20%	20%	20%	20%	20%	20%	30%	30%	20%	20%
	$MS_{Nikon,\ t,\ EUV}$	0%	0%	0%	0%	0%	0%	0%	10%	30%	60%	60%
Chipmakers: Finance ASML Only		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-DI, Nikon-DI)	$MS_{ASML,\ t,\ DP/MP}$	80%	80%	80%	80%	80%	80%	80%	80%	80%	80%	80%
	$MS_{ASML,\ t,\ EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
	$MS_{Nikon,\ t,\ DP/MP}$	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
	$MS_{Nikon,\ t,\ EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
Chipmakers: Finance Nikon Only		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-I, Nikon-I)	$MS_{ASML,\ t,\ DP/MP}$	80%	80%	80%	80%	75%	70%	55%	40%	20%	20%	20%

	$MS_{ASML, t, EUV}$	0%	0%	0%	0%	5%	10%	20%	30%	40%	40%	40%
	$MS_{Nikon, t, DP/MP}$	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
	$MS_{Nikon, t, EUV}$	0%	0%	0%	0%	0%	0%	5%	10%	20%	20%	20%
Chipmakers: Finance Nikon Only		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-I, Nikon-DI)	$MS_{ASML, t, DP/MP}$	80%	80%	80%	80%	75%	70%	60%	50%	35%	20%	20%
	$MS_{ASML, t, EUV}$	0%	0%	0%	0%	5%	10%	20%	30%	45%	60%	60%
	$MS_{Nikon, t, DP/MP}$	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
	$MS_{Nikon, t, EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
Chipmakers: Finance Nikon Only		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-DI, Nikon-I)	$MS_{ASML, t, DP/MP}$	80%	80%	80%	80%	70%	60%	45%	40%	40%	20%	20%
	$MS_{ASML, t, EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
	$MS_{Nikon, t, DP/MP}$	20%	20%	20%	20%	30%	40%	45%	40%	20%	20%	20%
	$MS_{Nikon, t, EUV}$	0%	0%	0%	0%	0%	0%	10%	20%	40%	60%	60%
Chipmakers: Finance Nikon Only		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-DI, Nikon-DI)	$MS_{ASML, t, DP/MP}$	80%	80%	80%	80%	80%	80%	80%	80%	80%	80%	80%
	$MS_{ASML, t, EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
	$MS_{Nikon, t, DP/MP}$	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
	$MS_{Nikon, t, EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
Chipmakers: Finance Both Suppliers		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-I, Nikon-I)	$MS_{ASML, t, DP/MP}$	80%	80%	80%	75%	70%	60%	50%	30%	20%	20%	20%
	$MS_{ASML, t, EUV}$	0%	0%	0%	5%	10%	20%	30%	40%	45%	40%	40%
	$MS_{Nikon, t, DP/MP}$	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
	$MS_{Nikon, t, EUV}$	0%	0%	0%	0%	0%	0%	5%	10%	15%	20%	20%
Chipmakers: Finance Both Suppliers		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-I, Nikon-DI)	$MS_{ASML, t, DP/MP}$	80%	80%	80%	75%	70%	60%	50%	40%	30%	20%	20%
	$MS_{ASML, t, EUV}$	0%	0%	0%	5%	10%	20%	30%	40%	50%	60%	60%
	$MS_{Nikon, t, DP/MP}$	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
	$MS_{Nikon, t, EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
Chipmakers: Finance Both Suppliers		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-DI, Nikon-I)	$MS_{ASML, t, DP/MP}$	80%	80%	80%	80%	70%	60%	60%	50%	40%	20%	20%
	$MS_{ASML, t, EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
	$MS_{Nikon, t, DP/MP}$	20%	20%	20%	20%	30%	40%	30%	30%	20%	20%	20%
	$MS_{Nikon, t, EUV}$	0%	0%	0%	0%	0%	0%	10%	20%	40%	60%	60%

Chipmakers: Finance Both Suppliers		2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021
(ASML-DI, Nikon-DI)	$MS_{ASML,\ t,\ DP/MP}$	80%	80%	80%	80%	80%	80%	80%	80%	80%	80%	80%
	$MS_{ASML,\ t,\ EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
	$MS_{Nikon,\ t,\ DP/MP}$	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
	$MS_{Nikon,\ t,\ EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%

Table 44: Scenario #4.4 EUV and DP/MP Market Share Ramp Rates for Each Supplier as Function of Player Action (Corresponds to Figure 14 in Chapter 4)

Assumed actions of players	Modeling MS by year	Year (t)										
Chipmakers: No Financing		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-I, Nikon-I)	$MS_{ASML,\ t,\ DP/MP}$	80%	80%	80%	80%	75%	70%	60%	45%	30%	20%	20%
	$MS_{ASML,\ t,\ EUV}$	0%	0%	0%	0%	5%	10%	20%	30%	40%	40%	40%
	$MS_{Nikon,\ t,\ DP/MP}$	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
	$MS_{Nikon,\ t,\ EUV}$	0%	0%	0%	0%	0%	0%	0%	5%	10%	20%	20%
Chipmakers: No Financing		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-I, Nikon-DI)	$MS_{ASML,\ t,\ DP/MP}$	80%	80%	80%	80%	75%	70%	60%	50%	35%	20%	20%
	$MS_{ASML,\ t,\ EUV}$	0%	0%	0%	0%	5%	10%	20%	30%	45%	60%	60%
	$MS_{Nikon,\ t,\ DP/MP}$	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
	$MS_{Nikon,\ t,\ EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
Chipmakers: No Financing		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-DI, Nikon-I)	$MS_{ASML,\ t,\ DP/MP}$	80%	80%	80%	80%	70%	60%	50%	45%	35%	20%	20%
	$MS_{ASML,\ t,\ EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
	$MS_{Nikon,\ t,\ DP/MP}$	20%	20%	20%	20%	30%	40%	50%	45%	35%	20%	20%
	$MS_{Nikon,\ t,\ EUV}$	0%	0%	0%	0%	0%	0%	0%	10%	30%	60%	60%
Chipmakers: No Financing		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-DI, Nikon-DI)	$MS_{ASML,\ t,\ DP/MP}$	80%	80%	80%	80%	80%	80%	80%	80%	80%	80%	80%
	$MS_{ASML,\ t,\ EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
	$MS_{Nikon,\ t,\ DP/MP}$	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
	$MS_{Nikon,\ t,\ EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
Chipmakers: Finance ASML Only		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-I, Nikon-I)	$MS_{ASML,\ t,\ DP/MP}$	80%	80%	80%	75%	70%	60%	50%	35%	20%	20%	20%
	$MS_{ASML,\ t,\ EUV}$	0%	0%	0%	5%	10%	20%	30%	40%	50%	40%	40%
	$MS_{Nikon,\ t,\ DP/MP}$	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
	$MS_{Nikon,\ t,\ EUV}$	0%	0%	0%	0%	0%	0%	0%	5%	10%	20%	20%

Chipmakers: Finance ASML Only		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-I, Nikon-DI)	$MS_{ASML, t, DP/MP}$	80%	80%	80%	75%	70%	60%	50%	40%	30%	20%	20%
	$MS_{ASML, t, EUV}$	0%	0%	0%	5%	10%	20%	30%	40%	50%	60%	60%
	$MS_{Nikon, t, DP/MP}$	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
	$MS_{Nikon, t, EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
Chipmakers: Finance ASML Only		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-DI, Nikon-I)	$MS_{ASML, t, DP/MP}$	80%	80%	80%	80%	80%	80%	80%	60%	40%	20%	20%
	$MS_{ASML, t, EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
	$MS_{Nikon, t, DP/MP}$	20%	20%	20%	20%	20%	20%	20%	30%	30%	20%	20%
	$MS_{Nikon, t, EUV}$	0%	0%	0%	0%	0%	0%	0%	10%	30%	60%	60%
Chipmakers: Finance ASML Only		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-DI, Nikon-DI)	$MS_{ASML, t, DP/MP}$	80%	80%	80%	80%	80%	80%	80%	80%	80%	80%	80%
	$MS_{ASML, t, EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
	$MS_{Nikon, t, DP/MP}$	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
	$MS_{Nikon, t, EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
Chipmakers: Finance Nikon Only		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-I, Nikon-I)	$MS_{ASML, t, DP/MP}$	80%	80%	80%	80%	75%	70%	55%	40%	20%	20%	20%
	$MS_{ASML, t, EUV}$	0%	0%	0%	0%	5%	10%	20%	30%	40%	40%	40%
	$MS_{Nikon, t, DP/MP}$	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
	$MS_{Nikon, t, EUV}$	0%	0%	0%	0%	0%	0%	5%	10%	20%	20%	20%
Chipmakers: Finance Nikon Only		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-I, Nikon-DI)	$MS_{ASML, t, DP/MP}$	80%	80%	80%	80%	75%	70%	60%	50%	35%	20%	20%
	$MS_{ASML, t, EUV}$	0%	0%	0%	0%	5%	10%	20%	30%	45%	60%	60%
	$MS_{Nikon, t, DP/MP}$	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
	$MS_{Nikon, t, EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
Chipmakers: Finance Nikon Only		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-DI, Nikon-I)	$MS_{ASML, t, DP/MP}$	80%	80%	80%	80%	70%	60%	45%	40%	40%	20%	20%
	$MS_{ASML, t, EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
	$MS_{Nikon, t, DP/MP}$	20%	20%	20%	20%	30%	40%	45%	40%	20%	20%	20%
	$MS_{Nikon, t, EUV}$	0%	0%	0%	0%	0%	0%	10%	20%	40%	60%	60%
Chipmakers: Finance Nikon Only		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-DI, Nikon-DI)	$MS_{ASML, t, DP/MP}$	80%	80%	80%	80%	80%	80%	80%	80%	80%	80%	80%
	$MS_{ASML, t, EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%

	$MS_{Nikon,\ t,\ DP/MP}$	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
	$MS_{Nikon,\ t,\ EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
Chipmakers: Finance Both Suppliers		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-I, Nikon-I)	$MS_{ASML,\ t,\ DP/MP}$	80%	80%	80%	75%	70%	60%	50%	30%	20%	20%	20%
	$MS_{ASML,\ t,\ EUV}$	0%	0%	0%	5%	10%	20%	30%	40%	45%	40%	40%
	$MS_{Nikon,\ t,\ DP/MP}$	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
	$MS_{Nikon,\ t,\ EUV}$	0%	0%	0%	0%	0%	0%	5%	10%	15%	20%	20%
Chipmakers: Finance Both Suppliers		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-I, Nikon-DI)	$MS_{ASML,\ t,\ DP/MP}$	80%	80%	80%	75%	70%	60%	50%	40%	30%	20%	20%
	$MS_{ASML,\ t,\ EUV}$	0%	0%	0%	5%	10%	20%	30%	40%	50%	60%	60%
	$MS_{Nikon,\ t,\ DP/MP}$	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
	$MS_{Nikon,\ t,\ EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
Chipmakers: Finance Both Suppliers		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-DI, Nikon-I)	$MS_{ASML,\ t,\ DP/MP}$	80%	80%	80%	80%	70%	60%	60%	50%	40%	20%	20%
	$MS_{ASML,\ t,\ EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
	$MS_{Nikon,\ t,\ DP/MP}$	20%	20%	20%	20%	30%	40%	30%	30%	20%	20%	20%
	$MS_{Nikon,\ t,\ EUV}$	0%	0%	0%	0%	0%	0%	10%	20%	40%	60%	60%
Chipmakers: Finance Both Suppliers		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML-DI, Nikon-DI)	$MS_{ASML,\ t,\ DP/MP}$	80%	80%	80%	80%	80%	80%	80%	80%	80%	80%	80%
	$MS_{ASML,\ t,\ EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
	$MS_{Nikon,\ t,\ DP/MP}$	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
	$MS_{Nikon,\ t,\ EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%

Table 45: Scenario #4.5 EUV and DP/MP Market Share Ramp Rates for Each Supplier as Function of Player Action (Corresponds to Figure 15 in Chapter 4)

Assumed actions of players	Modeling MS by year	Year (t)										
Chipmakers: ALL ACTIONS		**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**
(ASML – ALL ACTIONS) (Nikon – ALL ACTIONS)	$MS_{ASML,\ t,\ DP/MP}$	80%	80%	80%	80%	80%	80%	80%	80%	80%	80%	80%
	$MS_{ASML,\ t,\ EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
	$MS_{Nikon,\ t,\ DP/MP}$	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
	$MS_{Nikon,\ t,\ EUV}$	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%

A.5 Example EUVL Payoff Calculations for Equipment Suppliers

Let us arbitrarily choose to calculate ASML's payoff in Scenario #4.2, the "Lower EUV ramp" scenario corresponding to Figure 12 assuming Chipmakers choose 'Finance ASML only', ASML chooses 'Invest', and Nikon chooses 'Don't Invest'. From Figure 12 we see that ASML's E(NPV) in this situation is estimated to be $19.8B.

Using the intermediate variable calculations in Section A.3 above, ASML's appropriate payoff is given by applying Equation (A.5) to this particular state of the world within Scenario #4.2:

$$\begin{aligned}\pi_{ASML,0}(\text{'Finance ASML Only', 'Invest','Don't Invest'}) &= \pi_{ASML,0}(\text{'FA', 'I','D'}) \\ &= E_0\left[\sum_{t=1}^{10}\left[\delta^t\left(m_{net,DP/MP}R_{ASML,t,DP/MP}(\text{'FA', 'I','D'}) \right.\right.\right. \\ &\qquad \left.\left.\left. + m_{net,EUV}R_{ASML,t,EUV}(\text{'FA', 'I','D'})\right)\right]\right] \\ &\qquad - I_{ASML,0}(\text{'FA', 'I','D'})\end{aligned} \tag{A.28}$$

Where, applying Equation (A.6), the revenue of ASML in year t flowing from 193i DP/MP technology, $R_{i,t,DP/MP}$, is given by:

$$\begin{aligned}R_{ASML,t,DP/MP}(\text{'FA', 'I','D'}) &= f_{sr,DP/MP}\ell_{ASML,t,DP/MP}(\text{'FA', 'I','D'})c_{t,DP/MP}\end{aligned} \tag{A.29}$$

Similarly, applying Equation (A.7), the revenue of ASML in year t flowing from EUV technology, $R_{i,t,EUV}$, is given by:

$$R_{ASML,t,EUV}(\text{'FA', 'I','D'}) = f_{sr,EUV}\ell_{ASML,t,EUV}(\text{'FA', 'I','D'})c_{t,EUV} \tag{A.30}$$

From Equation (A.16) we see that: $I_{ASML,0} = \$1B$.

From Equation (A.20): $c_{t,EUV} = r_{supplier\ pricing,t}c_{0,EUV}\left(1 + g_{EUV,cost}\right)^t$

Where $r_{\text{supplier pricing,t}} = 1.0 \; \forall \; t$. This is true since:

$0 < MS_{ASML,t,EUV}$('Finance ASML Only', 'Invest','Don't Invest') + $MS_{ASML,t,DP/MP}$('Finance ASML Only', 'Invest','Don't Invest') < 1 $\forall \; t$, according to the market share values in Table 42 (the MS ramp table for Scenario #4.2). Said differently, this inequality implies that both ASML and Nikon have non-zero critical patterning market shares in every year considered under the conditions being evaluated here.

Given parameters $c_{0,EUV} = \frac{\$66.9}{\text{critical layer}}$ and $g_{\text{EUV cost}} = 5\%$ (both from Table 40), we calculate from Equation (A.20) that:

$$c_{t,EUV}(for\ t = 2011, \dots, 2021) = \vec{c}_{t,EUV} = [66.9, 70.2, 73.8, 77.4, 81.3, 85.4, 89.7, 94.1, 98.8, 103.8, 109.0] \quad (A.31)$$

Given $r_{0,EUV}$=1.53 and $g_{\text{cost ratio}}$=10% (both from Table 40), we calculate from Equation (A.21) that:

$$r_t(for\ t = 2011, \dots, 2021) = \vec{r}_t = [1.53, 1.68, 1.85, 2.04, 2.24, 2.46, 2.71, 2.98, 3.28, 3.61, 3.97] \quad (A.32)$$

We calculate (from Equation (A.22)) that:

$$c_{t,DP/MP}(for\ t = 2011, \dots, 2021) = \vec{c}_{t,DP/MP} = \vec{r}_t \circ \vec{c}_{t,EUV} = [102.4, 118.2, 136.5, 157.7, 182.2, 210.4, 243.0, 280.7, 324.2, 374.4, 432.5] \quad (A.33)$$

Where the ring operator ($\circ$) is used here to signify element-wise multiplication of the two vectors.

Now we calculate the yearly number of layers patterned by ASML via EUV and via DP/MP. Given n_0 = 7 and $g_{\text{critical layers}}$=12% (both from Table 40) we know that:

$$n_t(for\ t = 2011, \dots, 2021) = \vec{n}_t = [7.00, 7.84, 8.78, 9.83, 11.01, 12.34, 13.82, 15.47, 17.33, 19.41, 21.74] \quad (A.34)$$

Given parameters $W_{0,\text{ total}}$=4.17x10^7, $f_{\text{leading edge}}$=50%, and $g_{\text{wafer}} = 10\%$ (all from Table 40), we calculate from Equation (A.23) that:

$$W_{t,leading\ edge}(for\ t = 2011, \dots, 2021) = \vec{W}_{t,leading\ edge} = [2.08\text{x}10^7, 2.2910^7, 2.52\text{x}10^7, 2.77\text{x}10^7, 3.05\text{x}10^7, 3.36\text{x}10^7, 3.69\text{x}10^7, 4.06\text{x}10^7, 4.47\text{x}10^7, 4.91\text{x}10^7, 5.40\text{x}10^7]$$

Hence, applying Equation (A.25) we calculate that:

$$\ell_t(for\ t = 2011, \dots, 2021) = \vec{\ell}_t = \vec{W}_{t,leading\ edge} \circ \vec{n}_t = \begin{bmatrix} 1.46\text{x}10^8, 1.80\text{x}10^8, 2.21\text{x}10^8, 2.73\text{x}10^8, 3.36\text{x}10^8, 4.14\text{x}10^8, \\ 5.10\text{x}10^8, 6.28\text{x}10^8, 7.74\text{x}10^8, 9.54\text{x}10^8, 1.17\text{x}10^9 \end{bmatrix} \quad \text{(A.35)}$$

Thus, applying Equation (A.26), we find that:

$$\ell_{ASML,t,DP/MP}(\text{'Finance ASML Only', 'Invest','Don't Invest'}) = MS_{ASML,t,DP/MP}(\text{'Finance ASML Only', 'Invest','Don't Invest'})\ell_t \quad \text{(A.36)}$$

From Table 42, we know:

$$\overrightarrow{MS}_{ASML,t,DP/MP}(\text{'Finance ASML Only', 'Invest','Don't Invest'}) = [80\%, 75\%, 70\%, 60\%, 50\%, 40\%, 30\%, 20\%, 20\%, 20\%, 20\%] \quad \text{(A.37)}$$

Thus combining Equations (A.35) and (A.37) gives:

$$\vec{\ell}_{ASML,t,DP/MP}(\text{'Finance ASML Only', 'Invest','Don't Invest'}) = \overrightarrow{MS}_{ASML,t,DP/MP}(\text{'Finance ASML Only', 'Invest','Don't Invest'}) \circ \vec{\ell}_t = [1.17\text{x}10^8, 1.35\text{x}10^8, 1.55\text{x}10^8, 1.64\text{x}10^8, 1.68\text{x}10^8, 1.66\text{x}10^8, 1.53\text{x}10^8, 1.26\text{x}10^8, 1.55\text{x}10^8, 1.91\text{x}10^8, 2.35\text{x}10^8] \quad \text{(A.38)}$$

Similarly, applying Equation (A.27), we find that:

$$\ell_{ASML,t,EUV}(\text{'Finance ASML Only', 'Invest','Don't Invest'}) = MS_{ASML,t,EUV}(\text{'Finance ASML Only', 'Invest','Don't Invest'})\ell_t \quad \text{(A.39)}$$

Again, from Table 42, we know:

$$\overrightarrow{MS}_{ASML,t,EUV}(\text{'Finance ASML Only', 'Invest','Don't Invest'}) = [0\%, 5\%, 10\%, 20\%, 30\%, 40\%, 50\%, 60\%, 60\%, 60\%, 60\%] \quad \text{(A.40)}$$

Thus combining Equations (A.35) and (A.40) gives:

$$\begin{aligned}\vec{\ell}_{ASML,t,EUV}&\text{('Finance ASML Only', 'Invest','Don't Invest')}\\ &= \overrightarrow{MS}_{ASML,t,EUV}\text{('Finance ASML Only', 'Invest','Don't Invest')} \circ \vec{\ell}_t\\ &= [0, 8.98\text{x}10^6, 2.21\text{x}10^7, 5.45\text{x}10^7, 1.01\text{x}10^8, 1.66\text{x}10^8,\\ &\quad 2.55\text{x}10^8, 3.77\text{x}10^8, 4.64\text{x}10^8, 5.72\text{x}10^8, 7.05\text{x}10^8]\end{aligned} \tag{A.41}$$

Thus, given $f_{sr,\,DP/MP}$ =0.33 (from Table 40), and plugging in the numbers from Equations (A.33) and (A.38), into Equation (A.29) we calculate that:

$$\begin{aligned}\vec{R}_{ASML,t,DP/MP} = f_{sr,DP/MP}\vec{\ell}_{ASML,t,DP/MP}&\text{('Finance ASML Only', 'Invest','Don't Invest')} \circ \vec{c}_{t,DP/MP}=\\ &[3.94\text{x}10^9, 5.26\text{x}10^9, 6.98\text{x}10^9, 8.52\text{x}10^9, 1.01\text{x}10^{10}, 1.15\text{x}10^{10},\\ &1.23\text{x}10^{10}, 1.16\text{x}10^{10}, 1.66\text{x}10^{10}, 2.36\text{x}10^{10}, 3.35\text{x}10^{10}]\end{aligned} \tag{A.42}$$

Similarly, given $f_{sr,\,EUV}$ =0.68 (from Table 40), and plugging in the numbers from Equations (A.31) and (A.41), into Equation (A.30) we calculate that:

$$\begin{aligned}\vec{R}_{ASML,t,EUV} = f_{sr,EUV}\vec{\ell}_{ASML,t,EUV}&\text{('Finance ASML Only', 'Invest','Don't Invest')} \circ \vec{c}_{t,EUV}=\\ &[0, 4.29\text{x}10^8, 1.11\text{x}10^9, 2.87\text{x}10^9, 5.57\text{x}10^9, 9.61\text{x}10^9,\\ &1.55\text{x}10^{10}, 2.41\text{x}10^{10}, 3.12\text{x}10^{10}, 4.04\text{x}10^{10}, 5.22\text{x}10^{10}]\end{aligned} \tag{A.43}$$

Recall that the annual discounted expected profits are summed from 2012 to 2021 (i.e., omitting the first (2011) number for profits which was simply used as a starting point for many of the growth rates assumed in this model). Knowing that δ=0.15, $m_{net,DP/MP}$=15% and $m_{net,EUV}$=20% (all from Table 40), and plugging in numbers from Equations (A.16), (A.42), and (A.43) into Equation (A.28) gives the desired result that:

$$\begin{aligned}\pi_{ASML,0}&\text{('FA', 'I','D')}=E_0\left[\sum_{t=1}^{10}\delta^t\left(m_{net,DP/MP}R_{ASML,t,DP/MP}\text{('FA', 'I','D')} +\right.\right.\\ &\left.\left.m_{net,EUV}R_{ASML,t,EUV}\text{('FA', 'I','D')}\right)\right] - I_{ASML,0}\text{('FA', 'I','D')}\\ &= \$19.8B \text{ (for Scenario \#4.2)}\end{aligned} \tag{A.44}$$

Or, expanding this out in full detail gives:

$$\begin{aligned}
&\pi_{ASML,0}(\text{'FA', 'I','D'}) \\
&= \sum_{t=1}^{10} \left[\left(\frac{1}{1+0.15} \right)^{t} \left(m_{net,DP/MP} \vec{R}_{ASML,t,DP/MP}(\text{'FA', 'I','D'}) \right.\right. \\
&\qquad \left.\left. + m_{net,EUV} \vec{R}_{ASML,t,EUV}(\text{'FA', 'I','D'}) \right) \right] - I_{ASML,0}(\text{'FA', 'I','D'}) \\
&\qquad = \frac{1}{1.15} \left(0.15(5.26\text{x}10^{9}) + 0.20(1.11\text{x}10^{9}) \right) + \cdots \\
&\qquad + \frac{1}{1.15^{10}} \left(0.15(3.35\text{x}10^{10}) + 0.20(5.22\text{x}10^{10}) \right) - 1\text{x}10^{9} \\
&\qquad = \$19.8B \text{ (for Scenario \#4.2)}
\end{aligned} \tag{A.45}$$

Thus, we have completed the full calculation and retrieved the relevant payoff estimate given the player, scenario, and player actions chosen. Any other equipment supplier payoff estimates in Figure 11 through Figure ***19*** can be recovered in a like manner.

Appendix B: 450mm Model Payoff Calculation Details

Chapter 5 includes discussion regarding the following aspects of the 450mm wafer model: conceptual game-theoretic framework, essential assumptions, values of payoffs estimates, and sensitivity analyses to changes in model input parameters. This appendix (Appendix B) is meant to provide a much more comprehensive explanation of how Intel's, Samsung's, and TSMC's payoff estimates are derived in this model. It is meant to provide full traceability – allowing calculation of the payoff estimates in Figure 26 through Figure *34* for those who are interested. This appendix follows a logical sequence of steps to achieve this aim.

First, a complete list of 450mm model acronyms, variables, and parameters used in the payoff calculations will be provided for ease of cross-reference (Table 46 and Table *47*). Second, more complete expressions of the game-theoretic objective functions (a.k.a., payoff functions) and optimization formulations of the three players will be provided and discussed (Section B.2). Third, an algebraic set of "linking equations" with numerous model input parameters will be given (Section B.3). Fourth, all 450mm model input parameter estimates will be tabulated, with data source attribution and the author's reasoning about the estimates (Table 48). Finally, an example calculation will be performed to ensure the full traceability to the payoff estimates shown in Figures 26 through Figure *34*.

Table 46: Table of Terms, Acronyms, and Symbols for 450mm Model (Chapter 5)

Acronyms/Symbols	Meaning
450mm	450mm diameter silicon wafer substrates (and related semiconductor manufacturing technology)
CAGR	Compound Annual Growth Rate
COGS	Cost of Goods Sold
E_0	Expectation operator given information at time 0
I	Intel Corporation
IDM	Integrated Device Manufacturer
IST	The grouping of the three largest chip manufacturers: Intel (I), Samsung (S), and TSMC (T)
MS	Market Share
NT$	New Taiwan Dollars (the official currency of Taiwan)
S	Samsung Electronics
T	TSMC (Taiwan Semiconductor Manufacturing Corporation)

*B.1 Complete Reference List of 450mm Model Input Parameters, Decision Variables, and Other "Intermediate" Model Variables**

*Note: This table is meant to be a complete list (for ease of reference) of: model input parameters, decision variables, "intermediate" payoff variables, and other miscellaneous model inputs. The (direct) model input parameter (base case) estimates can be found in Table 48. A fuller description of the decision variables can be found in Section B.2. The equations which link "intermediate variables" with the model input parameters to calculate sub-components of the player payoff estimates are given in Section B.3 below.

Table 47: Input Model Parameters, Intermediate, and Payoff Variables for 450mm Model (Chapter 5)

Variable(s)/Parameter(s)	Description	Type
δ	Discount Factor (annual). $\delta = 1/(1+r)$, where r is the annual discount rate assumed.	parameter
$\pi_{i,0}$	E(NPV) payoff function for chipmaker i in year 0 (2011)	payoff var.
$B_{i,t,\text{market share}}$	Market share gain or loss due to 450mm technology for chipmaker i in year t.	intermediate
$B_{i,t,\text{mfg cost}}$	Manufacturing cost savings due to 450mm technology for chipmaker i in year t.	intermediate
$\Delta C_{i,t,450mm}$	Reduction in COGS that chipmaker i experiences in year t due to 450mm technology	intermediate
$COGS_{Intel}$	Approximate COGS for Intel Corporation in 2010($B USD)	parameter

Variable(s)/Parameter(s)	Description	Type
$COGS_{Samsung}$	Approximate COGS for Samsung Corporation in 2010($B USD)	parameter
$COGS_{TSMC}$	Approximate COGS for TSMC Corporation in 2010($B USD)	parameter
$d_{k, j}$	Market share percentage change in Scenario #5.k (see Table 14) given investment role j of chipmaker in question given its action and the action of the other two chipmakers	parameter
$f_{chipmaker\ profit}$	Fraction of chipmaker manufacturing cost savings (from 450mm) which are converted to chipmaker profits	parameter
$f_{financing}$	Fraction of remaining required financing which the chipmakers must collectively provide to the equipment suppliers in order to entice them to pursue 450mm development as quickly as possible (not *directly* used in payoff calculations)	miscellaneous
$f_{mfg\ savings}$	Fraction of COGS reduction to be expected from 450mm wafer manufacturing	parameter
$g_{450mm\ COGS}$	Growth rate of COGS for each chipmaker assuming that no 450mm technology is developed (450mm is assumed to have a "robust running start" before the benefits from 450mm COGS reductions start to accrue. See Figure 25)	parameter
$\mathbf{h_{i,t}}$	Step function which designates the year in which manufacturing cost savings and market share gains/losses start for chipmaker i (as a function of the strategic actions by each of IST).	intermediate
i	Index for arbitrary chipmaker. Possible chipmakers are i ϵ {Intel, Samsung, and TSMC}	miscellaneous
I_{Total}	Additional non-recurring engineering (i.e., R&D) costs remaining for full 450mm technology development (in 2011)	parameter
I_{Intel}	450mm equipment R&D investment required by Intel to confer the benefits associated with being an "early investor" in 450mm technology	parameter

Variable(s)/Parameter(s)	Description	Type
$I_{Samsung}$	450mm equipment R&D investment required by Samsung to confer the benefits associated with being an "early investor" in 450mm technology	parameter
I_{TSMC}	450mm equipment R&D investment required by TSMC to confer the benefits associated with being an "early investor" in 450mm technology	parameter
j	Index for arbitrary investment role j of chipmaker in question given its action and the action of the other two chipmakers. Possible roles are: $j \in$ {all-invest, sole-investor, dual-laggard, dual-investor, sole-laggard}	miscellaneous
k	Index for arbitrary 450mm scenario corresponding to Scenario #5.k as defined in Table 14 in Chapter 5. Possible scenarios are: $k \in \{1, 2, 3, 4, 5, 6, 7, 8\}$	miscellaneous
m_{Intel}	Net profit margin assumed for Intel applied to the 450mm-induced market share revenue gains/losses	parameter
$m_{Samsung}$	Net profit margin assumed for Samsung applied to the 450mm-induced market share revenue gains/losses	parameter
m_{TSMC}	Net profit margin assumed for TSMC applied to the 450mm-induced market share revenue gains/losses	parameter
$\Delta MS_{i,t}$	Fraction of overall market change for chipmaker i in year t	intermediate
$R_{industry}$	Estimated total semiconductor industry revenue in 2010 ($B USD)	parameter
R_{Intel} (Not directly used in payoff calculation. Provided as context for annual COGS amounts)	Approximate semiconductor revenue for Intel Corporation in 2010($B USD)	parameter
$R_{Samsung}$ (Not directly used in payoff calculation. Provided as context for annual COGS amounts)	Approximate semiconductor revenue for Samsung Corporation in 2010($B USD)	parameter
R_{TSMC} (Not directly used in payoff calculation. Provided as context for annual COGS amounts)	Approximate semiconductor revenue for TSMC Corporation in 2010($B USD)	parameter

Variable(s)/Parameter(s)	Description	Type
s_I	Decision variable for Intel	decision var.
S_I	Strategy set for Intel	(related to) decision var.
s_S	Decision variable for Samsung	decision var.
S_S	Strategy set for Samsung	(related to) decision var.
s_T	Decision variable for TSMC	decision var.
S_T	Strategy set for TSMC	(related to) decision var.
s_x^*	Optimal strategy for player X	decision var.
T	Index for calendar Year: t=0 corresponds to 2011 and t=20 corresponds to 2031	miscellaneous
t_{ending}	Year up until which cash flow associated with manufacturing cost savings and market share changes were calculated (calendar year)	parameter
$\Delta t_{benefits,all\ invest}$	Length of time between chipmaker investment (t_0=2011) and start of manufacturing cost savings and market share gains for "early investing" firms if all three players invest (years)	parameter
$\Delta t_{benefits,two\ investors}$	Length of time between chipmaker investment (t_0=2011) and start of manufacturing cost savings and market share gains for "early investing" firms if two players invest (years)	parameter
$\Delta t_{benefits,one\ investor}$	Length of time between chipmaker investment (t_0=2011) and start of manufacturing cost savings and market share gains for "early investing" firms if one players invests (years)	parameter
$\Delta t_{fast\ followers}$	Length of time between start of benefits accrued by early adopting firms and manufacturing cost savings and market share losses experienced by fast following firms (years)	parameter

B.2 Players' Objective Functions and Optimization Formulations (450mm Game)

B.2.1 Chipmakers' Strategy Sets and Objective Functions

To formally represent the EUVL R&D game the strategies of each player are defined as: s_I = strategy of Intel, s_S = strategy of Samsung, s_T = strategy of TSMC. Note per Figure 24 and the surrounding discussions in Chapter 5, the strategy sets of each player in the game should be defined as:

$$S_I = S_S = S_T = \{\text{'Invest', 'Don't Invest'}\} \tag{B.1}$$

where $s_I \in S_I$ and $s_S \in S_S$ and $s_T \in S_T$.

Given those strategy sets and the sub-components of profit considered (see Section 5.2) we can define the payoffs for each chipmaker to be:

$$\pi_{i,0}(s_I, s_S, s_T) = E_0\left[\sum_{t=1}^{20}\left[\delta^t\left(B_{i,t,mfg\ cost}(s_I, s_S, s_T) + B_{i,t,market\ share}(s_I, s_S, s_T)\right)\right]\right] - I_{i,0}(s_i) \tag{B.2}$$

where, t=0 corresponds to 2011. Also, for chipmaker i in year t, $B_{i,t,mfg\ cost}$ is the manufacturing cost savings from 450mm technology, and $B_{i,t,market\ share}$ is the market share gain (or loss) due to 450mm technology. $I_{i,0}$, the last term in Equation (B.2), is the R&D investment magnitude expended by chipmaker i in year 0 (2011).

Further, expanding the two components of chipmaker benefits/losses gives Equations (B.3) and (B.4) below.

$$B_{i,t,mfg\ cost}(s_I, s_S, s_T) = \Delta C_{i,t,450mm}(s_I, s_S, s_T) f_{chipmaker\ profit} \tag{B.3}$$

where $\Delta C_{i,t,450mm}$ is the reduction in COGS that chipmaker i experiences in year t due to 450mm technology and $f_{\text{chipmaker profit}}$ is the fraction of chipmaker manufacturing cost reductions which translates into chipmaker profits.

$$B_{i,t,market\ share}(s_I, s_S, s_T) = \Delta MS_{i,t}(s_I, s_S, s_T) m_i R_{industry} \quad \text{(B.4)}$$

where $\Delta MS_{i,t}$ is the fraction of overall market change in year t, m_i is chipmaker i's profit margin, and $R_{industry}$ is the annual revenue (in $) of the overall semiconductor market in year t.

The expectation operator is included here for completeness, although it is unnecessary for calculating the payoffs in Figure 26 through Figure 34, given that all the player parameter estimates are all deterministic (see Table 48).

B.2.2 Optimization Formulation for the Three Chipmakers

In the Nash Equilibria, the three chipmakers simultaneously solve their optimization problems.

Intel solves:

$$s_I^*(s_S, s_T) = \max_{s_I \epsilon S_I} \pi_{I,0}\left(s_I, s_S^*(s_I, s_T^*), s_T^*(s_I, s_S^*)\right) \quad \text{(B.5)}$$

Samsung solves:

$$s_S^*(s_I, s_T) = \max_{s_S \epsilon S_S} \pi_{S,0}\left(s_I^*(s_S, s_T^*), s_S, s_T^*(s_I^*, s_S)\right) \quad \text{(B.6)}$$

TSMC solves:

$$s_T^*(s_I, s_S) = \max_{s_T \epsilon S_T} \pi_{T,0}(s_I^*(s_S^*, s_T), s_S^*(s_I^*, s_T), s_T) \quad \text{(B.7)}$$

Since the game is a single-stage simultaneous game, the three simultaneous optimizations above complete the game formulation. Now that we have defined, at a high level, the optimization approaches of each player, let us proceed to define the set of more detailed equations which link the 450mm variables and parameters to the ultimate payoff calculations.

B.3 Intermediate Payoff Calculation Sub-Equations or "Linking Equations"

Calculation of 450mm-related Manufacturing Costs Savings of Chipmaker i in Year t (see Table 48 for data sources of related parameters):

$$\Delta C_{i,t,450mm}(s_I, s_S, s_T) = f_{mfg\ savings} COGS_i h_{i,t}(s_I, s_S, s_T) \quad \text{(B.8)}$$

where $h_{i,t}(s_I, s_S, s_T)$ is a step function which determines when the cost savings for chipmaker i start to be realized.

For Scenarios #5.1 through #5.4,

$$h_{i,t}(s_I, s_S, s_T) = \left\{ \begin{array}{c} 0\ if\ 1 \le t \le 4 \\ \left\{ \begin{array}{c} 1\ if\ t = 5\ \ and\ \ (s_I = s_S = s_T = 'Invest') \\ 0\ if\ t = 5\ \ and\ \ all\ other\ strategy\ profiles \end{array} \right\} \\ \left\{ \begin{array}{c} 1\ if\ t = 6\ \ and\ \ (i\ chooses\ 'Invest'\ and\ either\ of - i\ chooses\ 'Invest') \\ 0\ if\ t = 6\ \ and\ \ all\ other\ strategy\ profiles \end{array} \right\} \\ \left\{ \begin{array}{c} 1\ if\ t = 7\ \ and\ \ (i\ \ chooses\ 'Invest'\ or\ both\ of - i\ chooses\ 'Invest') \\ 0\ if\ t = 7\ \ and\ \ all\ other\ strategy\ profiles \end{array} \right\} \\ \left\{ \begin{array}{c} 1\ if\ 8 \le t \le 20\ \ and\ \ (s_I\ or\ s_S\ or\ s_T = '\ Invest') \\ 0\ if\ 8 \le t \le 20\ \ and\ \ all\ other\ strategy\ profiles \end{array} \right\} \end{array} \right\} \quad \text{(B.9)}$$

The purpose behind defining $h_{i,t}(s_I, s_S, s_T)$ this way is to implement the logic behind the parameters $\Delta t_{benefits,all\ invest}$, $\Delta t_{benefits,two\ investors}$, $\Delta t_{benefits,one\ investor}$, and $\Delta t_{fast\ followers}$ chosen for Scenarios #5.1 through #5.4 (see Table 48 for parameter estimates and justifications and Table 14 for a reminder of the 450mm benefit timing for those four scenarios). The $\mathbf{h_{i,t}}$ definition is exactly analogous for Scenarios #5.5 through #5.8 except that $\Delta t_{fast\ followers}$ is now assumed to be 2 years instead of 1 year, which impacts the formulation somewhat.

In Scenario #5.k (as defined in Table 14 in Chapter 5):

$$\Delta MS_{i,t}(s_I, s_S, s_T)$$

$$= \begin{cases} d_{k,all-invest} h_{i,t}(s_I, s_S, s_T) \ \ if\ s_I = s_S = s_T = 'Invest' \\ d_{k,sole-invest} h_{i,t}(s_I, s_S, s_T) \ \ if\ i\ chooses\ 'Invest' and\ both - i\ choose\ 'Don't\ Invest' \\ d_{k,dual-laggard} h_{i,t}(s_I, s_S, s_T) \ \ if\ i\ chooses\ 'Don't\ Invest' and\ either\ (but\ not\ both) \\ of - i\ choose\ 'Don't\ Invest' \\ d_{k,dual-invest} h_{i,t}(s_I, s_S, s_T) \ \ if\ i\ chooses\ 'Invest' and\ either\ (but\ not\ both)\ of - i\ choose \\ 'Invest' \\ d_{k,sole-laggard} h_{i,t}(s_I, s_S, s_T) \ \ if\ i\ chooses\ 'Don't\ Invest' and\ both\ of - i\ choose \\ 'Invest' \\ 0 \ \ if\ s_I = s_S = s_T = 'Invest' \end{cases} \quad (B.10)$$

where the d_k parameters are listed in Table 48 below.

B.4 450mm Model Input Parameters and Data Sources

Table 48: List of 450mm Model Base Case Parameters and their Sources

Model Parameter Symbol	Model Parameter Name	Estimated Parameter Value	Source of Parameter Estimate
Δ	Discount Factor (annual)	0.893 =1/(1+0.12)	450mm wafer technology has significant economic and schedule risk, but it has less technological risk than other semiconductor manufacturing projects of its size (e.g., EUV lithography development). Hence, a discount rate toward the middle of the typical corporate discount range (10%-15%) was chosen. Hence, 12% was chosen.
$COGS_{Intel}$	Approximate COGS for Intel Corporation in 2010($B USD)	15.1	Cost of sales for 2010 (assumed to be approximately COGS for the company overall) is found to be $15.1B in Intel's 2010 annual report (Intel 2010).

Model Parameter Symbol	Model Parameter Name	Estimated Parameter Value	Source of Parameter Estimate
$COGS_{Samsung}$	Approximate COGS for Samsung Corporation in 2010($B USD)	11.8	TSMC's cost of sales/net sales ratio was approximated at 57.4% (see $COGS_{TSMC}$ estimate below). Intel's cost of sales ratio in 2010 was approximately $15.1B/$40.0B = 37.8%. Because Intel has typically had a higher gross margin than Samsung (semiconductor), it can be supposed that Samsung Semi's COGS/Sales ratio will be higher than Intel's. Because TSMC is a foundry, producing chips for others, Samsung Semi's COGS/Sales ratio can be expected to be lower than TSMC's. Lacking a better estimate, a number closer to (but not equal to) Intel's ratio of 42% (cost of sales/net sales) was chosen. Hence, Samsung's COGS in 2010 are approximated as 0.42 ($28.1B) = $11.8B (these numbers are difficult to calculate for Samsung's semiconductor division from Samsung's annual reports due to financial consolidation across many business units besides semiconductors).
$COGS_{TSMC}$	Approximate COGS for TSMC Corporation in 2010($B USD)	7.4	From 2010 TSMC Annual report (TSMC 2010b). TSMC's average cost of sales/net sales ratio for the years 2006 through 2010 was approximately: 57.4% (using US GAAP data taken from page 3 of the annual report linked to above). This implies a baseline assumed annual COGS of ≈ 0.574 ($12.9B) = $7.4B USD in 2010.
$d_{0,j}$ (where j ϵ {all-invest, sole-invest, dual-laggard, dual-invest, sole-laggard})	Percentage market share change for any chipmaker under any set of actions in Scenario #5.0	+ 0.0%	Scenario #5.0 corresponds to an assumption of no market share changes regardless of the investment actions chosen by Intel, Samsung, and TSMC (see Table 14).
$d_{1,j}$ (where j ϵ {all-invest, sole-invest, dual-laggard, dual-invest, sole-laggard})	Percentage market share change for any chipmaker under any set of actions in Scenario #5.1	+ 0.0%	Scenario #5.1 corresponds to an assumption of no market share changes regardless of the investment actions chosen by Intel, Samsung, and TSMC (see Table 14).
$d_{2,\text{ all-invest}}$	Percentage market share change for all investors (in Scenario #5.2)	+ 0.0% (each)	Scenario #5.2 corresponds to 1.5% contestable semiconductor market share and all competition being *among* IST. Thus, if all three of IST invest, then none are expected to gain market share from the others. Hence, no MS changes are expected if all three of IST invest in 450mm technology.

Model Parameter Symbol	Model Parameter Name	Estimated Parameter Value	Source of Parameter Estimate
$d_{2,\text{dual-invest}}$	Percentage market share change for dual investor(in Scenario #5.2)	+0.75% (each)	Scenario #5.2 corresponds to 1.5% contestable semiconductor market share and all competition being *among* IST. Thus, if exactly two of IST invest, then each is expected to split the 1.5% contestable market share gain made from the sole non-investing member of IST. Hence, a +0.75% MS gain for each of the "dual investors".
$d_{2,\text{sole-laggard}}$	Percentage market share change for two lagging firms(in Scenario #5.2)	-1.5%	Scenario #5.2 corresponds to 1.5% contestable semiconductor market share and all competition being *among* IST. Thus, if exactly one of IST chooses not to invest, then it is expected to lose the 1.5% contestable market share gain to the other two members of IST who did invest early on 450mm technology. Hence, a 1.5% MS loss for a "sole laggard".
$d_{2,\text{sole-invest}}$	Percentage market share change for sole investor (in Scenario #5.2)	+1.5%	Scenario #5.2 corresponds to 1.5% contestable semiconductor market share and all competition being *among* IST. Thus, if exactly one of IST invests, then it is expected to gain the 1.5% contestable market share from the dual non-investing members of IST. Hence, a +1.5% MS gain for the "sole investor".
$d_{2,\text{dual-laggard}}$	Percentage market share change for two lagging firms(in Scenario #5.2)	-0.75% (each)	Scenario #5.2 corresponds to 1.5% contestable semiconductor market share and all competition being *among* IST. Thus, if exactly two of IST choose not to invest, then each is expected to lose half of the 1.5% contestable market share to the sole member of IST who did invest early on 450mm technology. Hence, a 0.75% MS loss for each of the "dual laggards".
$d_{3,\text{all-invest}}$	Percentage market share change for all investors (in Scenario #5.3)	+0.25% (each)	Scenario #5.3 corresponds to 1.5% contestable semiconductor market share and half of the contestable MS (i.e., 0.75%) being *among* IST and the remaining half of the contestable MS (i.e., 0.75%) being *between* IST and the smaller chipmakers. Hence, $d_{3,j}$ is defined as $0.5d_{2,j} + 0.5d_{4,j}$ where j defines the investment patterns of IST. Hence, $d_{3,\text{all-invest}} = 0.5*(0.0\%)+0.5*(0.5\%)=+0.25\%$
$d_{3,\text{dual-invest}}$	Percentage market share change for dual investor(in Scenario #5.3)	+0.75% (each)	Scenario #5.3 corresponds to 1.5% contestable semiconductor market share and half of the contestable MS (i.e., 0.75%) being *among* IST and the remaining half of the contestable MS (i.e., 0.75%) being *between* IST and the smaller chipmakers. Hence, $d_{3,j}$ is defined as $0.5d_{2,j} + 0.5d_{4,j}$ where j defines the investment patterns of IST. Hence, $d_{3,\text{dual-invest}} = 0.5*(0.75\%)+0.5*(0.75\%)=+0.75\%$
$d_{3,\text{sole-laggard}}$	Percentage market share change for two lagging firms(in Scenario #5.3)	-0.75%	Scenario #5.3 corresponds to 1.5% contestable semiconductor market share and half of the contestable MS (i.e., 0.75%) being *among* IST and the remaining half of the contestable MS (i.e., 0.75%) being *between* IST and the smaller chipmakers. Hence, $d_{3,j}$ is defined as $0.5d_{2,j} + 0.5d_{4,j}$ where j defines the investment patterns of IST. Hence, $d_{3,\text{sole-laggard}} = 0.5*(-1.5\%)+0.5*(0.0\%)=-0.75\%$

Model Parameter Symbol	Model Parameter Name	Estimated Parameter Value	Source of Parameter Estimate
$d_{3,\text{ sole-invest}}$	Percentage market share change for sole investor (in Scenario #5.3)	+1.5%	Scenario #5.3 corresponds to 1.5% contestable semiconductor market share and half of the contestable MS (i.e., 0.75%) being *among* IST and the remaining half of the contestable MS (i.e., 0.75%) being *between* IST and the smaller chipmakers. Hence, $d_{3,j}$ is defined as $0.5d_{2,j} + 0.5d_{4,j}$ where j defines the investment patterns of IST. Hence, $d_{3,\text{sole-invest}}$ = 0.5*(1.5%)+0.5*(1.5%)=+1.5%
$d_{3,\text{ dual-laggard}}$	Percentage market share change for two lagging firms(in Scenario #5.3)	-0.375% (each)	Scenario #5.3 corresponds to 1.5% contestable semiconductor market share and half of the contestable MS (i.e., 0.75%) being *among* IST and the remaining half of the contestable MS (i.e., 0.75%) being *between* IST and the smaller chipmakers. Hence, $d_{3,j}$ is defined as $0.5d_{2,j} + 0.5d_{4,j}$ where j defines the investment patterns of IST. Hence, $d_{3,\text{dual-laggard}}$ = 0.5*(-.75%)+0.5*(0.0%)=-0.375%
$d_{4,\text{ all-invest}}$	Percentage market share change for all investors (in Scenario #5.4)	+0.5% (each)	Scenario #5.4 corresponds to 1.5% contestable semiconductor market share and all competition *between* IST and smaller chipmakers. Thus, if all three of IST invest, then each are expected to gain one-third of the contestable market share from the smaller chipmakers. Hence, a +0.5% MS is expected for each of IST if all three invest in 450mm technology.
$d_{4,\text{ dual-invest}}$	Percentage market share change for dual investor(in Scenario #5.4)	+0.75% (each)	Scenario #5.4 corresponds to 1.5% contestable semiconductor market share and all competition *between* IST and smaller chipmakers. Thus, if exactly two of IST choose to invest, then each is expected to split the 1.5% contestable market share gain made from the smaller chipmakers. Hence, a +0.75% MS gain for each of the "dual investors".
$d_{4,\text{ sole-laggard}}$	Percentage market share change for two lagging firms(in Scenario #5.4)	+0.0%	Scenario #5.4 corresponds to 1.5% contestable semiconductor market share and all competition *between* IST and smaller chipmakers. Thus, if exactly one of IST chooses not to invest, then it is not expected to lose (or to gain) any of the 1.5% contestable market share (which will come at the expense of the smaller chipmakers. Hence, no MS changes are expected for a "sole laggard".
$d_{4,\text{ sole-invest}}$	Percentage market share change for sole investor (in Scenario #5.4)	+1.5%	Scenario #5.4 corresponds to 1.5% contestable semiconductor market share and all competition *between* IST and smaller chipmakers. Thus, if exactly one of IST invests, then it is expected to gain the 1.5% contestable market share from the smaller chipmakers. Hence, a +1.5% MS gain for the "sole investor" is expected.
$d_{4,\text{ dual-laggard}}$	Percentage market share change for two lagging firms(in Scenario #5.4)	+0.0% (each)	Scenario #5.4 corresponds to 1.5% contestable semiconductor market share and all competition *between* IST and smaller chipmakers. Thus, if exactly two of IST choose not to invest, then neither of them is expected to lose (or to gain) any of the 1.5% contestable market share. Hence, no MS changes are expected for the "dual laggards".

Model Parameter Symbol	Model Parameter Name	Estimated Parameter Value	Source of Parameter Estimate
$d_{5,j}$ (where j ϵ {all-invest, sole-invest, dual-laggard, dual-invest, sole-laggard})	Percentage market share change for any chipmaker under any set of actions in Scenario #5.5	+ 0.0%	Scenario #5.5 corresponds to an assumption of no market share changes regardless of the investment actions chosen by Intel, Samsung, and TSMC.
$d_{6,j}$ (where j ϵ {all-invest, sole-invest, dual-laggard, dual-invest, sole-laggard})	Percentage market share change for any chipmaker under any set of actions in Scenario #5.6	=1.67* $d_{2,j}$	Scenario #5.6 corresponds to similar assumptions to Scenario #5.2, except that the overall contestable market share is 2.5% (Scenario #5.6) vs. 1.5% (Scenario #5.2). Hence, each percentage market share should be multiplied by 1.67 (=2.5%/1.5%) of the corresponding market share change in Scenario #5.2.
$d_{7,j}$ (where j ϵ {all-invest, sole-invest, dual-laggard, dual-invest, sole-laggard})	Percentage market share change for any chipmaker under any set of actions in Scenario #5.7	=1.67* $d_{3,j}$	Scenario #5.7 corresponds to similar assumptions to Scenario #5.3, except that the overall contestable market share is 2.5% (Scenario #5.7) vs. 1.5% (Scenario #5.3). Hence, each percentage market share should be multiplied by 1.67 (=2.5%/1.5%) of the corresponding market share change in Scenario #5.3.
$d_{8,j}$ (where j ϵ {all-invest, sole-invest, dual-laggard, dual-invest, sole-laggard})	Percentage market share change for any chipmaker under any set of actions in Scenario #5.8	=1.67* $d_{4,j}$	Scenario #5.8 corresponds to similar assumptions to Scenario #5.4, except that the overall contestable market share is 2.5% (Scenario #5.8) vs. 1.5% (Scenario #5.4). Hence, each percentage market share should be multiplied by 1.67 (=2.5%/1.5%) of the corresponding market share change in Scenario #5.4.
$f_{\text{chipmaker profit}}$	Fraction of chipmaker manufacturing cost savings (from the introduction of 450mm technology) which are converted to net Chipmaker profits	50%	Best estimate of author. Clearly, it is reasonable to assume that not all manufacturing cost reductions will go directly to profit for the chipmakers. Various factors including inter-chipmaker competition and taxes will shave away at how 450mm manufacturing cost savings ultimately impact chipmaker profitability. Lacking precise estimates, but knowing that these factors are substantial, I used an estimate of 50%.

Model Parameter Symbol	Model Parameter Name	Estimated Parameter Value	Source of Parameter Estimate
$f_{financing}$ (Not directly used in payoff calculations. However, this value is used indirectly to calculate I_{Intel}, $I_{Samsung}$, and I_{TSMC}.)	Fraction of remaining required financing which the chipmakers must collectively provide to the equipment suppliers in order to entice them to pursue 450mm development as quickly as possible	40%	Best estimate of author. Obviously, the equipment suppliers will continue to bear a significant burden of 450mm R&D costs. However, as many industry commentators have observed, there is expected to be a sharing of R&D costs between equipment suppliers and chipmakers for large technology transitions going forward – for example 450mm wafers and EUVL (e.g., see McGrath 7/11/12 and Lapedus 10/25/10 for expressions of this viewpoint). Previous estimates of chipmaker financing aid to suppliers have typically been less than 40%, often significantly less than 40%. However, since the 450mm wafer-size transition is likely to be considerably more costly and the industry growth is slowing (see Hutcheson 2006 and Hutcheson 2013), it is likely that chipmakers would be expected to invest a sizeable portion of the total 450mm R&D bill in order to entice suppliers to develop the equipment. Hence, I have estimated this fraction at 40%.
$f_{mfg\ savings}$	Fraction of COGS reduction to be expected from 450mm wafer manufacturing	20%	Estimates for cost savings from prior wafer-size transitions range from 20%-30%. Estimates for the 450mm wafer size (over the 300mm wafer size) range from 10% to 30% (e.g., see SEMI 9/1/12, Mack 8/20/12, and McGrath 7/9/12). Selecting a point roughly in middle of this range gives 20% cost savings.

Model Parameter Symbol	Model Parameter Name	Estimated Parameter Value	Source of Parameter Estimate
g_{COGS}	Growth Rate of COGS for each chipmaker assuming that no 450mm technology is developed	0%	Best estimate of the author. This growth rate is very hard to assess. Although the historical 300mm-equivalent wafer start CAGR has been estimated in the range of 10% (see Table 40 in Appendix A), it is not clear how long this growth will persist into the future. For one thing, the fate of EUVL is uncertain, and it has been estimated that the wafer start CAGR could slow to zero growth if no successful alternative lithography technology is developed (see Table 40 in Appendix A). Secondly, as has been noted before the medium-to-long term growth rate of revenues of semiconductors seems to be moderating. Thirdly, it has been speculated that some chipmakers will make the transition to 450mm wafers while other will remain on 300mm or even 200mm wafers. One might well expect that annual COGS could increase in the future, but as discussed in Section 5.6.1 one can cover this eventuality by examining sensitivity analyses for other parameters which increase the overall magnitude of chipmaker benefits from 450mm. Given all of these various pressures on COGS estimates, for simplicity and to ensure some measure in conservatism for the 450mm benefits, the base case assumption is 0% growth on annual COGS is assumed once the benefit to 450mm wafers kicks in (as per Table 13).
I_{Total}	Total 450mm equipment R&D investment ($B USD)	15	Estimates for the total 450mm wafer-size R&D encompass a very wide range ($8B - $40B). For estimates toward the midpoint of this range see Hutcheson 2006 and McGrath 7/11/12. McGrath (7/11/12) relays a mid-range analyst estimate of $17B in R&D expenditures for 450mm and hinted that only a small amount of the spending has been completed by 2011. Thus a total 450mm R&D estimate of $15B was used.
I_{Intel}	450mm equipment R&D investment required by Intel to confer the benefits associated with being an "early investor" in 450mm technology ($B USD)	2.0	Given I_{Total} = $15B and $f_{financing}$ =40% for "full incentivization" of 450mm equipment development by the three largest chipmakers, the symmetric amount for each of the three chipmakers would be $2B =(0.40*$15B)/3. Thus this investment amount estimate was used for each chipmaker in the base case analysis.

Model Parameter Symbol	Model Parameter Name	Estimated Parameter Value	Source of Parameter Estimate
$I_{Samsung}$	450mm equipment R&D investment required by Samsung to confer the benefits associated with being an "early investor" in 450mm technology($B USD)	2.0	Same explanation as above.
I_{TSMC}	450mm equipment R&D investment required by TSMC to confer the benefits associated with being an "early investor" in 450mm technology($B USD)	2.0	Same explanation as above.
m_{Intel}	Net profit margin assumed for Intel for the market share gains/losses	23%	Best estimate of the author. Financial statements were used to calculate the net profit margins (= net income/net sales) for the three chipmakers: Intel, Samsung, and TSMC for the years 2006 through 2010. The averages for those five years were: 18.9% for Intel, 15.0% for Samsung, and 34.5% for TSMC. The average across all three firms was 22.8%. It is difficult to assess how margins may change over time and to predict the profitability of those chip market segments which are likely to be under contest across the chip manufacturers. Due to these uncertainties, the average net margin across the three companies (rounded to 23%) was chosen for all three firms.
$m_{Samsung}$	Net profit margin assumed for Samsung Electronics for the market share gains/losses	23%	Same explanation as above.
m_{TSMC}	Net profit margin assumed for TSMC for the market share gains/losses	23%	Same explanation as above.

Model Parameter Symbol	Model Parameter Name	Estimated Parameter Value	Source of Parameter Estimate
$R_{industry}$	Estimated Total Semiconductor Industry Revenue in 2010 ($B USD)	304	Estimate for overall semiconductor revenue in 2010 is $304B (e.g., see Osborne 12/17/10, Wikipedia "Semiconductor Industry", 1/24/13).
R_{Intel} (Not directly used in payoff calculation. Provided as context for annual COGS amounts)	Approximate semiconductor revenue for Intel Corporation in 2010($B USD)	40.0	iSuppli semiconductor rankings for 2010 (Osborne 12/17/10) estimate Intel's 2010 semiconductor revenue at $40.0B USD.
$R_{Samsung}$ (Not directly used in payoff calculation. Provided as context for annual COGS amounts)	Approximate semiconductor revenue for Samsung Corporation in 2010($B USD)	28.1	iSuppli semiconductor rankings for 2010 (Osborne 12/17/10) estimate Samsung's 2010 semiconductor revenue as $28.1B USD.
R_{TSMC} (Not directly used in payoff calculation. Provided as context for annual COGS amounts)	Approximate semiconductor revenue for TSMC Corporation in 2010($B USD)	25.8	Approximate average exchange rate (www.oanda.com) for calendar year 2010 was 0.03155 NT$ per USD$. TSMC's 2010 annual report (TSMC 2010a) indicates that fiscal year sales were: 406.9B NT$, or approximately $12.9B USD. Since TSMC solely provides chip-manufacturing services, one must inflate its revenue by some factor to make its revenues more comparable to those of the more purely IDM chip manufacturers (especially as of 2010) such as Intel and Samsung. One historical rule of thumb has been to multiply the foundry revenue by a factor of 2.5 to 3 to make it comparable to IDM chip revenues (Siekman 5/14/01). Using a more conservative multiplier of 2.0 leads to an "effective semiconductor revenue" of TSMC of 2.0 ($12.9B) = $25.8B

Model Parameter Symbol	Model Parameter Name	Estimated Parameter Value	Source of Parameter Estimate
t_{ending}	Year up until which cash flow associated with manufacturing cost savings and market share changes were calculated (calendar year)	2031	It is widely agreed that silicon transistors (if not silicon substrates as well) will give way to other materials for chip manufacturing. When and how this transition will occur is a matter of debate. Even when such a transition occurs, it is likely that a large volume of conventional semiconductor devices will continue to be manufactured on silicon (or at least on traditional single element or two element compound semiconductor) substrates. Thus it seems reasonable to assume that the time horizon for manufacturing cost savings due to the 450mm wafer manufacturing platform should extend for many years. The ITRS roadmap extends for 15 years, but one could easily imagine 450mm wafers extending beyond that. Thus, a 20 year time horizon (2011 – 2031) was adopted for the purposes of calculating the manufacturing cost savings and market share impacts due to 450mm wafers. The 450mm benefits here extend beyond those for the EUVL model (Chapter 4) because a wafer-size benefit is more certain to persist far into the future than is a lithography equipment benefit.
$\Delta t_{benefits,all\ invest}$	Length of time between chipmaker investment (t_0=2011) and start of manufacturing cost savings and market share gains for "early investing" firms if all three players invest (years)	5	Historically, there has been a long lead time between investment in a wafer-size transition equipment R&D and accrual of the benefits from this investment. Additionally this length of time has been increasing over the history of the semiconductor industry. Hutcheson (2006) estimates that the duration of transition for the last two wafers sizes was 8-9 years. Because (as of 2011) we are already partially through the transition to 450 mm it is reasonable to assume (for simplification) that the full manufacturing cost savings benefits of the new wafer size would start to accrue to early adopters sooner than that 8-9 years. In the case of investment by all three of IST, I approximate this lag as 5 years. This is also roughly consistent with press announcements by Intel and TSMC regarding their plans for ramping 450mm (Lapedus 1/24/11 and Lapedus 4/6/11) while recalling that manufacturing costs savings will likely not accrue in the first year or two of the manufacturing ramp (recalling Figure 25).

Model Parameter Symbol	Model Parameter Name	Estimated Parameter Value	Source of Parameter Estimate
$\Delta t_{\text{benefits,two investors}}$	Length of time between chipmaker investment (t_0=2011) and start of manufacturing cost savings and market share gains for "early investing" firms if all three players invest (years)	6	Same as above, except in the case of investment by two of the IST chipmakers, I approximate this lag as 6 years (i.e., one year longer than the case where all three chipmakers invest).
$\Delta t_{\text{benefits,one investor}}$	Length of time between chipmaker investment (t_0=2011) and start of manufacturing cost savings and market share gains for "early investing" firms if all three players invest (years)	7	Same as above, except in the case of investment by only one of the IST chipmakers, I approximate this lag as 7 years (i.e., two years longer than the case where all three chipmakers invest).
$\Delta t_{\text{fast followers}}$	Length of time between start of benefits accrued by early adopting firms and manufacturing cost savings and market share losses experienced by fast following firms (years)	0 (for Scenario #5.0) 1 (for Scenarios #5.1 through #5.4) 2 (for Scenarios #5.5 through #5.8)	Different technologies have differing levels of difficulty for fast following. Also, firms have different capabilities for fast following quickly. For example, Samsung is seen by some to be a company which can fast follow particularly well (Section 6.5.1). Although one could model each firm as having a different "fast following" time, for the base case analysis, it is simpler (and more transparent) to assume the same length of fast following lag for each of the firms. Given considerable difficulty of installing and tuning entirely new equipment coupled with annual bucketing of financial benefits of 450mm, the two reasonable possibilities seem to be a one-year lag or a two-year lag for fast following chipmakers. A one-year lag is assumed in Scenarios #5.1 through #5.4. A two-year lag is assumed for Scenarios #5.5 through #5.8. Scenario #5.0 is a reference scenario which assumes no time lag for fast following.

B.5 Example 450mm Payoff Calculations

Let us arbitrarily choose (as an illustrative example) to calculate Samsung's payoff in Scenario #5.4 (see Figure 30) for the ('Invest', 'Invest', 'Invest') state of the world. From Figure 30 we see that Samsung's E(NPV) in this situation is estimated to be $4.8B. We will trace this estimate calculation example all the way from the model parameter values to the payoff estimate.

First, we deduce from Equation (B.9) that:

$$h_{S,t}('Invest','Invest','Invest') = \begin{matrix} 0\ if\ 1 \le t \le 4 \\ 1\ if\ 5 \le t \le 20 \end{matrix} \quad \text{(B.11)}$$

Said more simply, we've shown that Samsung accrues the benefits of 450mm starting in year 5 and keeps them through the horizon of the analysis (i.e., up through t=20).

Then, combining Equations (B.11) and (B.8) and knowing that $f_{\text{mfg savings}}$= 20% and $COGS_{\text{Samsung}}$ = $11.8B, we find that:

$$\Delta C_{S,t,450mm}('Invest','Invest','Invest') = \begin{matrix} 0\ if\ 1 \le t \le 4 \\ \$2.36B\ if\ 5 \le t \le 20 \end{matrix} \quad \text{(B.12)}$$

Knowing that $f_{\text{chipmaker profit}}$= 50%, and plugging Equation (B.12) into Equation (B.3) gives:

$$B_{S,t,mfg\ cost}('Invest','Invest','Invest') = \begin{matrix} 0\ if\ 1 \le t \le 4 \\ \$1.18B\ if\ 5 \le t \le 20 \end{matrix} \quad \text{(B.13)}$$

From Table 48 we find that:

$$d_{4,all-invest} = 0.5\% \quad \text{(B.14)}$$

Then, plugging Equations (B.14) and (B.11) into Equation (B.10) yields:

$$\Delta MS_{i,t,450mm}('Invest','Invest','Invest') = \begin{matrix} 0\ if\ 1 \le t \le 4 \\ 0.005\ if\ 5 \le t \le 20 \end{matrix} \quad \text{(B.15)}$$

Knowing that $m_{Samsung}$= 23% and $m_{Samsung}$= 23% and plugging Equation (B.15) into Equation (B.4) gives:

$$B_{S,t,market\ share}('Invest','Invest','Invest') = \begin{matrix} 0\ if\ 1 \le t \le 4 \\ \$0.350B\ if\ 5 \le t \le 20 \end{matrix} \quad \text{(B.16)}$$

Hence, knowing that $I_{S,0}$= \$2.0B and δ = 0.893 (from Table 48) and plugging Equation (B.13) and (B.16) into Equation (B.2) results in:

$$\begin{aligned} \pi_{S,0}('Invest','Invest','Invest') &= \sum_{t=5}^{20}[0.893^t(\$1.18B + \$0.350B)] - \$2.0B \\ &= \left(\frac{0.893^5 - 0.893^{21}}{1 - 0.893}\right)(\$1.53B) - \$2.0B \\ &= \$4.8B \end{aligned} \quad \text{(B.17)}$$

Thus, we have completed the full calculation and retrieved the relevant payoff estimate given the player, scenario, and player actions chosen. Any other payoff estimates in Figure 26 through Figure ***34*** can be recovered in a like manner.

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