6.012   Microelectronic Devices and Circuits   Fall 2002

Design Problem #1 -Digital Circuits
Assigned: October 18, 2002
Due: November 1, 2002 at recitation

Reading Assignment: Chapter 5 and Section 13.5.3 of Howe & Sodini

PLEASE WRITE YOUR RECITATION SESSION TIME ON YOUR PROJECT REPORT

Objective of Project
The goal of this project is to design a section of a CMOS Integrated Row Driver for a new display technology for Electronic Book (eBook) or Portable Digital Assistant (PDA) applications. The circuit you are designing is a buffer that drives a large capacitive load.

Background
In active-matrix addressing, row drivers apply pulses to the row (gate) lines of the switch transistors to select rows sequentially, one at a time from top to bottom. While data voltages (corresponding to the pixel image and gray scale) are presented to the column (data) lines, application of a voltage to the row (gate) lines turns on the pixel transistors that charge the liquid crystal (capacitor) to the data voltage.

The Buffer Circuit you are to implement has to meet a number of delay specifications, however, you will also like to minimize power dissipation and the chip area. Specifically, you are required to implement a CMOS based circuit that minimizes the power consumed and the chip area. Your management would like to know this information by November 1, 2002 so that a product announcement could be made a later date.

There are two approaches you are to explore. You are to make a recommendation to the design team about which of the two approaches to use in the Row Driver Chip.

Approach 1: The first approach uses a string of N-inverters (N is even), starting with a minimum size inverter but the device with of subsequent stages scaled up with respect to the previous stage by a factor of e (e ≈ 2.718) until the final stage, which then drives the large capacitive load. Your goal will be to determine N such that the average propagation delays specification is met. You are also to calculate the power dissipation and the chip area. {See Figure 1}

Approach 2: The second approach uses two stages of inverters with a 1:1 ratio between the NMOS and PMOS device widths, with the objective of minimizing the area. However, this leads to differences in the propagation delay high-to-low and propagation delay low-to-high. This novel buffer balances the two propagation delays by charging the capacitive load using an additional NMOS pull-up whose source is tied to the capacitive load. A constraint that is placed

on your design is that the maximum ratio of the device widths of the second inverter to the device width of the first inverter is 4:1{See Figure 2}.
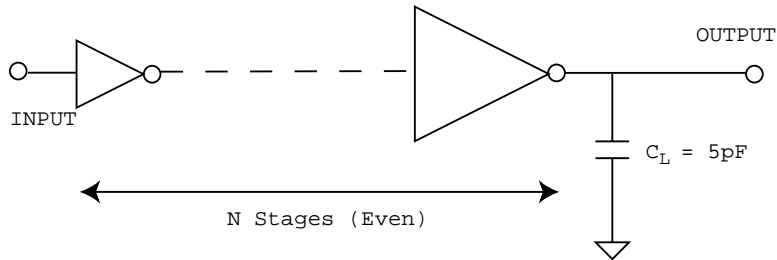
Figure 1: Scaled Inverter Chain.
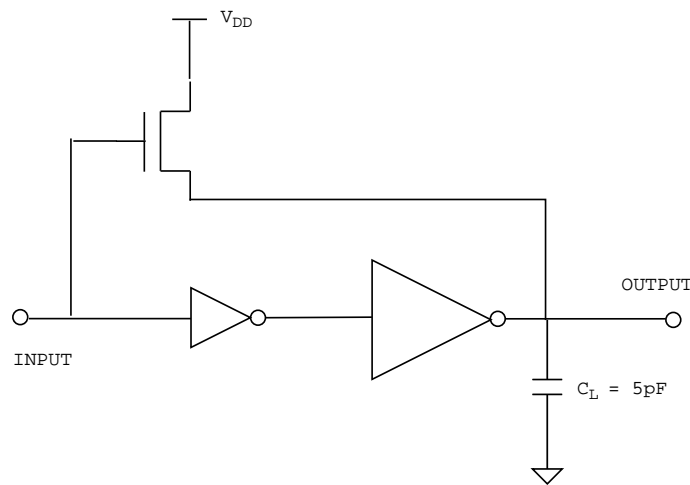
Figure 2: Circuit for Design Problem: NMOS Pull-UP Buffer Circuit

Specifications
The design goal is to achieve symmetrical propagation delays of $t_{PHL} = t_{PLH} = 1.5$ ns. Transistor specifications and SPICE models are given below. The minimum dimensions for transistors are W=12 μm and L=1.5 μm. The parameter LAMBDA must be changed according to the transistor length. The numbers given in the table are for the minimum size transistor that has a gate length of 1.5 μm.

	Devices		Units
	NMOS	PMOS	
VTO	0.77	-0.66	V
GAMMA	0.480	0.42	$V^{1/2}$
TOX	5E-08	5E-08	m
KP	86E-06	26E-06	A/V^2
LAMDA	8E-02	0.13	V^{-1}
PHI	0.74	0.77	V
CJ	5.7E-04	3.9E-04	F/m^2
MJ	0.5	0.5	
CJSW	1.5E-10	1.2E-10	F/m
MJSW	0.33	0.33	
CGSO	4.1E-10	5.6E-10	F/m
CGDO	4.1E-10	5.6E-10	F/m
PB	0.79	0.87	V

**Table 1:** Model Parameters of all available devices.

Device Models

CMOS devices available in this process run at a supply voltage of 5 V. The model parameters for minimum-size transistors are listed in Table I. All minimum size transistors have dimensions: L_n= 1.5 μm, W_n = 12 μm, L_p = 1.5 μm, W_p = 12 μm. For all transistors, L_{diff} = 6 μm (read Section 4.6 of Howe & Sodini to see how transistor capacitances scale with geometry).

Design Objectives

The design goals in order of importance are: (1) to perform the correct logical function, (2) to meet timing constraints, (3) to minimize power dissipation, (4) to minimize total area used.

- The delay between the rising edge of INPUT and OUTPUT reaching the 50% point of its final value must be less than 1.5 ns (t_{PLH} and t_{PHL} < 1.5 ns).

- All logic gates within your circuit must have noise margins of at least 1.5 V.

- Your circuit model and simulation results must reflect the effects of parasitic capacitances. You need to provide SPICE with information that allows it to calculate parasitic capacitances, as described in the following section.

- Average power dissipation when the standard input waveforms are applied must be minimized.
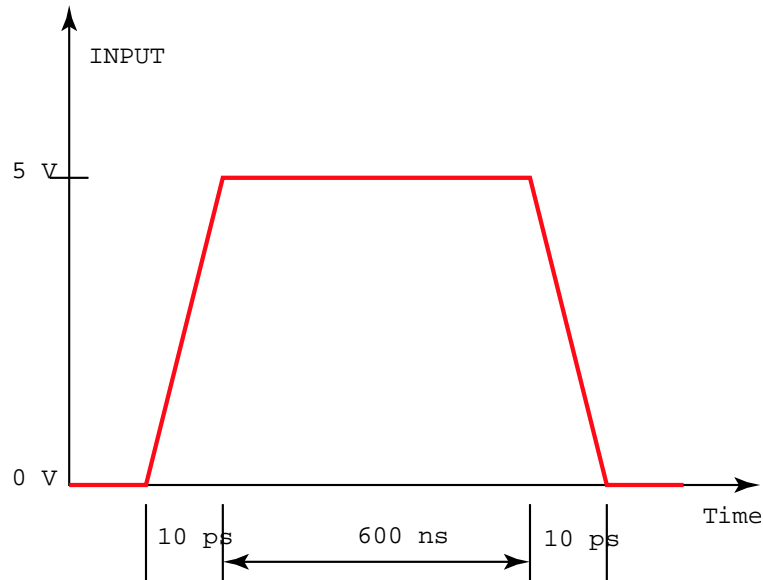
Figure 3: Input Waveforms
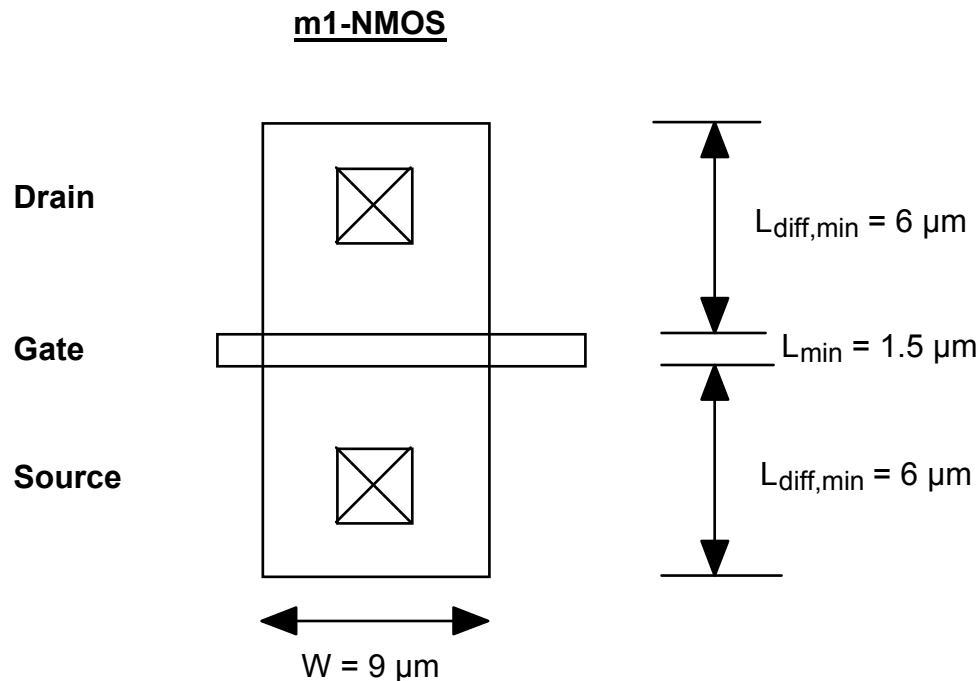
Design Approach

The suggested procedure for design of the buffer circuit is outlined below

- Determine the Sizes of the Output transistors that will meet the propagation delay goals
- Determine the values of t_{PLH} and t_{PHL}
- Determine the value of N (for the first approach) or the size of the NMOS pull-up transistor that meet symmetrical propagation delay goals (for the second approach)
- Determine the power dissipation
- Determine the circuit area
- Optimize for minimum power disspation and minimum circuit area while meeting the power delay goals.

Preliminary Design and Calculations

This section describes simple models for gate, drain, and source capacitances. Estimating these capacitances requires understanding the layout of the transistor including the areas that the source and drain occupy.

Gate capacitance is dominated by the capacitance between the gate and the channel. As the gate voltage changes from HIGH to LOW, the transistor goes through all three regions of operations and exact computation of gate capacitance is difficult. For hand calculations, use the worst-case value of C_G (fF)= C_{ox} (fF/m^2) * W (m) * L (m).

m1-NMOS

Drain

Gate

Source

$L_{diff,min}$ = 6 μm

L_{min} = 1.5 μm

$L_{diff,min}$ = 6 μm

W = 9 μm

Figure 4: Example of transistor layout

Drain and source capacitances arise from the pn-junctions between the source/drain regions and the substrate. This junction should always be reverse-biased, so we only need to worry about depletion capacitance. In a modern IC process, the properties of the junction between the bottom of the drain/source area and the substrate is considerably different from the junction around its perimeter. For this reason, SPICE has two capacitance parameters, CJ and CJSW. CJ is the pn-junction capacitance per unit area of the bottom of the source or drain region (units = F/m^2). CJSW is the capacitance of the "sidewall," or perimeter, of the drain or source region (units = F/m). For hand-calculation, assume that these capacitances are linear and independent of bias voltage.

You must hand calculate the parasitic drain-substrate and source-substrate capacitances for each transistor, as they have a significant effect on the speed of, and power consumed by, your circuit. As an example, we will find the source and drain capacitances for the transistor illustrated above.

The outside perimeter of the drain is W + 2*L $_{diff, min}$ = 6 + 9 + 6 μm = 21 μm. Note that the gate side of the drain is not included. The drain area is W * $L_{diff, min}$ = 9 μm * 6 μm = 54 $μm^2$ = 54*10^{-12} m^2. The perimeter and area of the source are identical to those of the drain.

The SPICE model for this transistor is:
```
m1 1 2 3 4 N1 L=1.5u W=9u pd=21u ps=21u ad=54p as=54p
```

For the drain, 21 μm * CJSW + 54 $μm^2$ * CJ = 10.5 + 5.5 fF = 16 fF. The source has the same dimensions, thus the same capacitance.

HSPICE Simulation

You will need to do two different kinds of simulations: DC sweeps and transients. The DC sweep is used to find the transfer functions of various stages. The easiest way to run DC sweeps is to create an HSPICE deck that contains transistor models, the sub-circuit under test, and simulation commands. *Awaves* can plot the input voltage on the x-axis, and the output voltage on the y-axis.

Use a transient simulation to measure propagation delays. The delay times for CMOS logic circuits are defined as the period from one signal crossing $V_{DD}/2$ to a second signal crossing $V_{DD}/2$.

HSPICE has a convenient command to measure the average power dissipation of a circuit during a specified time interval.

```
.measure tran pdiss avg power from=0n to=100n
```

This command will cause a line like the one below to appear in the HSPICE output file:

```
pdiss = 9.6116E-03 from= 0.0000E-00 to= 1.000E-07.
```

Report

The deliverables of this design problem are as follows.

[20 points] *Answer sheet with summary of results*. This sheet should show the location of all inverters, the size of all transistors and the voltage at which the inverters operate. It should also show the results of your hand calculations, and the results of SPICE simulations for the specifications listed above. You can use the sheet at the end of this handout for this purpose.

[70 points]   A *technical report* with the following parts:
<u>Summary of hand calculations</u>
Here you should show a schematic diagram of your design. Then you should show calculations of the current driving capability of each inverter, the input capacitance presented by each inverter, the dynamic power required in driving each stage, the delays through every inverter, and the noise margins at the inverter driving the laod. In this part of the report, you should indicate the selected transistor dimensions and operating voltages for each inverter. Show how you arrived at your values of N for the inverter chain, and the size of each transistor including the NMOS Pull-up transistor. Show approximate calculations for the expected propagation delays t_{PHL} and t_{PLH}, and for power dissipation for the standard input waveforms. What part(s) of the circuit dissipate the most power?

Identify the logic gate with the smallest noise margin (either V_{NMH} or V_{NML}). Mark this gate on your schematic diagram. Submit a plot from Awaves of its DC voltage transfer curve. If multiple gates have the smallest noise margin, for example two identical inverters identify all of them but submit only one plot.

HSPICE scripts
You should turn in a printout of your HSPICE scripts. These scripts should be placed in your Athena Public directory for our examination. Make sure to give us your username and the complete path to these scripts in the summary page so that we can run them.

SPICE printouts
You should include a printout showing the transfer characteristics of the first inverter at the end of the wire with an extraction of the noise margins. You should also include printouts of the waveforms **INPUT** and **OUTPUT**. These printouts should show the propagation delays from **INPUT** to **OUTPUT**. Also, include the portion of the output file that shows the simulated power dissipation.

[10 points] A *one-page design review abstract*. This is an abstract summarizing your project for a design review meeting. This abstract should concisely state the nature of the problem, the key design issues and trade-offs involved, your design strategy arguing why it is a good one, and the key results. It should bring up to speed other designers that will attend the design review. Your design (as well as others for other parts of the chip) will be presented at this review. The design team will be making a decision about which Buffer Circuit to use in the Display Driver Chip based on your presentation.

Miscellaneous

You are encouraged to work on this design problem with a partner. However, both members of the team must have carried out all aspects of the design problem. It is not allowed to break the design problem into two pieces and have each partner carry out only one of these pieces. Each individual must also turn in a complete set of deliverables as outlined above. The partner's name should be identified in the answer sheet.

The deadline for this assignment is firm. We will not accept late submissions.

Use HSPICE on Athena. Specify LEVEL=1. Refer to the accompanying manual for help on how to get started in HSPICE. Use 25 °C as temperature in SPICE.

You should start this assignment early. There are many aspects to this design problem that will require sustained attention on your part for a substantial amount of time. There is also a learning curve associated with SPICE. This assignment cannot be done at the last minute!

Ask us plenty of questions. While every effort has been made for the specs to be reasonable and for the design project to be well described, there might be residual ambiguities. The first line of advice is the TA's. After that, don't hesitate to approach the recitation instructors and the lecturer.

Design Problem #1 -Digital Circuits
Fall 2002

Name(s):_____

Athena username(s):_____

HSPICE input filename(s):_____

Inverter Chain Design

SPECIFICATION	YOUR DESIGN
N (number of inverters at output stage)	

PARAMETER	SPECIFICATION	CALCULATED VALUE	SIMULATED VALUE
Average Power Dissipation.	Not specified		
Chip Area	Not Specified		

NMOS Pull-up Buffer Design

PARAMETER	SPECIFICATION	CALCULATED VALUE	SIMULATED VALUE
t_{PHL}	< 1.5 ns		
t_{PLH}	< 1.5 ns		
Minimum Noise Margin	> 1.5 Volt		
Average Power Dissipation.	Not specified		
Chip Area	Not Specified		