Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science

6.002 – Circuits & Electronics
Fall 2006

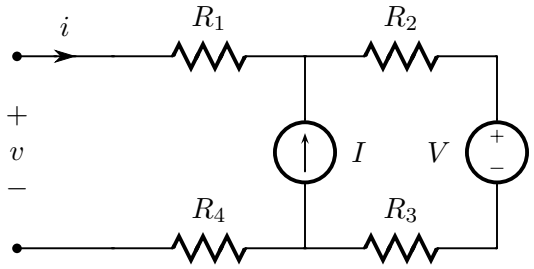
Problem Set #3

Issued 9/22/06 – Due 9/29/06

Projected reading for 9/26 – 9/29 from A&L: Sec 2.6, Ch 6, Sec 6.9 & Ch 7, Sec 6.9 & Ch 7.

Exercise 3.1 (0.5 Point): A car battery is measured to have an open-circuit voltage of 12 V, and a short circuit current of 200 A. What are its Thevenin and Norton equivalents? What is the maximum power that this battery can deliver to a resistive load? What is the voltage across the load, and the current into it, during maximum power delivery?

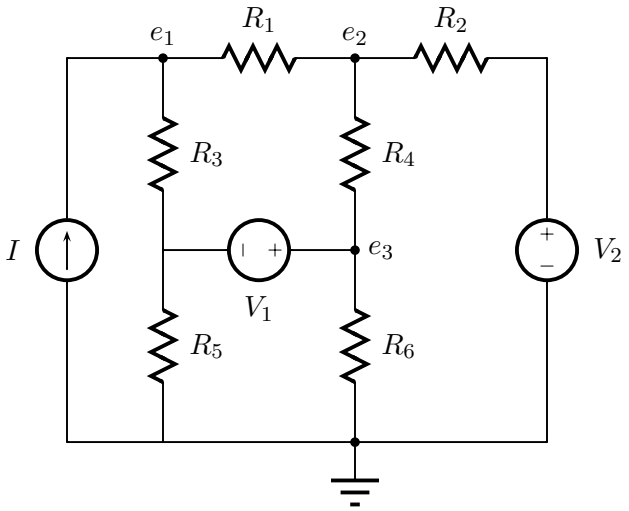
Exercise 3.2 (0.5 Point): Find the Thevenin and Norton equivalent of the following network.



Exercise 3.3 (1 Point): Using the node method, develop a set of simultaneous equations for the network shown below that can be used to solve for the three unknown node voltages in the network. Express these equations in the form

$$G \begin{bmatrix} e_1 \\ e_2 \\ e_3 \end{bmatrix} = S$$

where G is a 3×3 matrix of conductance terms and S is a 3×1 vector of terms involving the sources. You need not solve the set of equations for the node voltages.



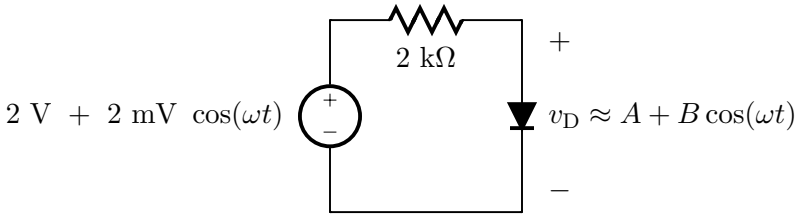
Problem 3.1 (2 Points): This problem is a continuation of Problem 1.4. In answering this problem, you may use again the diode data you measured with WebLab for Problem 1.4, or you may measure the data again.

(A) A real diode often behaves like the theoretical diode described in Problem 1.4 in series with a linear resistor. The linear resistor is a parasitic resistor, and results from the resistance of the silicon that surrounds the diode. This resistance has a noticeable affect on the terminal relation of the diode only for the most positive values of $V_{\rm D}$ and $i_{\rm D}$. Explain why this is the case, and describe how this explains any discrepancies observed in Part (C) of Problem 1.4. Also, using the measured data, determine the series resistance of the real diode.

(B) The real diode is connected to a Thevenin equivalent network as show below. In this case, $v_{\rm D}$ will take the form

$$v_{\rm D} \approx A + B\cos(\omega t)\ ,$$

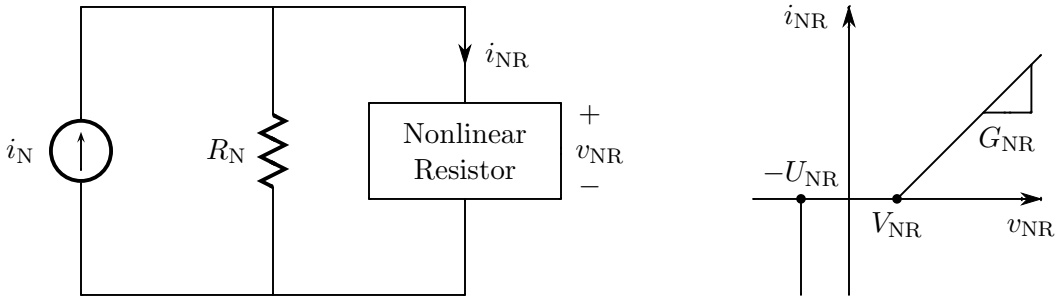
which is a linearized approximation. First, using graphical or numerical analysis, determine A; A is the large-signal value of $v_{\rm D}$ that occurs when the Thevenin voltage is 2 V, that is, when the small-signal voltage 2 mV $\times$ $\cos(\omega t)$ vanishes. Second, using a linearized small-signal analysis, determine B; B is the amplitude of the small-signal component of the linearized $v_{\rm D}$ that is driven by the small-signal cosinusoidal component of the Thevenin voltage. In doing so, linearize the measured diode data, either graphically or numerically, as opposed to the theoretical diode characteristic discussed in (A) above.



The following hints may help answer the questions posed above.

- You may find it instructive to examine the measured data visually with WebLab using using a linear y-axis display.
- As was the case for Problem 1.4, both questions posed above can be answered either graphically or numerically. If you choose a graphical method, then you should plot the downloaded data using MatLab, Excel or another program, or print a screen-shot of the graph produced by WebLab. Capturing screen-shots is a platform specific activity; consult the WebLab documentation for Windows- and Athena-specific advice. If you choose a numerical method, then you should process the downloaded data using MatLab, Excel or another program.

Problem 3.2 (2 Points): A Norton equivalent network is used to excite a nonlinear resistor as shown below. The graphical i-v characteristic that defines the nonlinear resistor is also shown below. Determine the terminal current i_{NR} and the terminal voltage v_{NR} of the nonlinear resistor for all values of i_{N}. Assume U_{NR} and V_{NR} are both positive voltages. Hint: consider using a load-line analysis to gain insight.



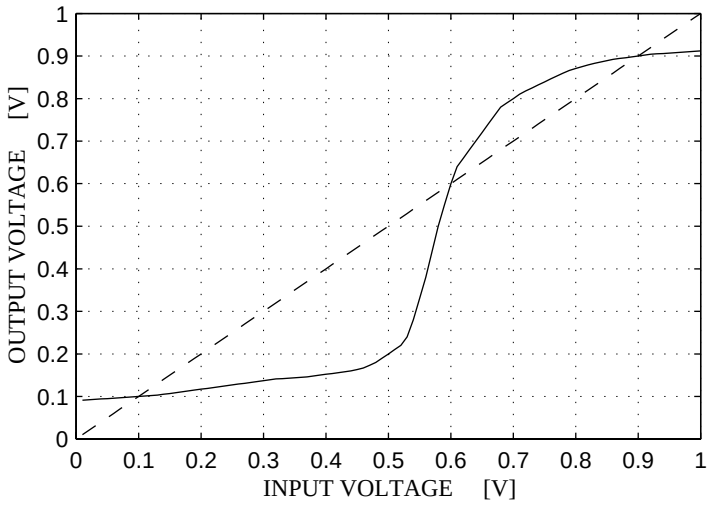
Problem 3.3: Consider the Boolean-logic buffer having the input-output behavior shown below; the dashed diagonal is for reference. *(A larger copy of the graph, which may be turned in with your solutions if you wish, is printed on the last page.)* The usual static discipline is to be defined for this buffer such that $V_{\mathrm{OL}} < V_{\mathrm{IL}} < V_{\mathrm{IH}} < V_{\mathrm{OH}}$. The high-level noise margin for this static discipline is $V_{\mathrm{OH}} - V_{\mathrm{IH}}$. The low-level noise margin for this static discipline is $V_{\mathrm{IL}} - V_{\mathrm{OL}}$.

(A) If zero noise margin were acceptable, over what voltage range could V_{IL} be chosen? What is the corresponding voltage range of V_{OL}?

(B) What combination of V_{IL} and V_{OL} maximizes the low-level noise margin?

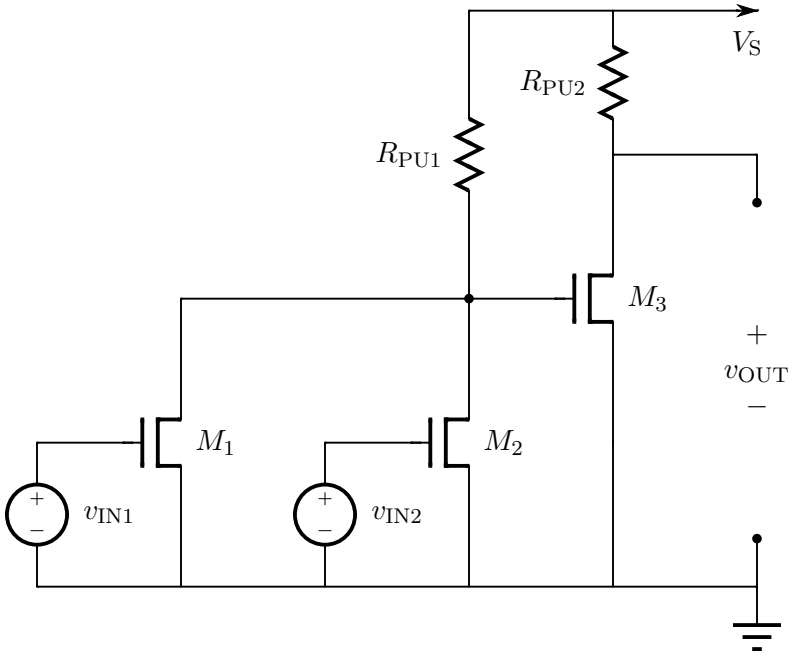
(C) If zero noise margin were acceptable, over what voltage range could V_{IH} be chosen? What is the corresponding voltage range of V_{OH}?

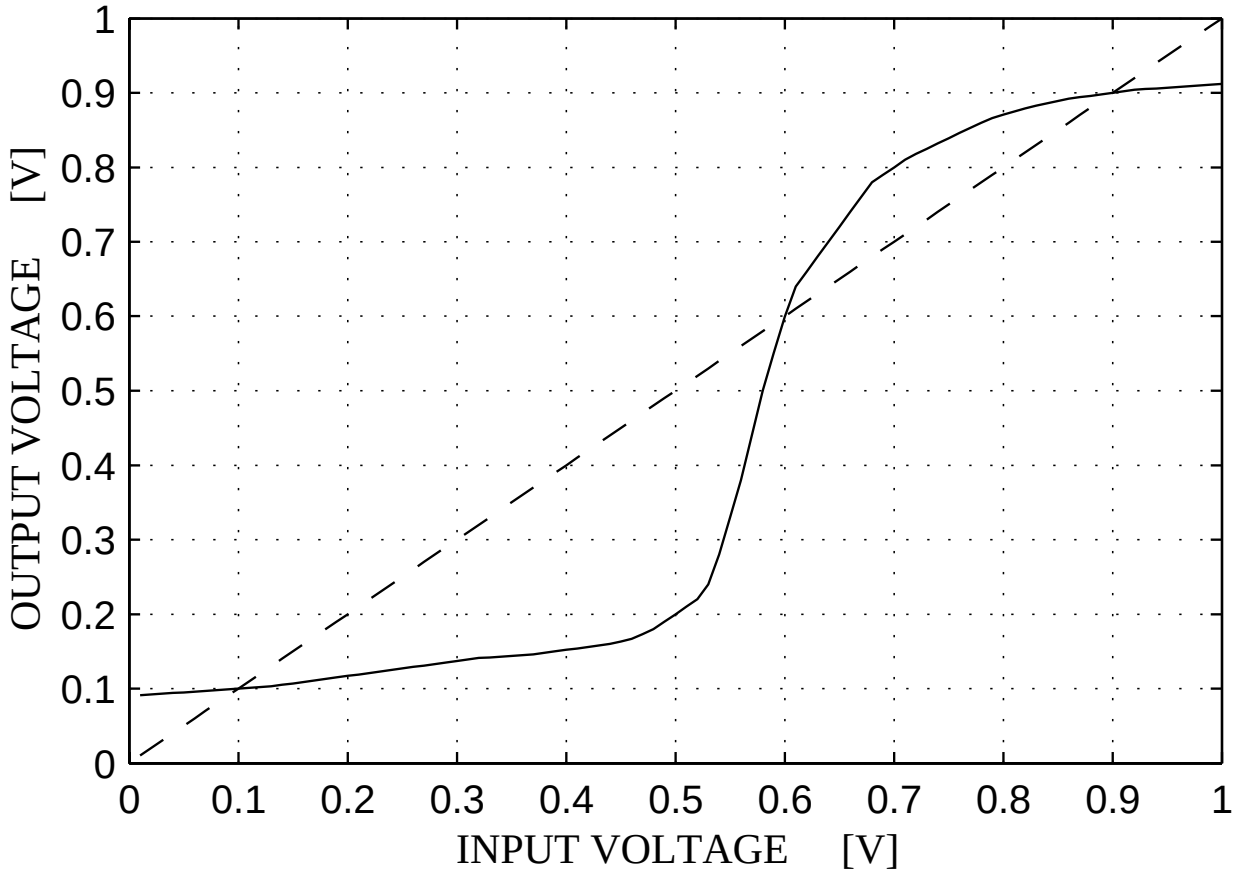
(D) What combination of V_{IH} and V_{OH} maximizes the high-level noise margin?



Problem 3.4: Consider the NMOS two-input OR gate shown below. This gate is to be implemented with MOSFETs having 0.5 V $\leq V_{\rm T} \leq$ 3 V and $10^3\ \Omega \leq R_{\rm ON} \leq 10^5\ \Omega$, and pull-up resistors having $10^3\ \Omega \leq R_{\rm PU} \leq 10^5\ \Omega$. (The inequalities express a permissible design space as opposed to a range of manufacturing uncertainty.) The MOSFETs and pull-up resistors need not have identical parameters.

Complete the design of the OR gate by choosing values for each $V_{\rm T}$, $R_{\rm ON}$ and $R_{\rm PU}$ so that: $V_{\rm OL} = 0.5$ V; $V_{\rm IL} = 1.5$ V; $V_{\rm IH} = 2$ V; $V_{\rm OH} = 3$ V; and the power dissipated by the gate is minimized. If any parameter does not have a unique design value, then give the permissible range for that parameter. Assume $V_{\rm S} = 3.5$V.




OUTPUT VOLTAGE [V]
INPUT VOLTAGE [V]
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1