Device Characterization and Circuit Design Project Solutions

1 Characterization

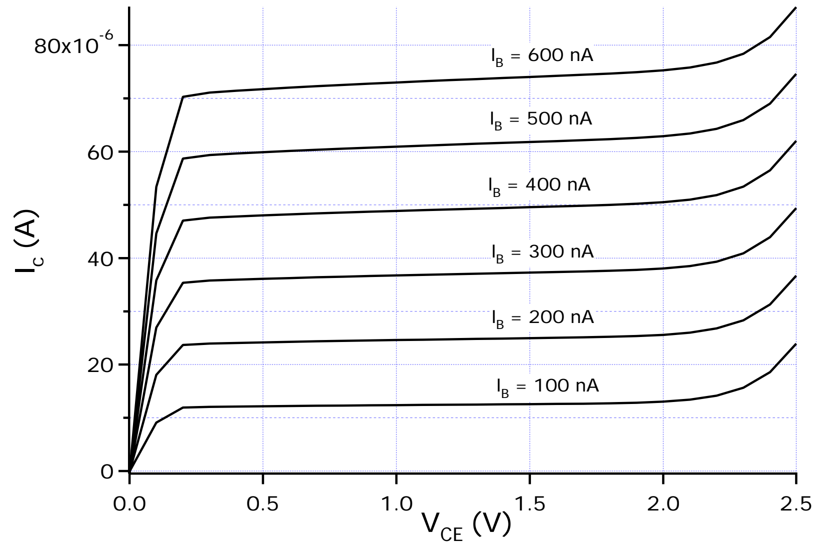

Figure 1: Graph 1

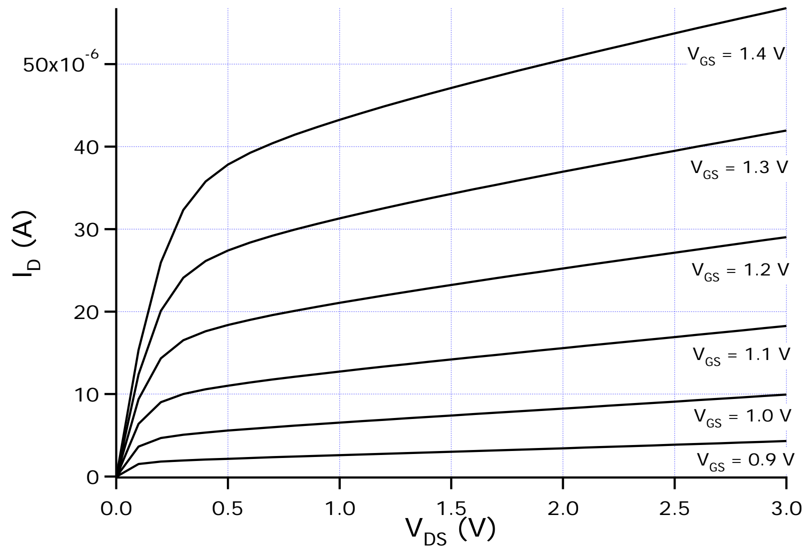

Figure 2: Graph 2

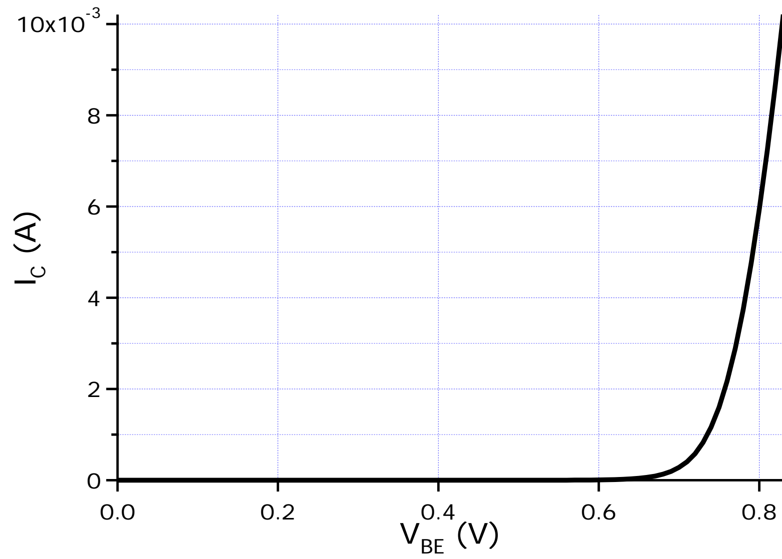

Figure 3: Graph 3

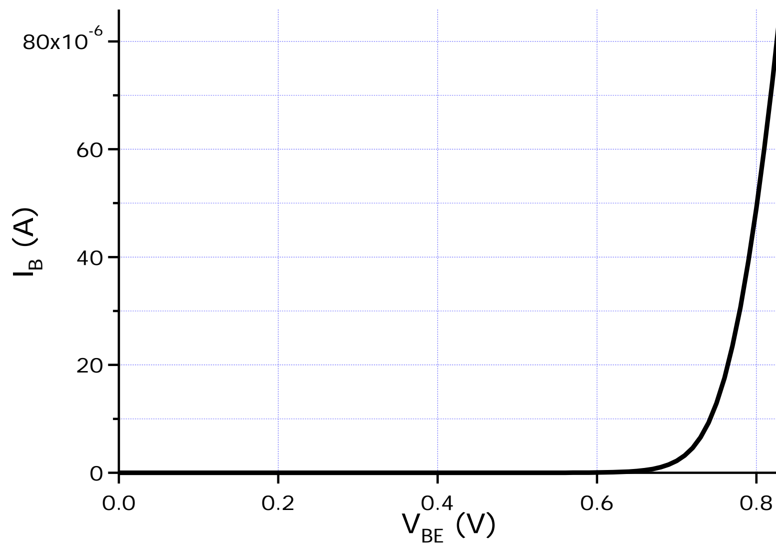

Figure 4: Graph 4

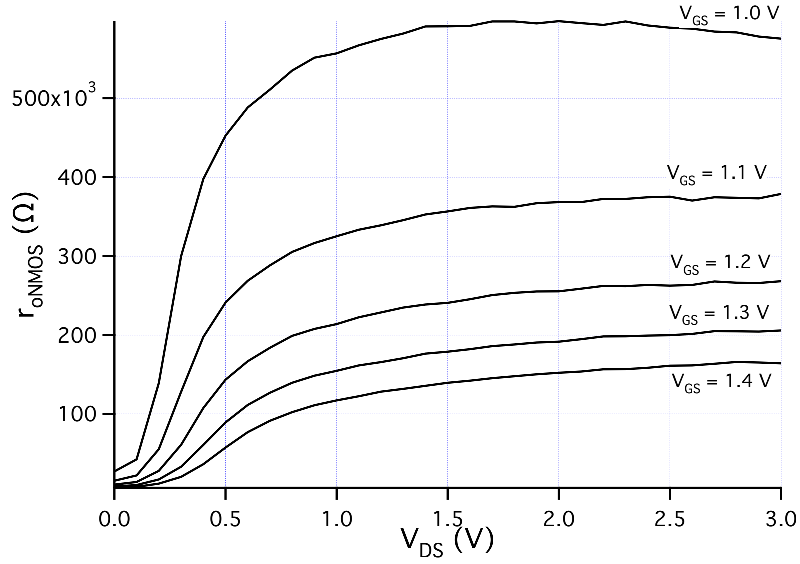

Figure 5: Graph 5

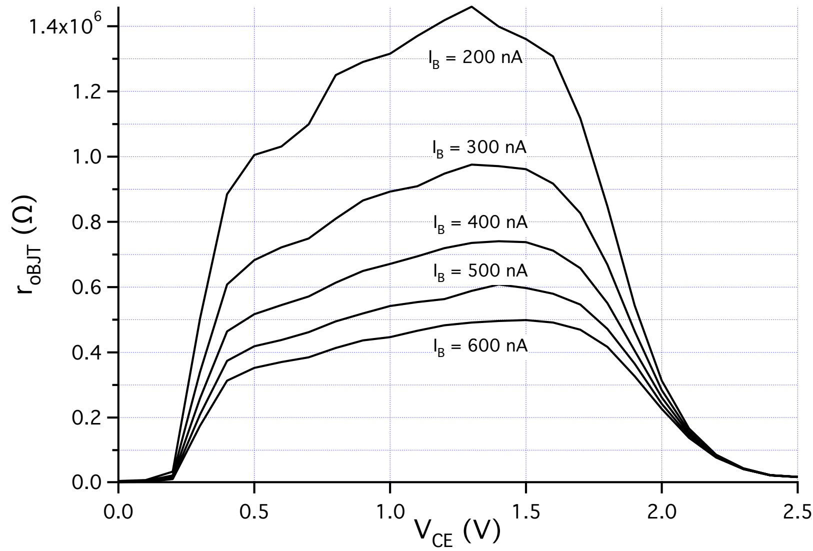

Figure 6: Graph 6

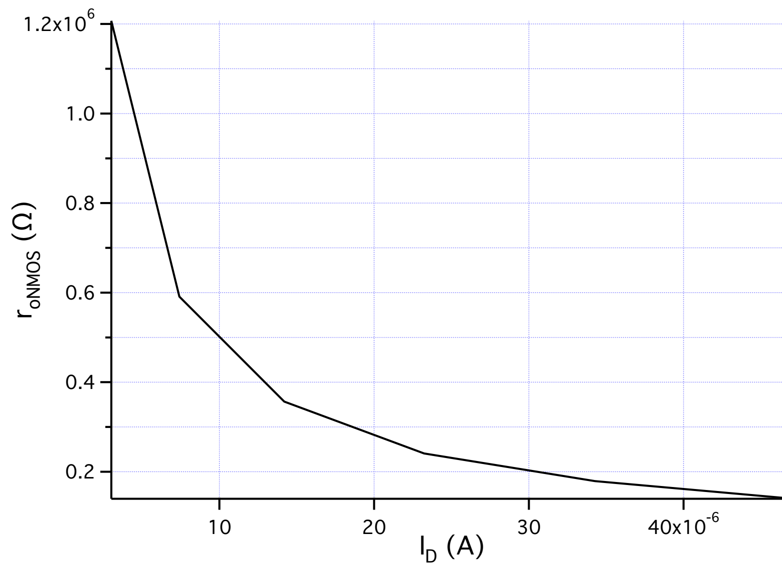

Figure 7: Graph 7

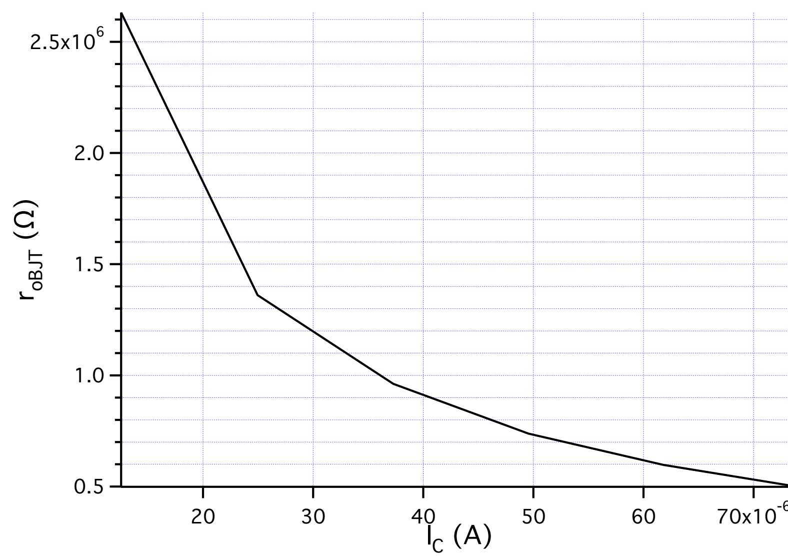

Figure 8: Graph 8

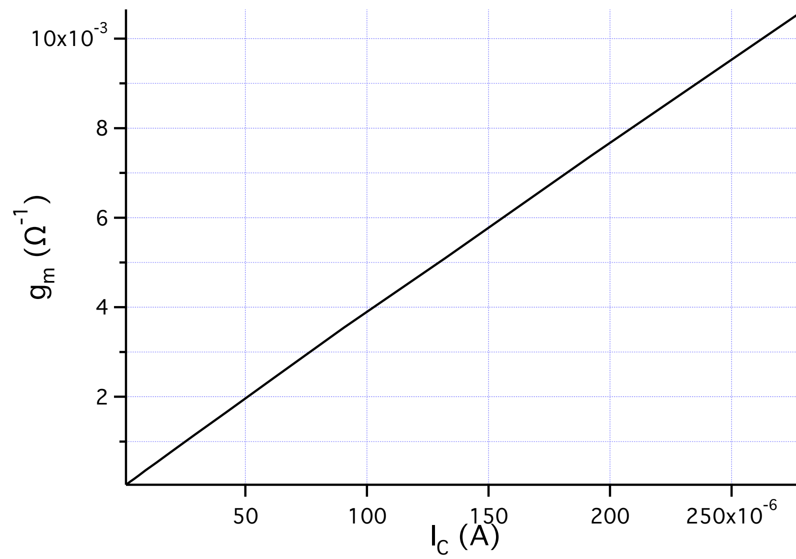

Figure 9: Graph 9

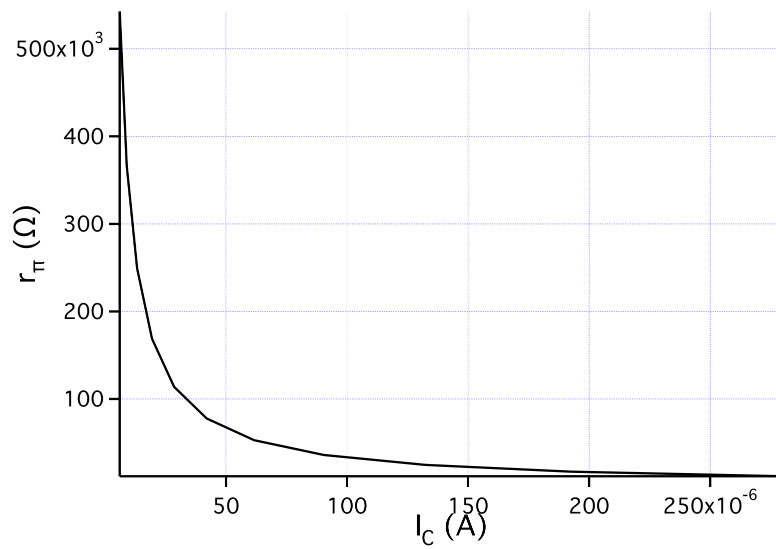

Figure 10: Graph 10

2 Amplifier Design (*50 points total*)

1. (Small Signal - *30 points*)

   To solve for the three parameters (gain, input resistance, output resistance), draw the small signal model and apply test voltages or currents, using KCL at the output (emitter) node.

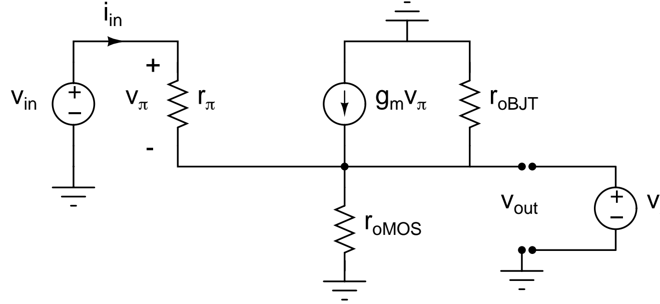

Figure 11: Small signal model of the amplifier. The n-MOSFET reduces to a transistor output resistance. The source v_x is attached to measure output resistance.

Gain:

$$\frac{v_{in} - v_{out}}{r_\pi} - \frac{v_{out}}{r_{oMOS}} - \frac{v_{out}}{r_{oBJT}} + g_m(v_{in} - v_{out}) = 0$$

$$v_{in}(g_m + \frac{1}{r_\pi}) = v_{out}(\frac{1}{r_\pi} + \frac{1}{r_{oMOS}||r_{oBJT}} + g_m)$$

$$\mathbf{A_v = \frac{1}{1 + \frac{r_\pi}{(g_m r_\pi + 1) r_{oMOS}||r_{oBJT}}}} \tag{1}$$

Input Resistance:

$$v_{in} = i_{in} r_\pi + i_{in}(r_{oMOS}||r_{oBJT}) + g_m i_{in} r_\pi (r_{oMOS}||r_{oBJT})$$

$$\mathbf{R_{in} = r_\pi + (g_m r_\pi + 1) r_{oMOS}||r_{oBJT} \approx g_m r_\pi (r_{oNMOS}||r_{oBJT})} \tag{2}$$

Ouput Resistance:

$$i_x = \frac{v_x}{r_\pi} + \frac{v_x}{r_{oMOS}||r_{oBJT}} + g_m v_x$$

$$\mathbf{R_{out} = r_{oMOS}||r_{oBJT}||r_\pi||\frac{1}{g_m} \approx \frac{1}{g_m}} \tag{3}$$

Range of bias current:

The lower limit of current is set by the output resistance specification. For $R_{out} < 1000\ \Omega$, we require $g_{mBJT} > 0.001$. Solving the formula for g_m assuming room temperature provides an approximate value. For a more accurate result, consult Graph 9 for actual g_m vs. I_C data. This gives an answer $\mathbf{I_C > 28\ \mu A}$.

The upper limit is set by the input resistance or gain, whichever is the stricter specification. The gain spec was set to be quite loose at $V_{OUT} = 1.5$V but relatively strict at the swing endpoints. It is the input resistance specification that sets the high current limit. Intuitively, one can consider that r_π, r_{oMOS}, and r_{oBJT} are all inversely proportional to I_C, such that the factor in the denominator of the A_v expression should not change to first order with increasing current assuming that both transistors remain in their constant current regimes. The input resistance however depends on the factor $g_m r_\pi = \beta$ would does not change with I_C to first order, and the output resistances of the transistors which do vary inversely with I_C. From the data in Graphs 7 and 8, we see that the output resistances remain high ($> 15\ k\Omega$) for $I_D = I_C < 400\ \mu$A. The limiting factor is the MOSFET that eventually solidly enters its linear (low resistance) regime with increasing bias current. For $I_D \approx 500\ \mu$A, $\beta \approx 100$. Therefore we are looking for the point where $r_{oMOS} \approx 10\ k\Omega$. This occurs for a current of about 470 μA. However, $V_{GS} = 3.3$V is required to reach that current, so realistically the highest current that would be used is approximately 440 μA, corresponding to $V_{GS} = 3$V (both answers are considered correct).

$$\mathbf{28\ \mu A < I_C < 440\ \mu A}$$

2. (Bias point selectrion - *20 points*)

The gain specification was set relatively low because of the wide swing that was required.

At the low swing ($V_{CE} = 2.5$ V), the I_C of the BJT starts rising very quickly. The output resistance of the BJT thus becomes relatively very low at that point, independent of bias current. Additionally, as the bias current is raised (to lower r_π), the mosfet starts to enter the linear region resulting in a lower output resistance for that device. It is a combination of those two effects that limit the swing towards the bottom rail and that limit the bias current.

At the high swing, we are limited by the BJT entering saturation ($V_{CE} < V_{CEsat} \approx 0.2$ V).

The specs can be easily met with a current in the $I_C = I_D = 25-60\ \mu A$ range. As an example, consider $I_C = 40\ \mu A$. From Graphs 2 and 3, this implies $V_{GS} = 1.35V$, $V_{BE} = 0.65$V. Therefore, the bias voltages are $V_B = 1.35$ V and $V_{BIAS} = 0.65 + 1.5 = 2.15$ V.

Using Graphs 5-10, we extract all important values and calculate the specifications as shown in the following table.

	$V_{OUT} = 1.5$ V	$V_{OUT} = 0.5$ V	$V_{OUT} = 2.5$ V	Spec.
r_π (Ω)	77830	77830	77830	
g_m (Ω^{-1})	0.00165	0.00165	0.00165	
r_{oBJT} (Ω)	950k	18k	520k	
r_{oNMOS} (Ω)	160k	57.5k	161k	
A_v	0.996	0.956	0.994	> 0.950
R_{IN} (Ω)	18M	1.7M	15M	> 1M
R_{OUT} (Ω)	606	606	606	< 1000