Homework #7 - November 12, 1998

Due: November 19, 1998 at lecture

1. (60 points) **MOSFET characterization**. In this problem, you are going to measure and characterize an integrated n-channel MOSFET. Access to this MOSFET is provided through our experimental *Web-based Microelectronics Device Characterization Set-up*. Lane Brooks has just released a second version of the software for this problem. This new release has hopefully solved most of the bugs that were reported with the first version and has added a number of new and handy features. An updated manual is enclosed. It is also available on line.

In this problem, an nMOSFET is to be characterized. This is an integrated device. The details of the connections are available on line. You have to exercise care with this device. You should measure the specified characteristics. Once satisfied with the look of the data on the HP4155 interface, you should download the data set for graphing and further analysis. It will be to your advantage to make good use of the *Set-up* and *User-defined* functions that Lane has built.

For all the following measurements, hold V_{GS} between 0 and 2.5 V and V_{DS} between 0 and 4 V. Unless specified, the back bias should be $V_{BS} = 0$ V. When relevant, examine V_{BS} between 0 and -2.5 V. Here is your assignment:

1. Measure and download the *output characteristics*, that is, I_D vs. V_{DS} with V_{GS} as parameter. In the HP4155, program also the output conductance g_d. Download it too.

   In your local machine and using your preferred software tool, graph the output characteristics (**graph 1**, linear scales) and the output conductance (g_d vs. V_{DS} with V_{GS} as parameter, **graph 2**, linear scales). From the output characteristics, extract V_{DSsat}. Describe your algorithm. Graph V_{DSsat} vs. V_{GS} (**graph 3**, linear scales). Overlap in this graph, the ideal behavior of V_{DSsat} given in class ($V_{DSsat} = V_{GS} - VT$). Comment on differences. From the output conductance data extract the *Early voltage*. Show how you did this (**graph 4**, linear scales).

2. Measure and download the *transfer characteristics*, that is I_D vs. V_{GS} with V_{DS} as parameter. Program and download also the transconductance g_m. Graph I_D vs. V_{GS} (**graph 5**, linear scales) and g_m vs. V_{GS} (**graph 6**, linear scales). Extract and graph

the threshold voltage for different values of V_{DS} (**graph 7**, linear scales). State your definition of V_T.

3. Measure and download the *transfer characteristics in linear regime* for $V_{DS} = 0.1\ V$. Graph g_m vs. V_{GS} (**graph 8**, linear scales). Comment on how result compares with presentation in lecture.

4. Measure and download the *backgate characteristics in linear regime*, that is, I_D vs. V_{GS} with V_{BS} as parameter for $V_{DS} = 0.1\ V$. Graph the characteristics (**graph 9**, linear scales). Also graph the evolution of threshold voltage with V_{BS}. By matching these data with the equation given in class, extract the values of the γ parameter and ϕ_{sth} (**graph 10**, linear scales).

5. Measure and download the *backgate transconductance in saturation regime*, that is, g_{mb} vs. V_{BS} for $V_{GS} = 2.5\ V$ and $V_{DS} = 4\ V$. Have the HP4155 calculate g_{mb} for you. Graph the result. (**graph 11**, linear scales). Comment on the relative magnitude of g_m and g_{mb}.

6. Measure and download the *subthreshold characteristics*, that is I_D vs. V_{GS} with V_{DS} as parameter for $V_{DS} = 0.1\ V$. Graph I_D vs. V_{GS} (**graph 12**, log-linear scales). Extract the subthreshold slope.

This problem is likely to take a substantial amount of time. You must start early. The graphs need not be too fancy, just simply correct. They must have proper tickmarks, axis labeling and correct units. If there are several lines, each one should be properly identified (handwriting is OK).

If you encounter problems, please e-mail Lane (lbrooks@mit.edu), Samuel (smertens@mit.edu) or me (alamo@mit.edu). The MOSFET is real and it can be damaged. If the characteristics look funny, let us know. Most surely, there are still residual bugs in the system. Keep a note of them and give us feedback at the end of the exercise.

The system will be available over the following schedule:

Thursday 11/12, 5 PM through Monday 11/16, 10 AM.
Tuesday 11/17, 10 AM through Thursday 11/19, 10 AM.

After this time, the system will be dismantled and will no longer be available for this homework.

2. (40 points) This homework is to illustrate some of the trade-offs of using two different gate materials in modern MOSFETs.

a) Design a n-channel MOSFET with a n^+-polySi gate and a 100 $\mathring{A}$ oxide thickness to have a "long-channel" threshold voltage of +1 V.

b) Redesign the device using a gate metal that has a work function 0.55 eV larger than that of n^+-polySi. V_T should again be +1 V for a long-channel device.

c) Compute the field at the Si/SiO_2 interface at threshold for both structures.

d) Compute the oxide field at threshold for both structures.

e) Compute the depletion region thickness at threshold for both structures.

f) Estimate the minimum value of L_g that these two technologies can attain before short-channel effects become intolerable. Use the empirical formula given in class. Use $x_j = 0.06\ \mu m$. Make judicious assumptions. Use $V_{DD} = 5\ V$.

g) Discuss the tradeoffs of using one gate material vs. the other.