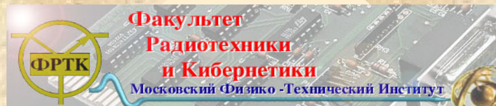

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RF AND MICROWAVE POWER AMPLIFIER DESIGN

A. Grebennikov, *RF and Microwave Power Amplifier Design*, New York: McGraw-Hill, 2004

LECTURE 1. NONLINEAR ACTIVE DEVICE MODELING

1.1. Power MOSFETs

- small-signal equivalent circuit and determination of its elements

- nonlinear I-V models

- nonlinear C-V models and charge conservation

1.2. GaAs MESFETs and HEMTs

- small-signal equivalent circuit and determination of its elements

- nonlinear I-V and C-V models

1.3. BJTs and HBTs

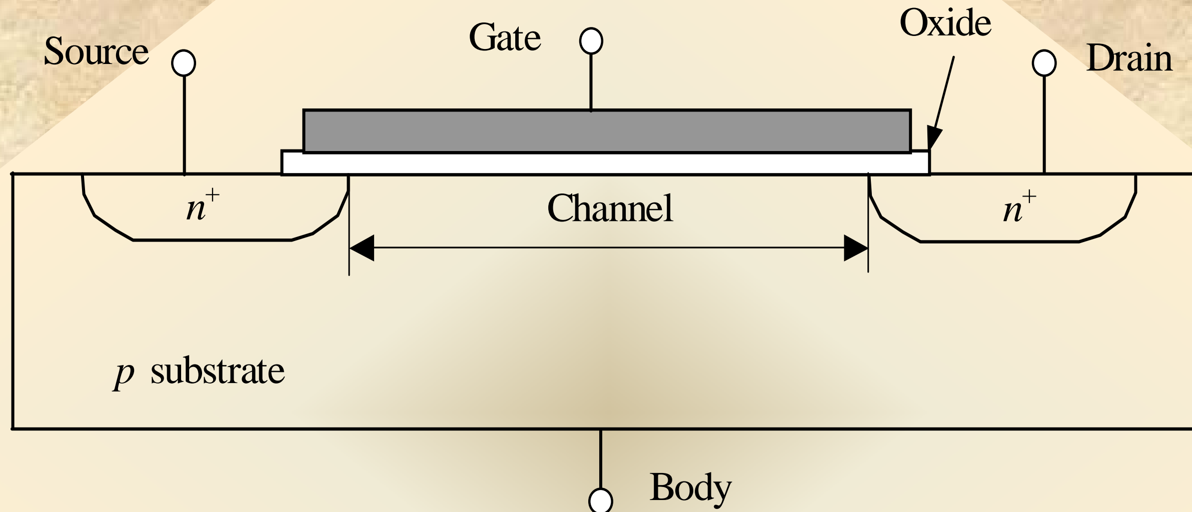
- small-signal equivalent circuit and determination of its elements

- equivalence of π -circuit and T-circuit topologies

- nonlinear I-V and C-Vmodels

1.1. Power MOSFETs

Simplified structure of n-channel metal-oxide-silicon (MOS) transistor



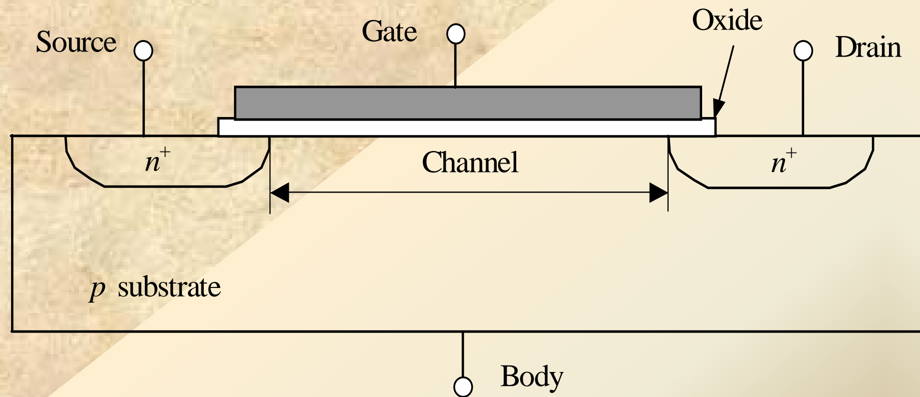
- transistor is formed on p-type silicon body (substrate)

- low-resistivity gate is formed on oxide top

- two heavily doped n regions with low resistivity: source and drain

- region between source and drain is channel characterized by its length L and width W

1.1. Power MOSFETs



Operation principle:

- *if gate potential is made sufficiently positive with respect to other part of the structure, electrons can be attracted directly below insulator*

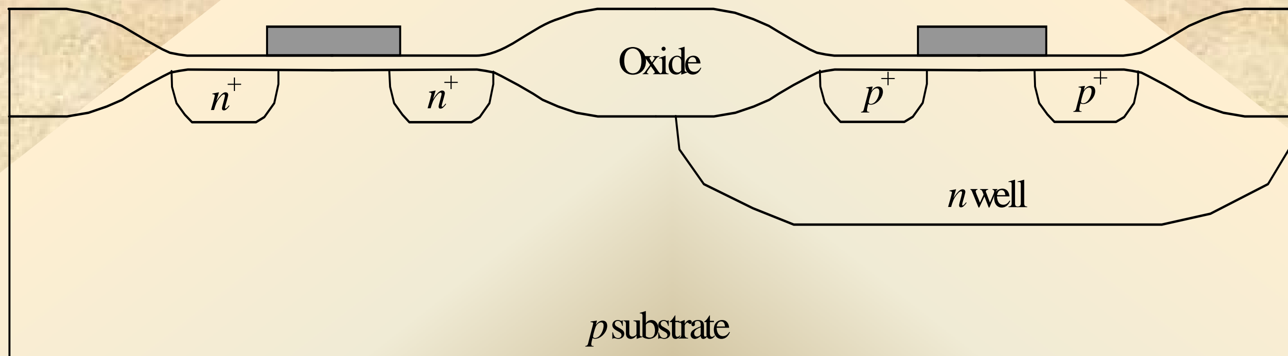
- *these electrons can come through n^+ regions where they exist in abundance and can fill channel between them*

- *number of electrons in channel can be varied through gate potential*

- *if two n^+ regions are biased at different potentials, lower-potential n^+ region acts as source for electrons, which then flow through channel and are drained by higher-potential n^+ region*

1.1. Power MOSFETs

Simplified structure of complimentary CMOS transistor (local oxidation of silicon)



- p substrate is common to all nMOS devices and serves as isolation region between them

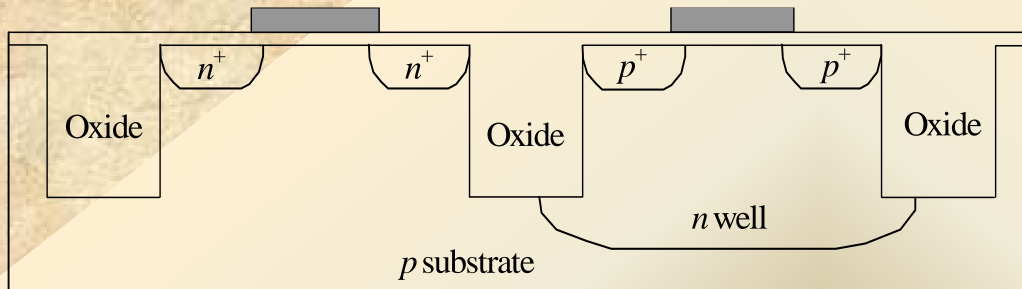
- pMOS devices are contained within n-type well regions

- thick oxide is needed to eliminate accident creation of parasitic channel underneath of it

- sufficient distance between various regions must be maintained to prevent latchup: elimination bipolar transistor action

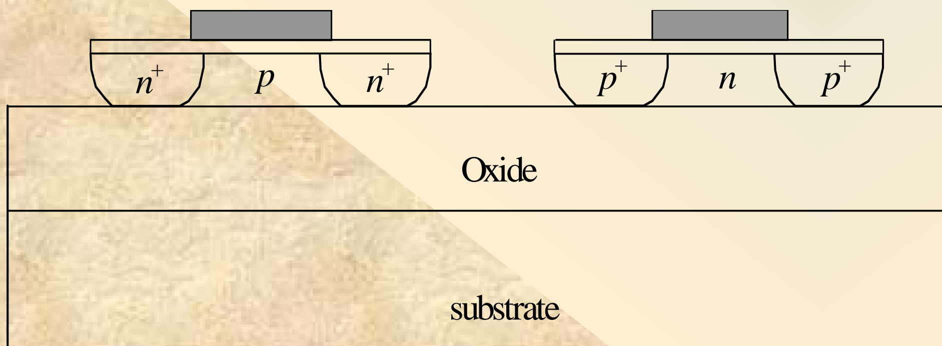
1.1. Power MOSFETs

Simplified structure of CMOS transistor (shallow-trench isolation)



- devices are closer to each other

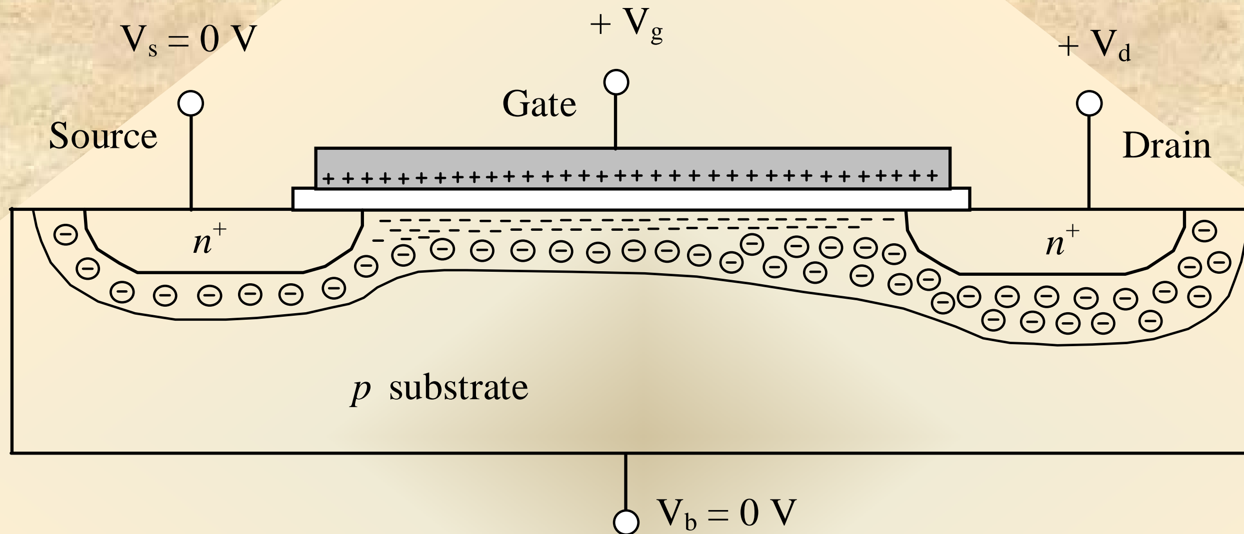
Simplified structure of CMOS transistor (silicon on insulator)



- complete device isolation

1.1. Power MOSFETs

N-channel MOS transistor under bias in inversion region



- positive charges applied to gate repel holes from surface ⇒ depletion region with negatively charged acceptors: **inversion**

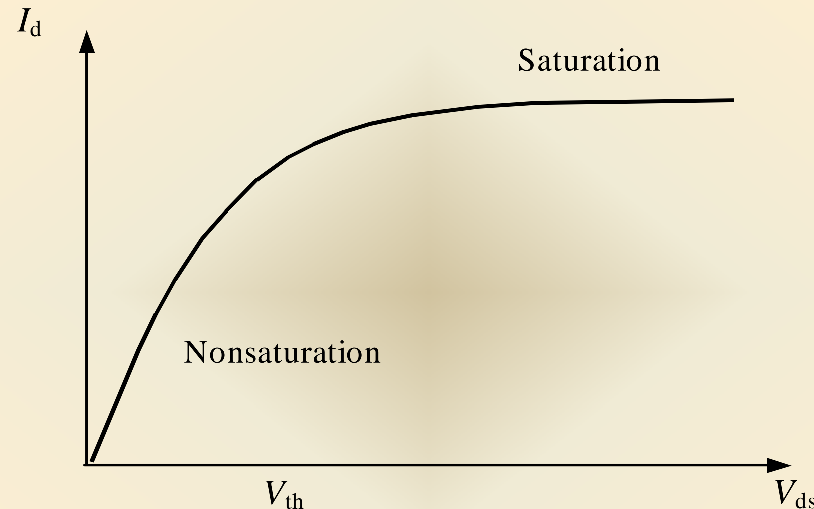
- drain potential is positive: larger number of negatively charged acceptors around drain than source

- fewer electrons are needed in channel near drain to balance positive gate charge: largest electron concentration near source

1.1. Power MOSFETs

N-channel MOS transistor under bias in inversion region

Gate potential is raised ⇒ three inversion region: weak inversion, moderate inversion and strong inversion

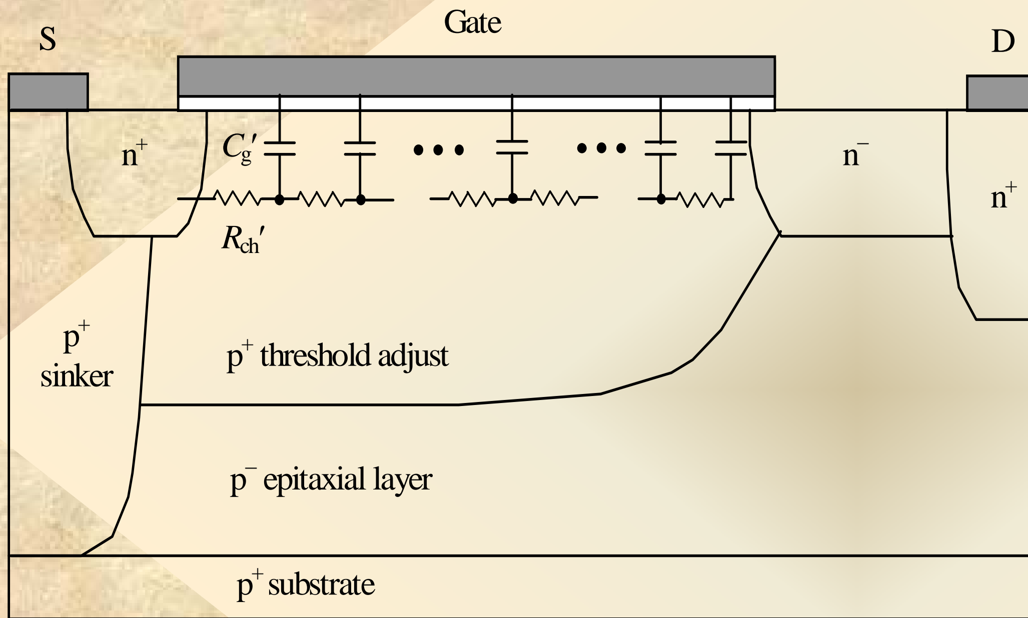


- **for small V_{ds}, effect of drain potential on drain current is large: nonsaturation region**

- **for large V_{ds}, drain current gradually tends to saturate draining all electrons that can be supplied by channel for given gate potential: saturation region**

1.1. Power MOSFETs

Physical structure of lateral diffusion MOS transistor (LDMOSFET)



- heavily doped p+ sinker for low resistivity between source and p+ substrate (source grounding) to provide high current flow between drain and source

- low substrate resistivity and sufficient distance between regions to prevent latchup (forward-biased p-n diodes): lightly doped p^- epitaxial layer and heavily doped p^+ substrate

- lightly doped n^- drain layer for drain-source breakdown protection

1.1. Power MOSFETs

Gate channel model: bias-dependent RC distributed transmission line

$$[ABCD] = \begin{bmatrix} \cosh\gamma L & Z_0 \sinh\gamma L \\ \dfrac{\sinh\gamma L}{Z_0} & \cosh\gamma L \end{bmatrix} \Rightarrow Z_{gs} = \frac{A}{C} = R_{ch}\frac{\coth\gamma L}{\gamma L}$$

where $\gamma = \sqrt{j\omega R'_{ch} C'_g}$ - propagation constant,

$Z_o = R'_{ch} / \gamma$ - characteristic impedance

$R'_{ch} = R_{ch} / L$ - gate charging resistance per unit length

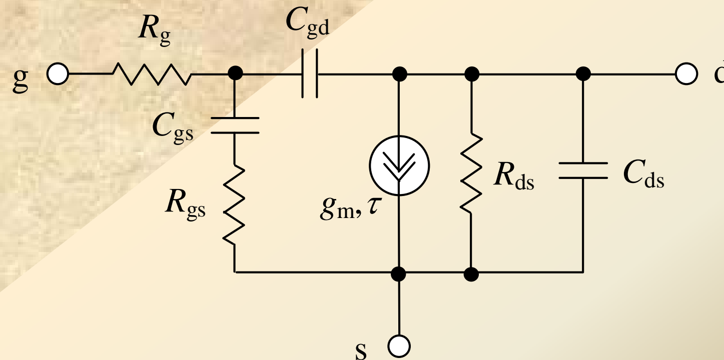
$C'_g = C_g / L$ - gate capacitance per unit length

$$Z_{gs} = R_{ch}\frac{\coth\gamma L}{\gamma L} \cong \frac{R_{ch}}{\gamma L}\left(\frac{1}{\gamma L} + \frac{\gamma L}{3}\right) = \frac{R_{ch}}{3} + \frac{1}{j\omega C_g}$$

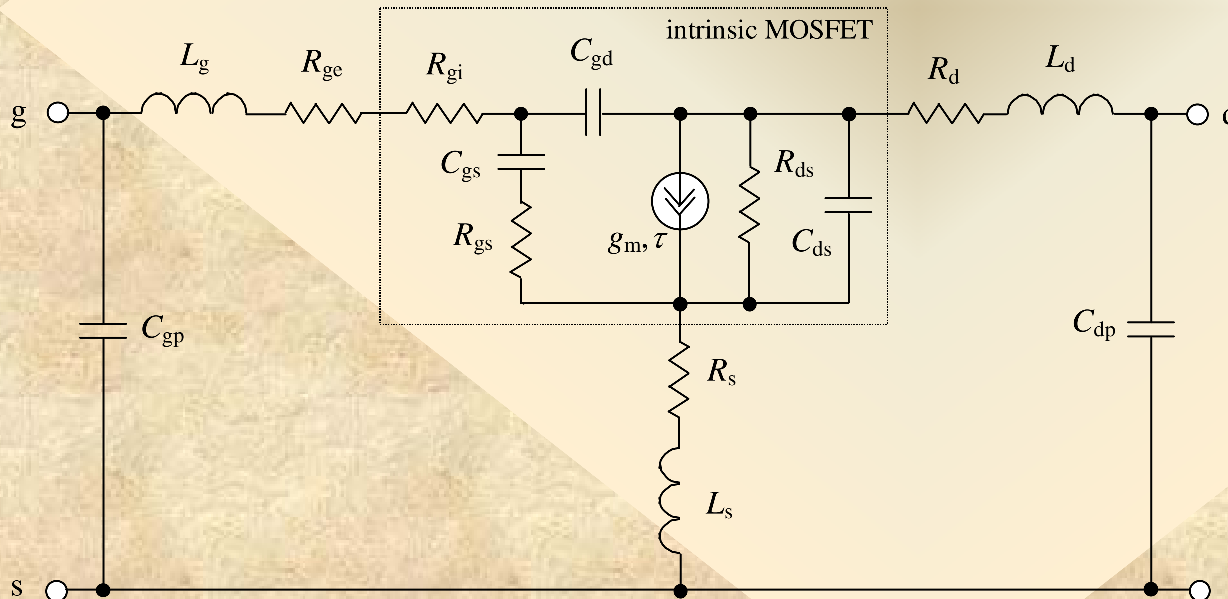
- intrinsic impedance between gate and source

1.1. Power MOSFETs

Equivalent circuit of lateral diffusion MOS transistor (LDMOSFET)



- intrinsic device model including nonlinear current source and device resistances and capacitances



- complete small-signal MOSFET equivalent circuit describing device electrical behavior over entire frequency range up to maximum frequency

1.1. Power MOSFETs

Determination of equivalent circuit parameters

To determine intrinsic circuit parameters, it is best to use Y-parameters for intrinsic device:

$$Y = \begin{bmatrix} \dfrac{j\omega C_{gs}}{1 + j\omega\tau_g} + j\omega C_{gd} & -j\omega C_{gd} \\ \dfrac{g_m \exp(-j\omega\tau)}{1 + j\omega\tau_g} - j\omega C_{gd} & G_{ds} + j\omega\left(C_{ds} + C_{gd}\right) \end{bmatrix}$$

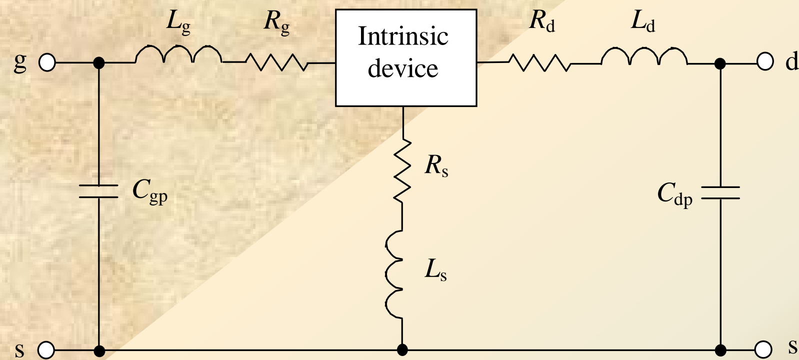
where $\tau_g = R_{gs} C_{gs}$ ***- gate constant ,*** τ ***- effective channel carrier transit time***

For known (measured or analytically estimated) extrinsic parameters, procedure of determination of intrinsic Y-parameters from experimental data is:

- ***measurement of S-parameters of extrinsic device***
- ***transformation of S-parameters to Y-parameters with subtraction of parallel elements: capacitances***
- ***transformation of Y-parameters to Z-parameters with subtraction of series elements: inductances***
- ***transformation of Z-parameters to Y-parameters of intrinsic device two-port network***

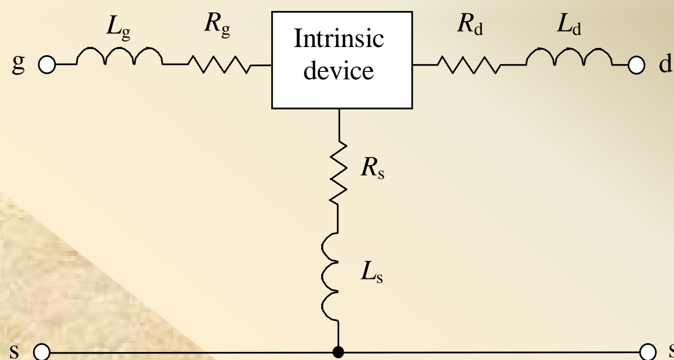
1.1. Power MOSFETs

Determination of equivalent circuit parameters



$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix}$$

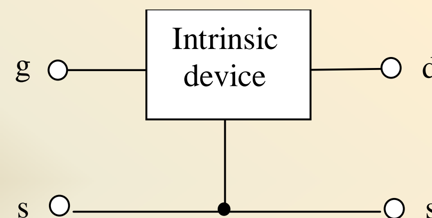
- transformation of S-parameters to Y-parameters with subtraction of parallel elements: capacitances



$$\begin{bmatrix} Y_{11} - j\omega C_{gp} & Y_{12} \\ Y_{21} & Y_{22} - j\omega C_{dp} \end{bmatrix}$$

- transformation of Y-parameters to Z-parameters with subtraction of series elements: inductances

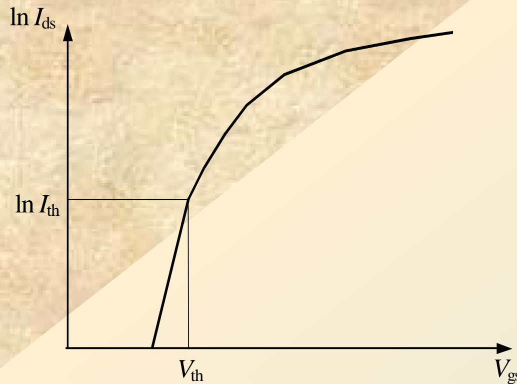
$$\begin{bmatrix} Z_{11} - R_g - R_s - j\omega(L_g + L_s) & Z_{12} - R_s - j\omega L_s \\ Z_{21} - R_s - j\omega L_s & Z_{22} - R_d - R_s - j\omega(L_d + L_s) \end{bmatrix}$$

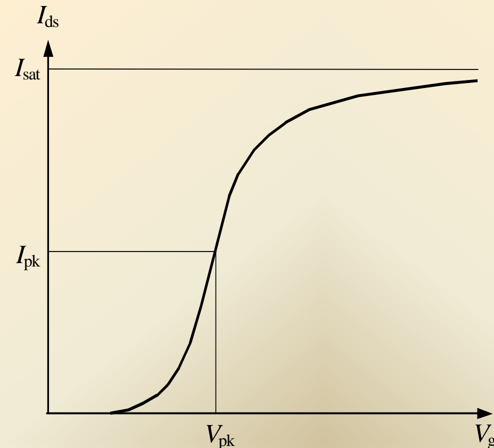


- transformation of Z-parameters to Y-parameters of intrinsic device two-port network

1.1. Power MOSFETs

Nonlinear I-V models





- ***drain current in strong-inversion region is proportional to square of V_{gs} - V_{th}***
- ***drain current in weak-inversion region is dominated by diffusion component - exponential dependencies***

To achieve continuous behavior from weak-inversion region to strong-inversion region ⇒

$$I_{ds}(V_{gs}) = A\left\{\ln\left[1+\exp\left(B\left(V_{gs}-V_{th}\right)\right)\right]\right\}^2$$

where $I_{ds}\big|_{V_{gs}=V_{th}} = I_{th}$ $\quad \left.\dfrac{\partial I_{ds}}{\partial V_{gs}}\right|_{V_{gs}=V_{th}} = S_{th}$

To describe drain current in saturation region ⇒

$$I_{max}(V_{ds}) = I_{sat}\left(1+\lambda V_{ds}\right)\tanh\left(\alpha V_{ds}\right)$$

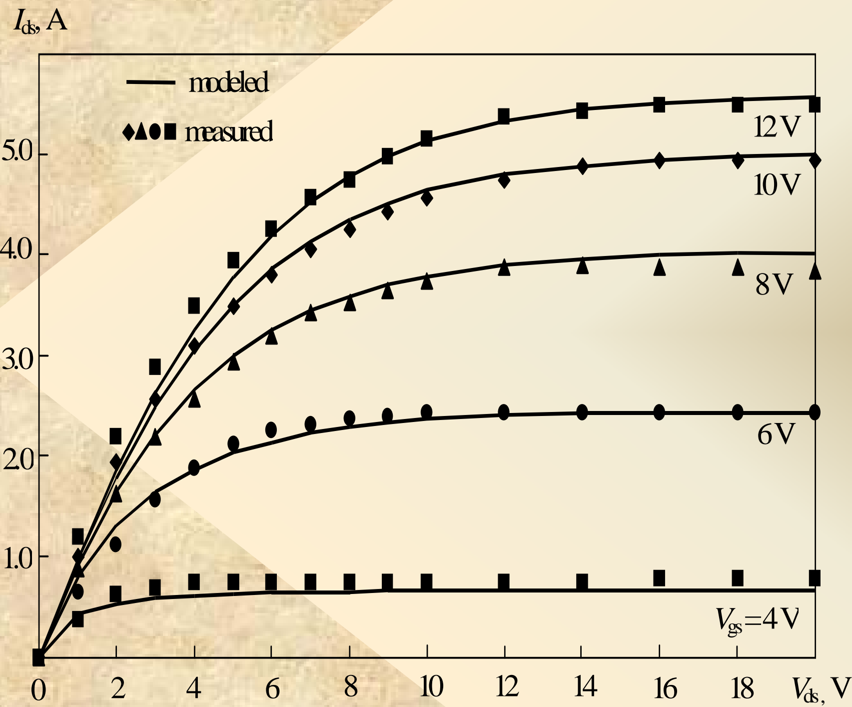
Entire I-V model ⇒

$$I_{ds}(V_{gs}, V_{ds}) = I_o \Bigg/ \left[1+\left(\frac{I_o}{I_{max}}\right)^n\right]^{\frac{1}{n}}$$

1.1. Power MOSFETs

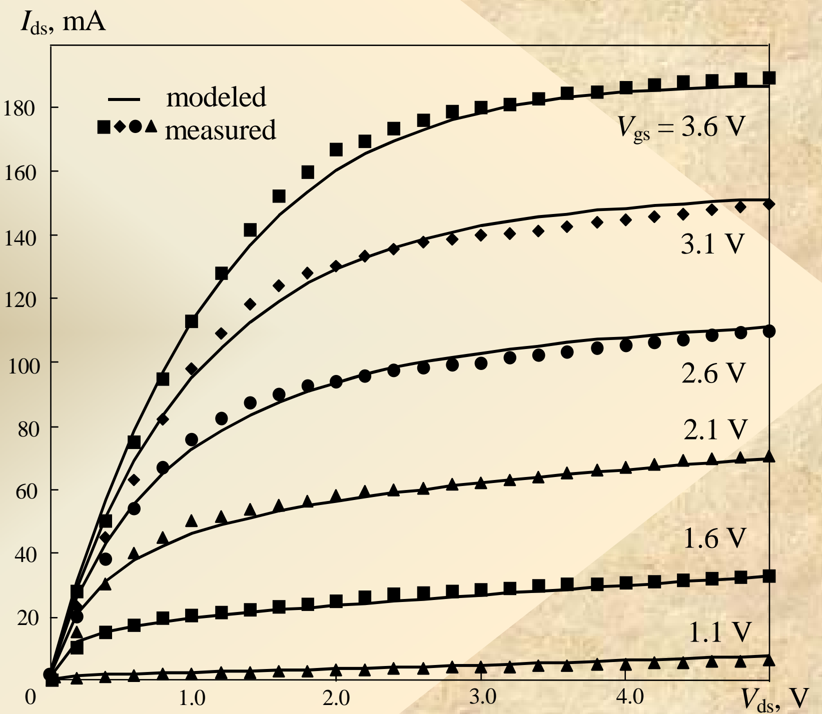
Nonlinear I-V models

High voltage LDMOSFET (l = 1.1 um, w = 4 cm)



Mean-square error - 0.5%

Low voltage MOSFET (w = 2 mm)

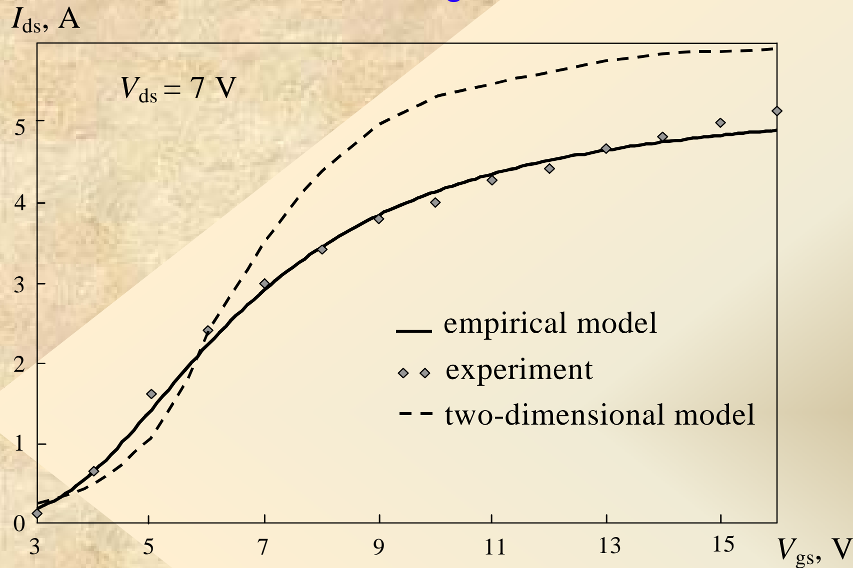


Mean-square error - 0.42%

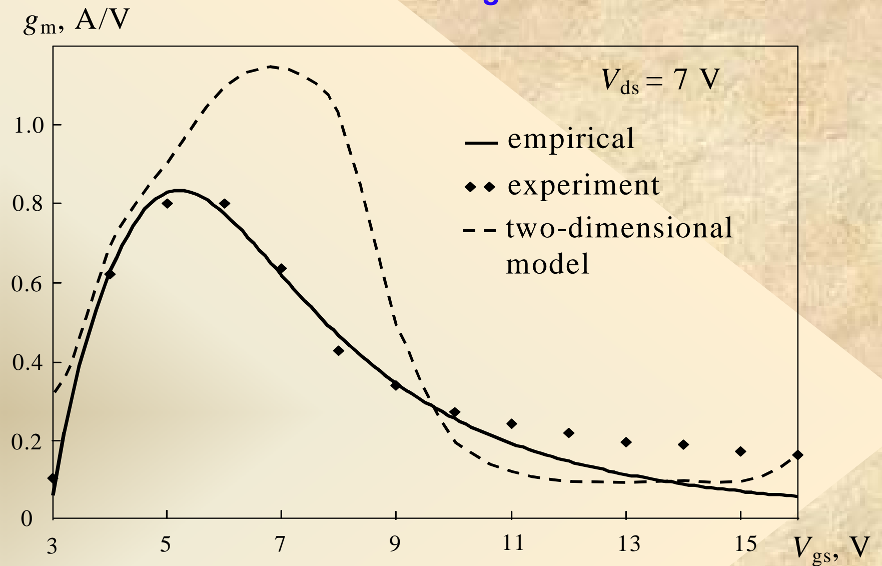
1.1. Power MOSFETs

Nonlinear I-V models: high voltage LDMOSFET

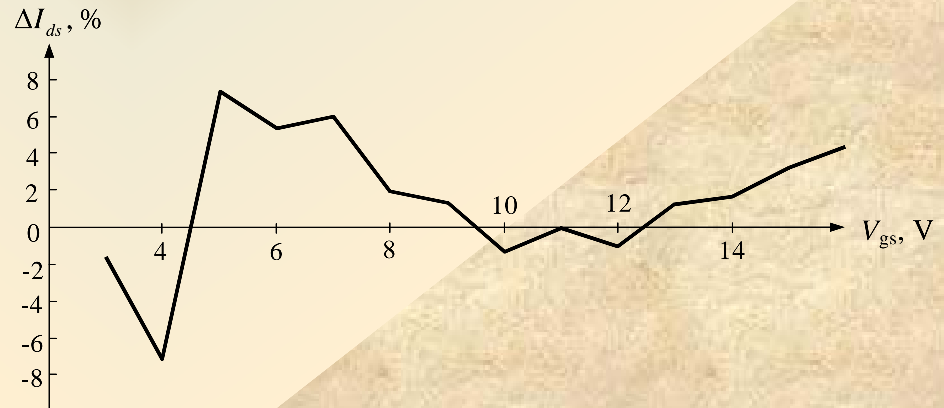
I_{ds} vs V_{gs}



g_m vs V_{gs}



Normalized linear deviation of I_{ds} vs V_{gs}

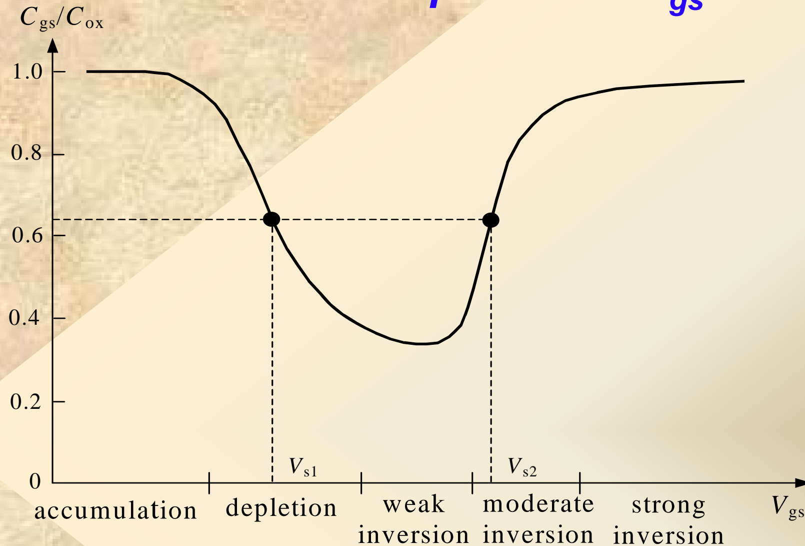


- *maximum deviation of 8% in inversion region*

1.1. Power MOSFETs

Nonlinear C-V models

Gate-source capacitance C_{gs}



- constant in accumulation region equal to total intrinsic oxide capacitance
- reduces in depletion and weak-inversion regions and increases in moderate inversion region
- constant in saturation region equal to 2/3 of oxide capacitance

$$C_{gs} = C_{gsmin} + C_s\left\{1 + \tanh\left[\frac{S}{C_s}\left(V_{gs} - V_s\right)\right]\right\}$$

- hyperbolic function to describe each part of Cgs (Vgs)

where

$$S_1 = \left.\frac{\partial C_{gs}}{\partial V_{gs}}\right|_{V_{gs}=V_{s1}} \qquad S_2 = \left.\frac{\partial C_{gs}}{\partial V_{gs}}\right|_{V_{gs}=V_{s2}}$$

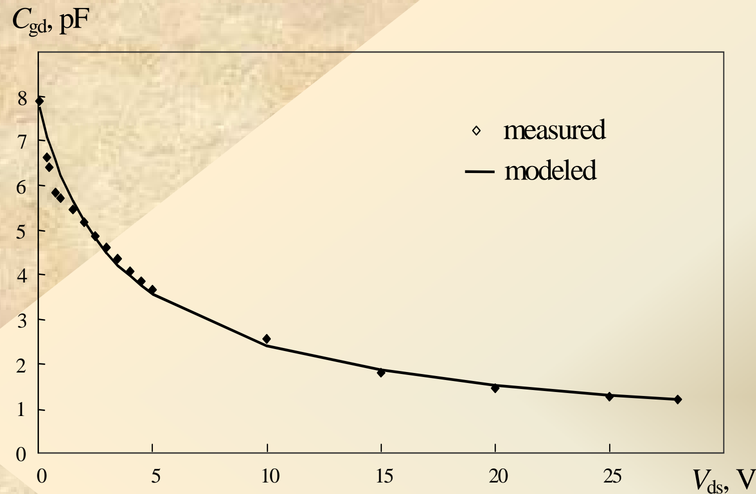
$$C_{gs} = C_{gsmax} - C_{gso}\left\{1 + \tanh\left[\frac{S_1}{C_s}\left(V_{gs} - V_{s1}\right)\right]\right\}\left\{1 + \tanh\left[\frac{S_2}{C_s}\left(V_{gs} - V_{s2}\right)\right]\right\}$$

- resulting approximation

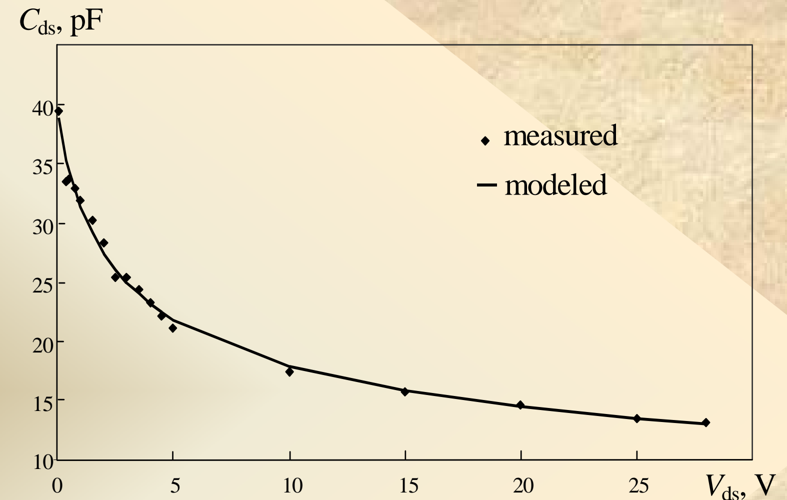
1.1. Power MOSFETs

Nonlinear C-V models

Gate-drain capacitance C_{gd}



Drain-source capacitance C_{ds}



$$C_{gd(ds)} = C_{gdo(dso)} \left(\frac{\varphi + V_{dso}}{\varphi + V_{ds}} \right)^{m}$$

- junction approximation

where m depends on doping concentration

For LDMOSFETs ⇒

Capacitance	$C_{gd(ds)o}$, pF	m	φ, V
C_{gd}	7.88	0.8	2.94
C_{ds}	39.42	0.33	1.0

Mean-square error - 4.3%

1.1. Power MOSFETs

Charge conservation

$$\begin{bmatrix} I_g \\ I_d \\ I_s \end{bmatrix} = j\omega \begin{bmatrix} C_{gg} & -C_{gd} & -C_{gs} \\ -C_{dg} & C_{dd} & -C_{ds} \\ -C_{sg} & -C_{sd} & C_{ss} \end{bmatrix} \cdot \begin{bmatrix} V_g \\ V_d \\ V_s \end{bmatrix}$$

- matrix equation for small-signal charging circuit in frequency domain: three-terminal MOSFET

To transform three-terminal into two-port network with common source terminal ⇒

$I_g = I_{gs}$, $I_d = I_{ds}$, $I_s = -(I_{gs} + I_{ds})$
$V_g - V_s = V_{gs}$, $V_d - V_s = V_{ds}$

$$C_{gg} = C_{gd} + C_{gs} = C_{dg} + C_{sg},$$
$$C_{dd} = C_{dg} + C_{ds} = C_{gd} + C_{sd},$$
$$C_{ss} = C_{sg} + C_{sd} = C_{gs} + C_{ds},$$

$$Y_c = \begin{bmatrix} j\omega(C_{gs} + C_{gd}) & -j\omega C_{gd} \\ -j\omega(C_{gd} + C_m) & j\omega(C_{ds} + C_m + C_{gd}) \end{bmatrix}$$

- relationships between capacitances in three-terminal devices

- admittance matrix for capacitive two-port network where $C_m = C_{dg} - C_{gd}$ is transcapacitance

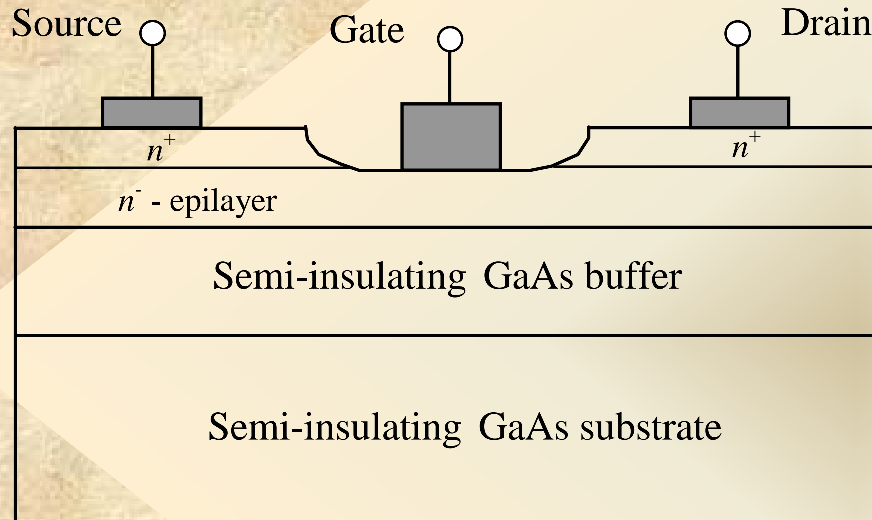
$$g_m - j\omega C_m = g_m \sqrt{1 + \left(\frac{\omega}{\omega_T} \frac{C_m}{C_{gs}}\right)^2} \exp\left[-j\tan^{-1}\left(\frac{\omega}{\omega_T} \frac{C_m}{C_{gs}}\right)\right] \cong g_m \exp(-j\omega\tau_c)$$

where

$$\tau_c = C_m / \omega_T C_{gs}$$

1.2. GaAs MESFETs and HEMTs

Simplified structure of GaAs metal-semiconductor field-effect transistor (MESFET)



- transistor is formed on semi-insulating GaAs substrate

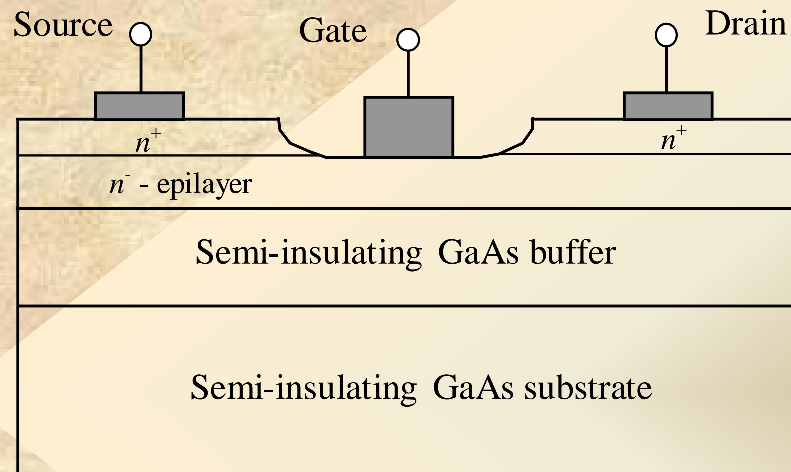
- n-doped epilayer is necessary to realize channel and is made thicker to minimize source and drain resistances

- two heavily doped n regions with low resistivity between metal source and drain

- semi-insulating buffer for high resistivity and to prevent impurities in substrate from diffusing into epilayer

1.2. GaAs MESFETs and HEMTs

Operation principle:



- if two n^+ regions are biased at different potentials, lower-potential n^+ region acts as source for electrons, which then flow through channel and are drained by higher-potential n^+ region

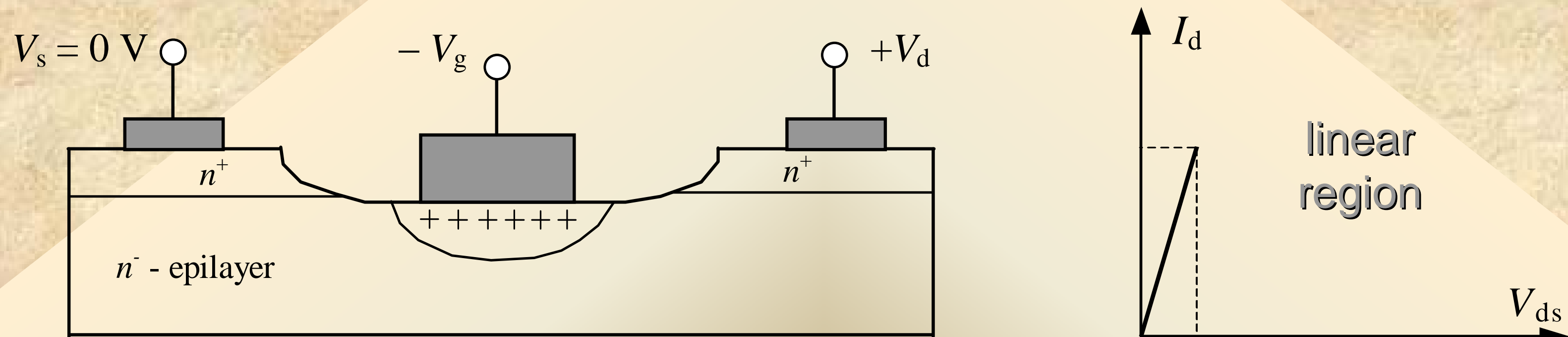
- depletion region under Schottky-barrier gate is formed containing only positively charged donors

- thickness of depletion region can be varied through gate potential resulting in changing of channel conductivity

- channel current is due to electrons and device operation speed is defined by only velocity of charge variation under gate

1.2. GaAs MESFETs and HEMTs

GaAs MESFET operation

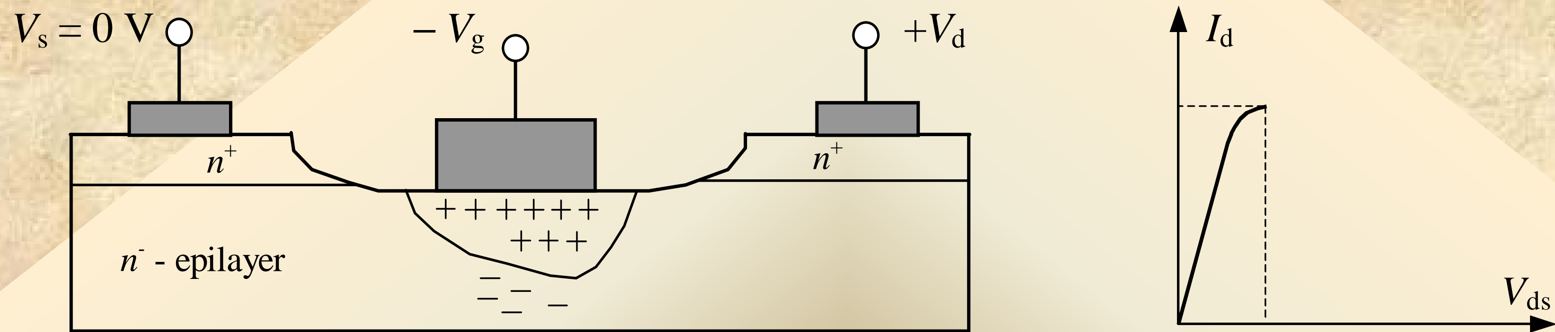


- when $V_{gs} = 0$ V and V_{ds} is raised from zero to some low value, depletion region under gate is relatively narrow with longitudinal electric field and current in channel where current is proportional to V_{ds}

- when $V_{gs} < 0$ V and V_{ds} = const, depletion region widens reducing current and at some pinch-off voltage channel becomes fully depleted with zero drain current

1.2. GaAs MESFETs and HEMTs

GaAs MESFET operation

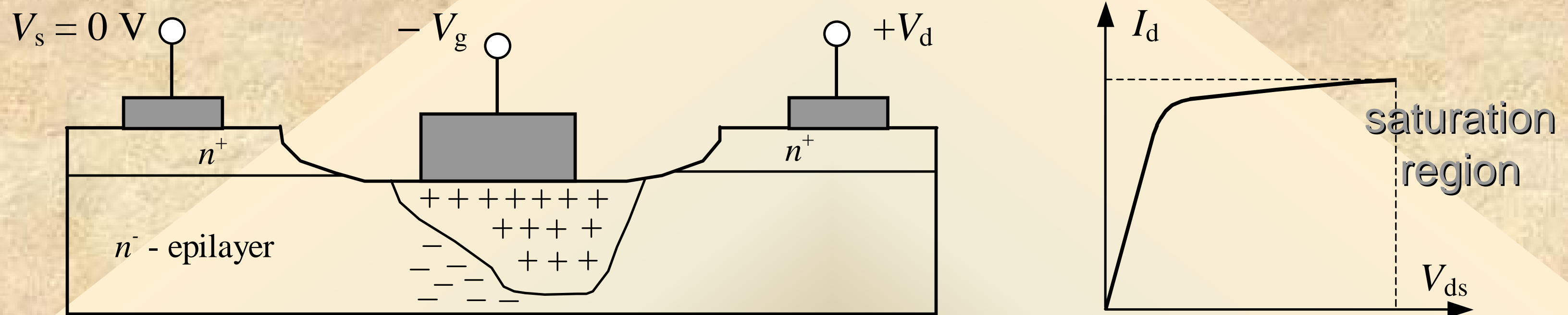


- when $V_{gs} = 0$ V and V_{ds} is raised further, channel current increases; however, depletion region becomes wider at drain end with narrower conductive channel resulting in region of electron accumulation near gate end

- for higher V_{ds}, electron cannot move faster as electron velocity cannot exceed their saturated drift velocity

1.2. GaAs MESFETs and HEMTs

GaAs MESFET operation

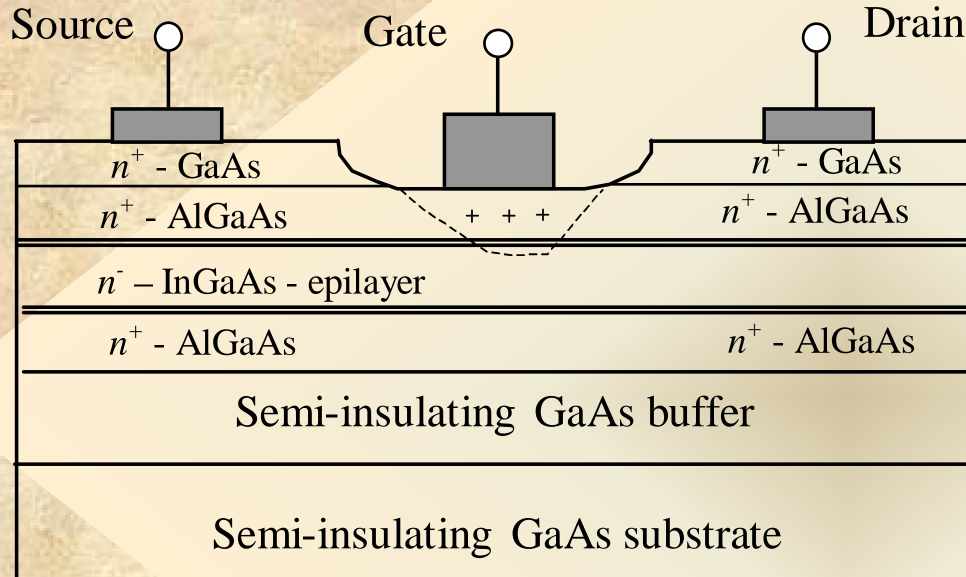


- as V_{ds} is increased further, depleted region widens towards drain and more of voltage increase is dropped across depletion region (charge domain) whereas less is dropped across unsaturated region

- saturation occurs when electrons move at saturated drift velocity over large part of channel length; no longer increase in charge in depletion region, so gate-drain capacitance reduces to stray capacitance between metalizations whereas gate-source capacitance rises to approximately twice compared with value in linear operation

1.2. GaAs MESFETs and HEMTs

High mobility electron transistor (HEMT)



- transistor is formed on semi-insulating GaAs substrate

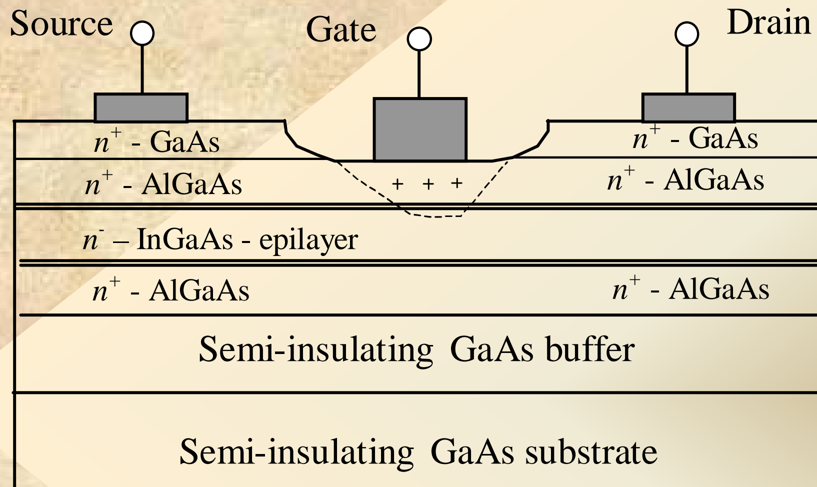
- two heavily n-doped GaAs regions with low resistivity between metal source and drain

- two heavily n-doped AlGaAs layers with high energetic barrier for holes to maximize high electron mobility in channel

- undoped InGaAs n-epilayer as channel

1.2. GaAs MESFETs and HEMTs

HEMT: operation principle



- ***if two n^+ regions are biased at different potentials, lower-potential n^+ region acts as source for electrons, which then flow through channel and are drained by higher-potential n^+ region***

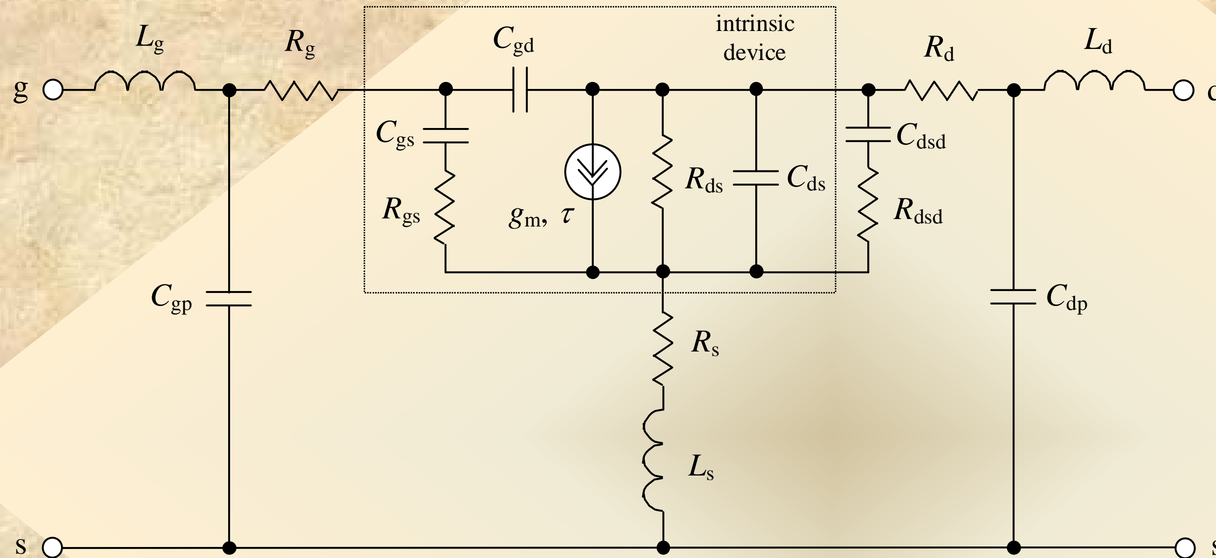
- ***depletion region under Schottky-barrier gate is formed containing only positively charged donors***

- ***two heavily n-doped AlGaAs layers with high energetic barriers for holes and low energetic barrier for electrons protect channel from hole injection resulting in high mobility of electrons in channel (in 3 times higher than electron saturation velocity in GaAs epilayer)***

- ***spacing between AlGaAs layer and InGaAs channel is optimized to achieve high breakdown voltage***

1.2. GaAs MESFETs and HEMTs

Small-signal equivalent circuit of MESFET and HEMT



$$C_{gd} = \frac{\partial (Q_g + Q_d)}{\partial V_{gd}}$$

$$C_{gs} = \frac{\partial (Q_g + Q_d)}{\partial V_{gs}}$$

- gate-source capacitance C_{gs} and gate-drain capacitance C_{gd} represent charging effect in depletion region; drain-source capacitance C_{ds} is small and its influence is insignificant

- capacitance C_{dsd} and resistance R_{dsd} represent model dispersion of I-V characteristic due to trapping effects in channel resulting in discrepancy between DC measurement and S-parameter measurements at high frequencies

Determination of equivalent circuit parameters

To determine intrinsic circuit parameters, it is best to use Y-parameters for intrinsic device:

$$Y = \begin{bmatrix} \dfrac{j\omega C_{gs}}{1+j\omega\tau_g} + j\omega C_{gd} & -j\omega C_{gd} \\ \dfrac{g_m \exp(-j\omega\tau)}{1+j\omega\tau_g} - j\omega C_{gd} & \dfrac{1}{R_{ds}} + j\omega\left(C_{ds}+C_{gd}\right) \end{bmatrix}$$

where $\tau_g = R_{gs}C_{gs}$ **- gate constant ,** τ **- effective channel carrier transit time**

From real and imaginary parts of intrinsic Y-parameters:

$$C_{gd} = -\frac{\operatorname{Im} Y_{12}}{\omega} \Rightarrow C_{gs} = -\frac{\operatorname{Im} Y_{11} - \omega C_{gd}}{\omega}\left[1 + \left(\frac{\operatorname{Re} Y_{11}}{\operatorname{Im} Y_{11} - \omega C_{gd}}\right)^2\right] \qquad C_{ds} = \frac{\operatorname{Im} Y_{22} - \omega C_{gd}}{\omega}$$

$$\Downarrow$$

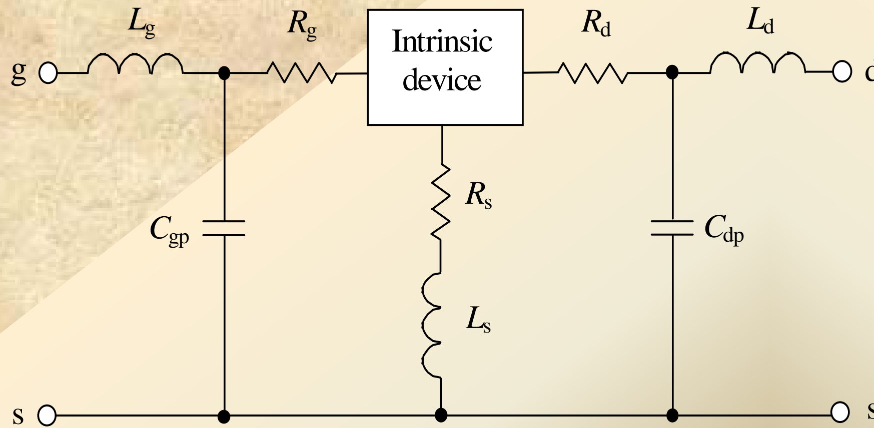
$$R_{gs} = \frac{\operatorname{Re} Y_{11}}{\left(\operatorname{Im} Y_{11} - \omega C_{gd}\right)^2 + \left(\operatorname{Re} Y_{11}\right)^2} \Rightarrow g_m = \sqrt{\left(\operatorname{Re} Y_{21}\right)^2 + \left(\operatorname{Im} Y_{21} + \omega C_{gd}\right)^2} \cdot \sqrt{1 + \left(\omega C_{gs} R_{gs}\right)^2}$$

$$\Downarrow$$

$$R_{ds} = \frac{1}{\operatorname{Re} Y_{22}} \qquad \tau = \frac{1}{\omega}\sin^{-1}\left(\frac{-\omega C_{gd} - \operatorname{Im} Y_{21} - \omega C_{gs} R_{gs} \operatorname{Re} Y_{21}}{g_m}\right)$$

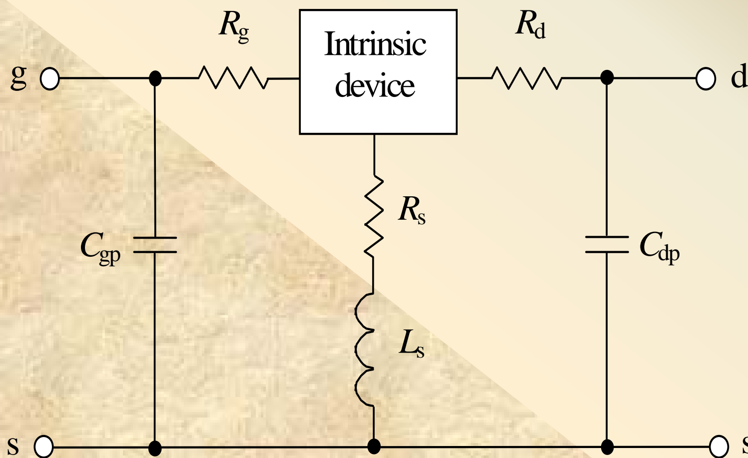
1.2. GaAs MESFETs and HEMTs

Determination of equivalent circuit parameters



$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix}$$

- measurements of S-parameters of full equivalent circuit

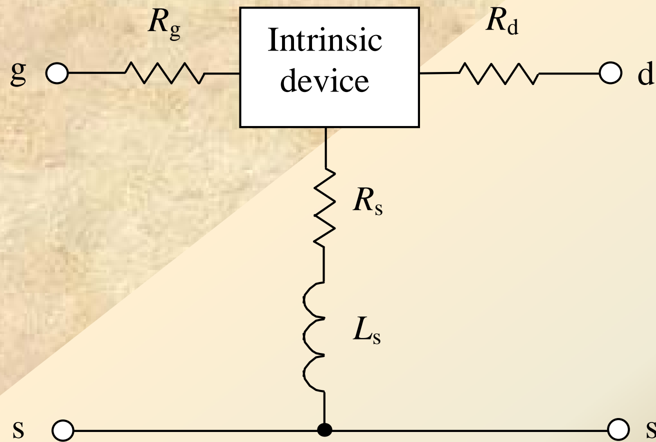


$$\begin{bmatrix} Z_{11} - j\omega L_g & Z_{12} \\ Z_{21} & Z_{22} - j\omega L_d \end{bmatrix}$$

- transformation of S-parameters to Z-parameters with subtraction of series inductances

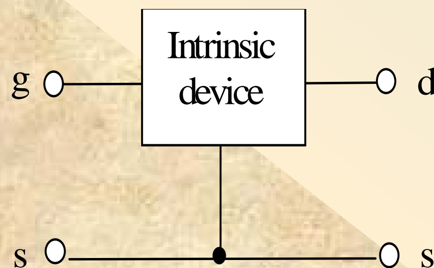
1.2. GaAs MESFETs and HEMTs

Determination of equivalent circuit parameters



$$\begin{bmatrix} Y_{11} - j\omega C_{gp} & Y_{12} \\ Y_{21} & Y_{22} - j\omega C_{dp} \end{bmatrix}$$

- transformation of Z-parameters to Y-parameters with subtraction of parallel capacitances



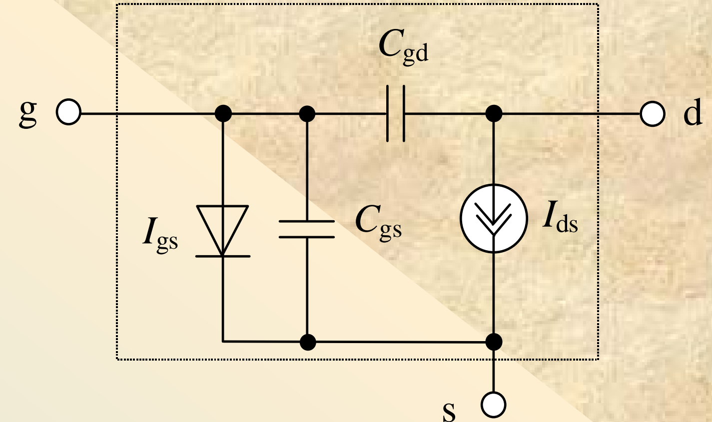
$$\begin{bmatrix} Z_{11} - R_g - R_s - j\omega L_s & Z_{12} - R_s - j\omega L_s \\ Z_{21} - R_s - j\omega L_s & Z_{22} - R_d - R_s - j\omega L_s \end{bmatrix}$$

- transformation of Y-parameters to Z-parameters with subtraction of series resistances and inductance

- transformation of Z-parameters to intrinsic two-port Y-parameters

Nonlinear I-V and C-V models

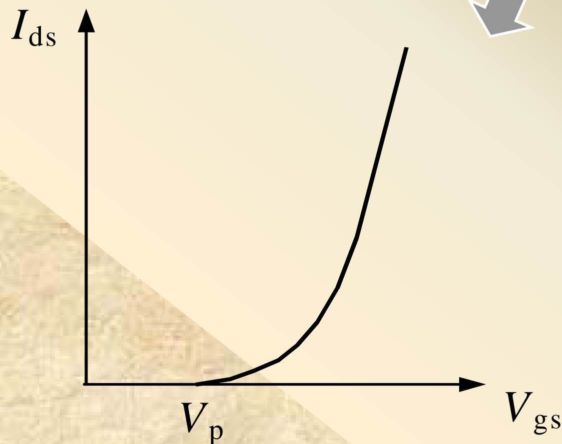
Curtice quadratic model

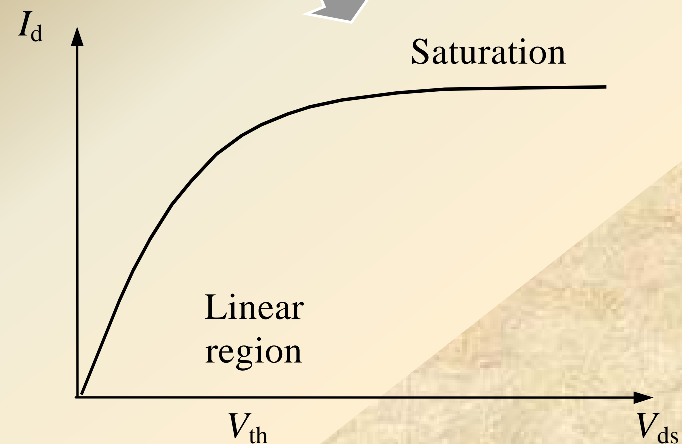


$$C_{gs} = C_{gs0} / \left(1 - \frac{V_{gs}}{V_{gsi}}\right)^{0.5}$$

- abrupt junction approximation

$$I_{ds} = \beta \left(V_{gs} - V_p\right)^2 \left(1 + \lambda V_{ds}\right) \tanh\left(\alpha V_{ds}\right)$$





where λ - slope in saturation region

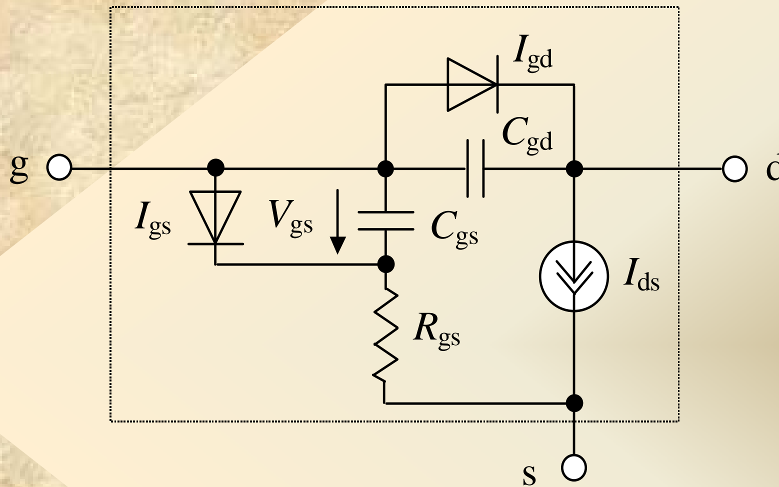
V_p - pinch-off voltage

β - transconductance parameter defined from experimental data

1.2. GaAs MESFETs and HEMTs

Nonlinear I-V and C-V models

Curtice cubic model



- *additional gate-source resistor R_{gs}*
- *additional diode between drain and gate*

$$I_{ds} = \left(A_0 + A_1 V_{gs} + A_2 V_{gs}^2 + A_3 V_{gs}^3\right) \tanh\left(\gamma V_{ds}\right)$$

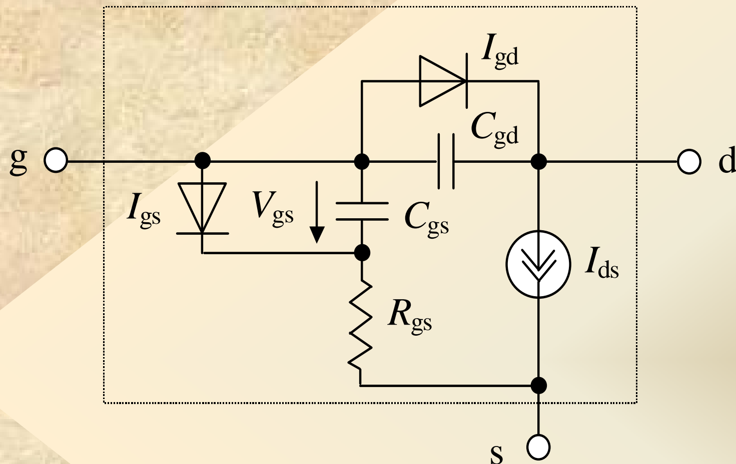
$$C_{gs} = C_{gs0} / \left(1 - \frac{V_{gs}}{V_{gsi}}\right)^{0.5}$$

- abrupt junction approximation

1.2. GaAs MESFETs and HEMTs

Nonlinear I-V and C-V models

Materka model



$$I_{ds} = I_{dss}\left(1 - \frac{V_{gs}}{V_p}\right)^2 \tanh\left(\frac{\alpha V_{ds}}{V_{gs} - V_p}\right)$$

$$I_{gs} = I_{gss}\left[\exp\left(\alpha_s V_{gs}\right) - 1\right]$$

$$I_{gd} = I_{gdsr}\left[\exp\left(\alpha_{sr} V_{gd}\right) - 1\right]$$

$$C_{gs} = C_{gs0} \Big/ \left(1 - \frac{V_{gs}}{V_{gsi}}\right)^{0.5}$$

TriQuint model

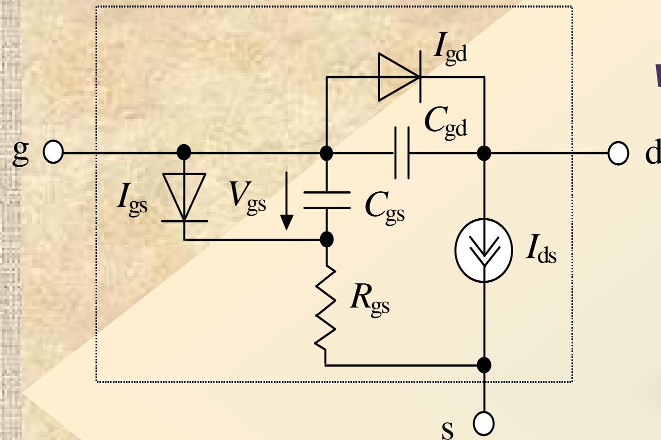
$$I_{ds} = \frac{I_{ds0}}{1 + \delta V_{ds} I_{ds0}},$$

$$I_{ds0} = \begin{cases} \beta\left(V_{gs} - V_T\right)^Q\left[1 - \left(1 - \dfrac{\alpha V_{ds}}{3}\right)^3\right], & 0 < V_{ds} < \dfrac{3}{\alpha} \\ \beta\left(V_{gs} - V_T\right)^Q, & V_{ds} \geq \dfrac{3}{\alpha} \end{cases}$$

- ***better approximation at near pinch-off region***
- ***decrease of drain current I_{ds} at higher values which is result of self-heating effect***

Nonlinear I-V and C-V models

Angelov model

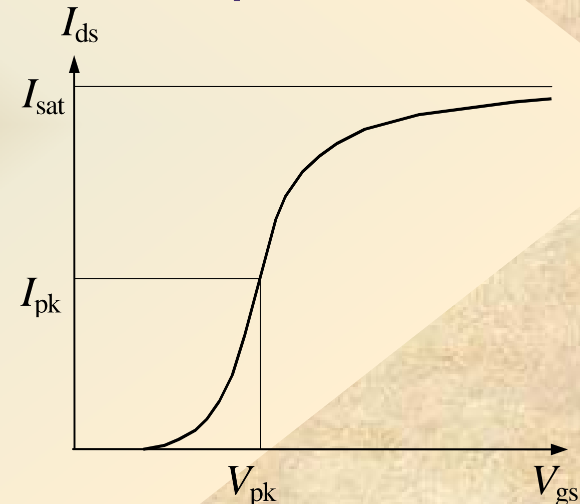


$$I_{ds} = I_{pk}(1 + \tanh\psi)(1 + \lambda V_{ds})\tanh(\alpha V_{ds})$$

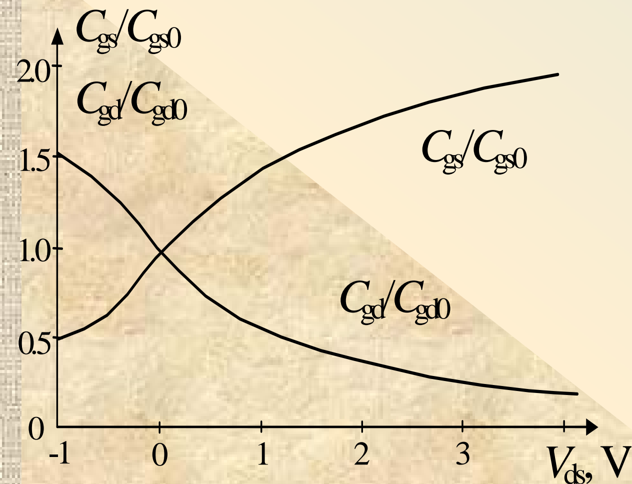
where I_{pk} - drain current at maximum transconductance

$$\psi = P_1(V_{gs} - V_{pk}) + P_2(V_{gs} - V_{pk})^2 + P_3(V_{gs} - V_{pk})^3 + \ldots$$

where P_i can be obtained from experimental data



Accurate description of I_{ds}-V_{gs} dependence in pinch-off and saturation regions



$$C_{gs} = C_{gs0}\left[1 + \tanh(P_{1gsg}V_{gs})\right]\left[1 + \tanh(P_{1gsd}V_{ds})\right]$$

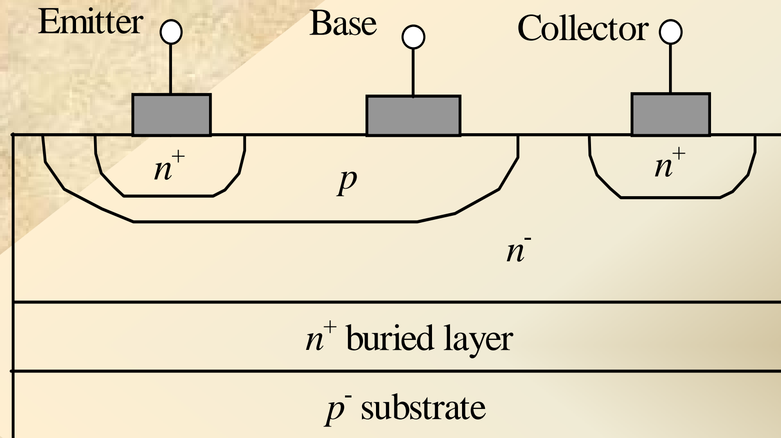
$$C_{gd} = C_{gd0}\left[1 + \tanh(P_{1gdg}V_{gs})\right]\left[1 - \tanh(P_{1gdd}V_{ds} + P_{1cc}V_{gs}V_{gd})\right]$$

where P_{1gsg}, P_{1gsd}, P_{1gdg}, P_{1gdd} are fitting parameters

1.3. BJTs and HBTs

Simplified structures of n-p-n bipolar-junction transistor (BJT)

BJT for integrated circuit made by planar process



- heavily doped n-region is diffused into p-region to produce emitter-base junction

- lightly doped p-type layer is used for substrate

- lightly n-doped collector region allows collector-base junction to sustain relatively high voltages without breaking down

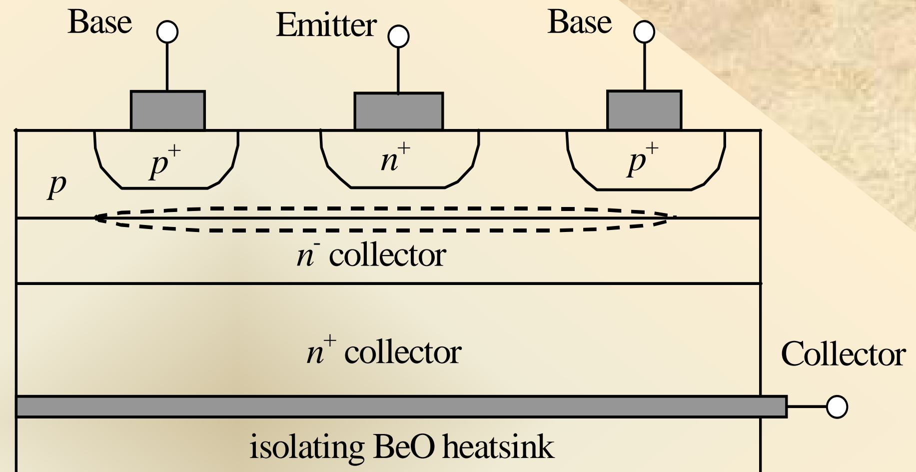
- heavily n-doped buried layer added to reduce series resistance between junction and metallic collector contact

- base doping level and its width is quite small to minimize base transit time and maximize electron injection efficiency from emitter

1.3. BJTs and HBTs

Simplified structures of n-p-n bipolar-junction transistor (BJT)

BJT for power application



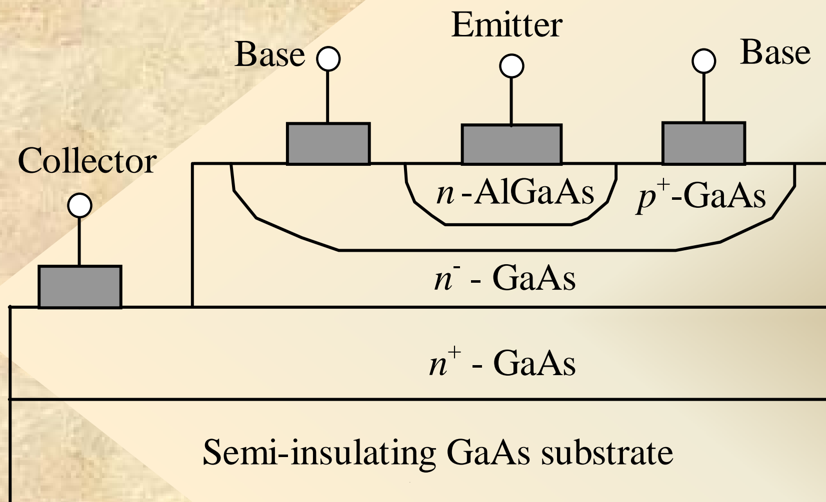
- for constant base-emitter bias, increase in collector-base voltage widens collector-base space-charge layer, thus reducing base width resulting in collector current increase when collector voltage is increased (Early effect)

- for constant collector voltage, effect of high injection results in widening of charge-neutral base region when entire space-charge region is pushed toward heavily doped collector region decreasing transistor current gain and degrades device frequency response (Kirk effect)

1.3. BJTs and HBTs

Simplified structures of n-p-n heterojunction bipolar transistor (HBT)

AlGaAs HBT for integrated circuit made by planar process



- forward-bias emitter injection efficiency is very high since wider bandgap AlGaAs emitter injects electrons into GaAs p-base at lower energy level, but holes are prevented from flowing into emitter by high energy barrier, thus resulting in possibility to decrease base length, base-width modulation and increase frequency response

- heavily p-doped base to reduce base resistance

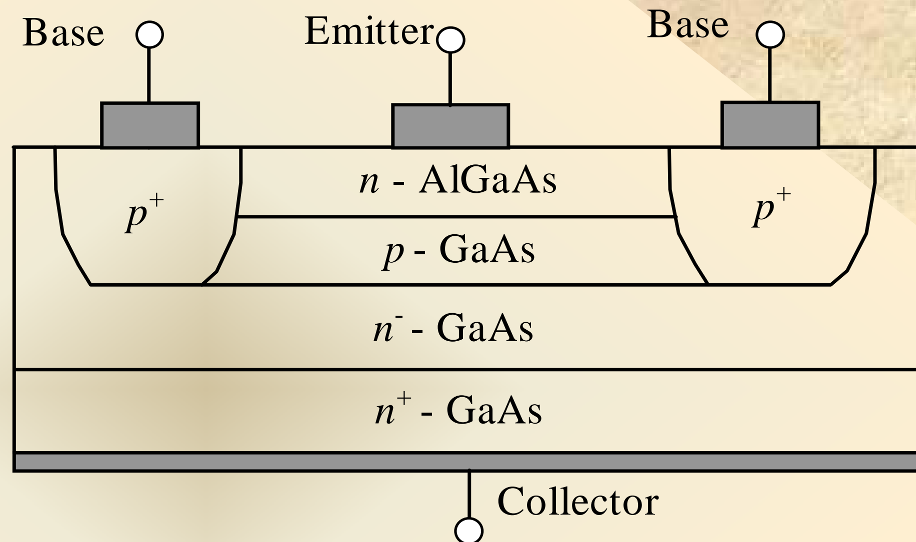
- lightly n-doped emitter to minimize emitter capacitance

- lightly n-doped collector region allows collector-base junction to sustain relatively high voltages without breaking down

1.3. BJTs and HBTs

Simplified structures of n-p-n heterojunction bipolar transistor (HBT)

Single-chip AlGaAs/GaAs HBT

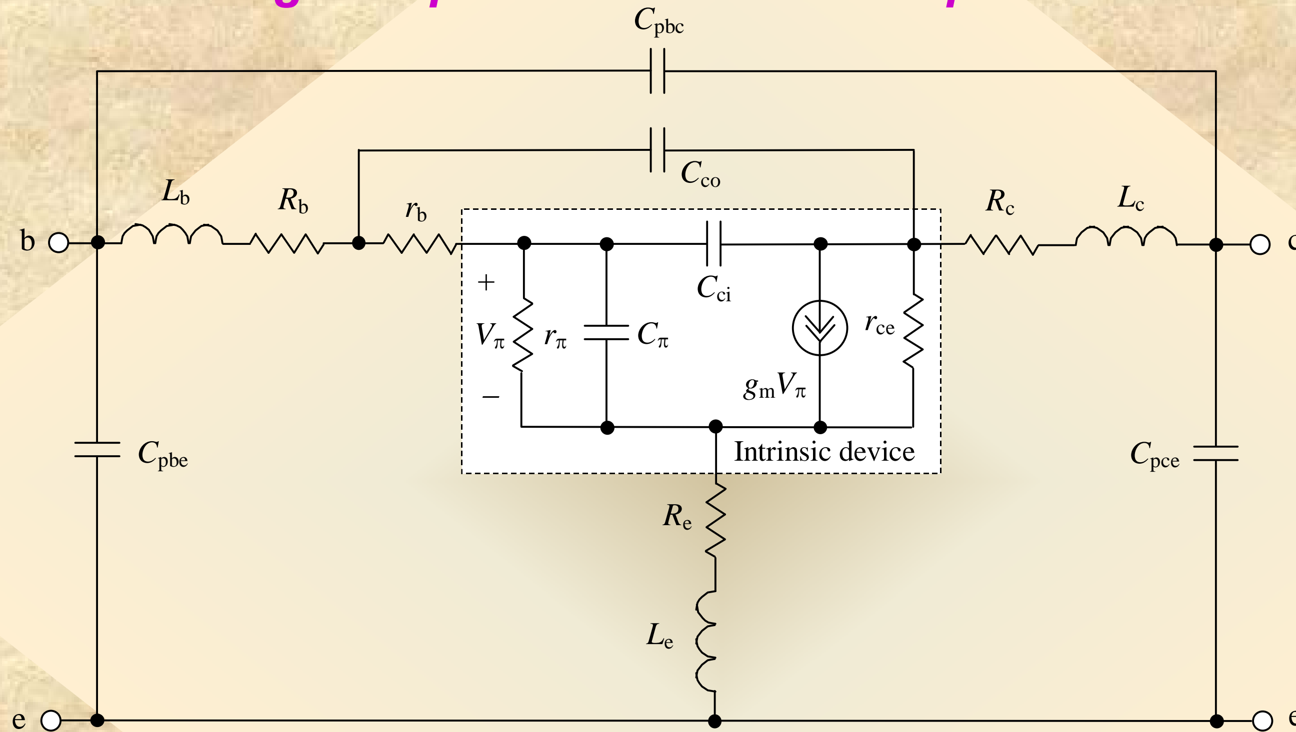


- lower 1/f noise since surface states of GaAs no longer contribute significant noise to emitter current

- using wide bandgap InGaP layer instead of AlGaAs results in improvement of device performance over temperature

1.3. BJTs and HBTs

Small-signal equivalent π-circuit of bipolar transistor



- intrinsic dynamic resistance r_π and charging capacitance C_π represent base-emitter diode p-n junction

- feedback capacitance C_{co} is extrinsic and capacitance C_{ci} is intrinsic representing base-collector junction capacitance having significant effect on device performance

- intrinsic collector-emitter resistance r_{ce} models Early effect

1.3. BJTs and HBTs

Determination of equivalent circuit parameters

To determine intrinsic circuit parameters, it is best to use Y-parameters for intrinsic device:

$$Y_{11} = \frac{1}{r_\pi} + j\omega\left(C_\pi + C_{ci}\right) \qquad Y_{12} = -\, j\omega C_{ci}$$

$$Y_{21} = g_m \exp\left(-j\omega\tau_\pi\right) + j\omega C_{ci} \qquad Y_{22} = \frac{1}{r_{ce}} + j\omega C_{ci}$$

where τ_π - effective transit time

From real and imaginary parts of intrinsic Y-parameters:

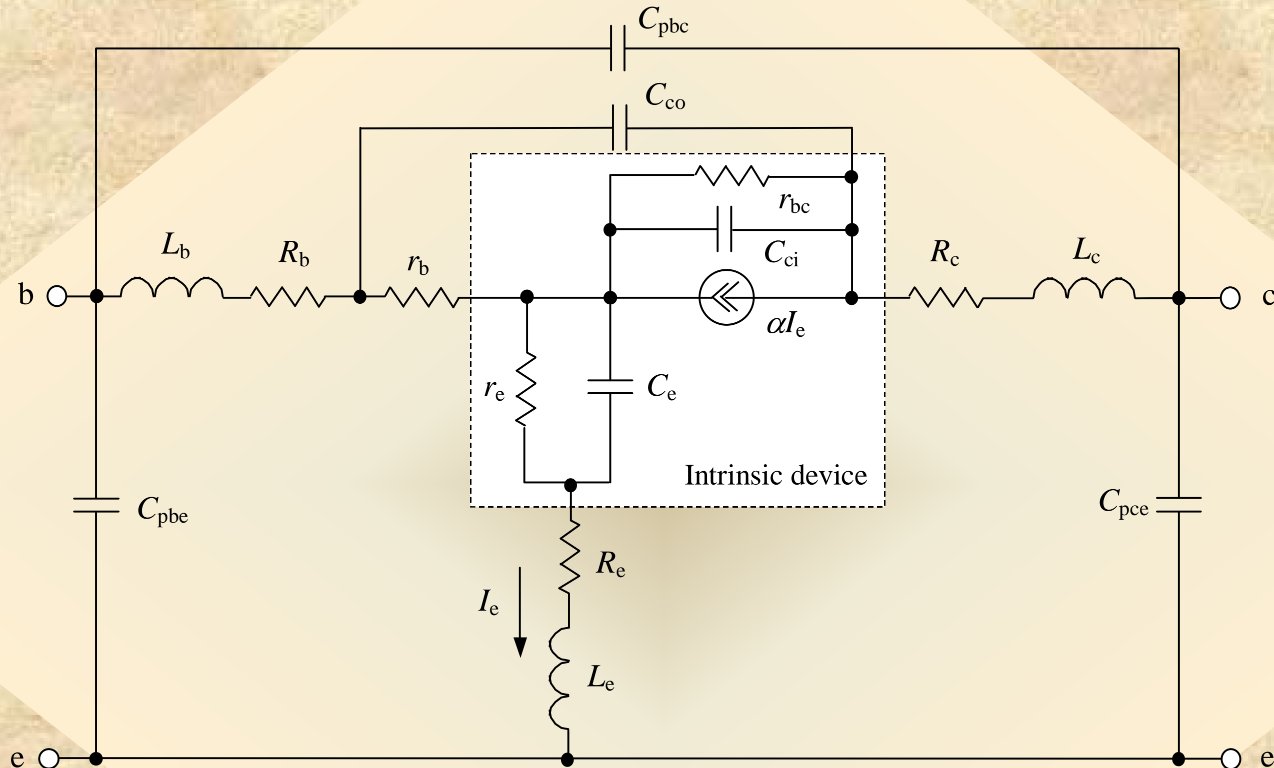
$$C_\pi = \frac{\mathrm{Im}\left(Y_{11} + Y_{12}\right)}{\omega} \qquad r_\pi = \frac{1}{\mathrm{Re}\,Y_{11}} \qquad C_{ci} = -\frac{\mathrm{Im}\,Y_{12}}{\omega}$$

$$\tau_\pi = \frac{1}{\omega}\cos^{-1}\frac{\mathrm{Re}\,Y_{21} + \mathrm{Re}\,Y_{12}}{\sqrt{\left(\mathrm{Re}\,Y_{21}\right)^2 + \left(\mathrm{Im}\,Y_{21} + \mathrm{Im}\,Y_{12}\right)^2}}$$

$$g_m = \sqrt{\left(\mathrm{Re}\,Y_{21}\right)^2 + \left(\mathrm{Im}\,Y_{21} + \mathrm{Im}\,Y_{12}\right)^2} \qquad r_{ce} = \frac{1}{\mathrm{Re}\,Y_{22}}$$

1.3. BJTs and HBTs

Small-signal equivalent T-circuit of bipolar transistor



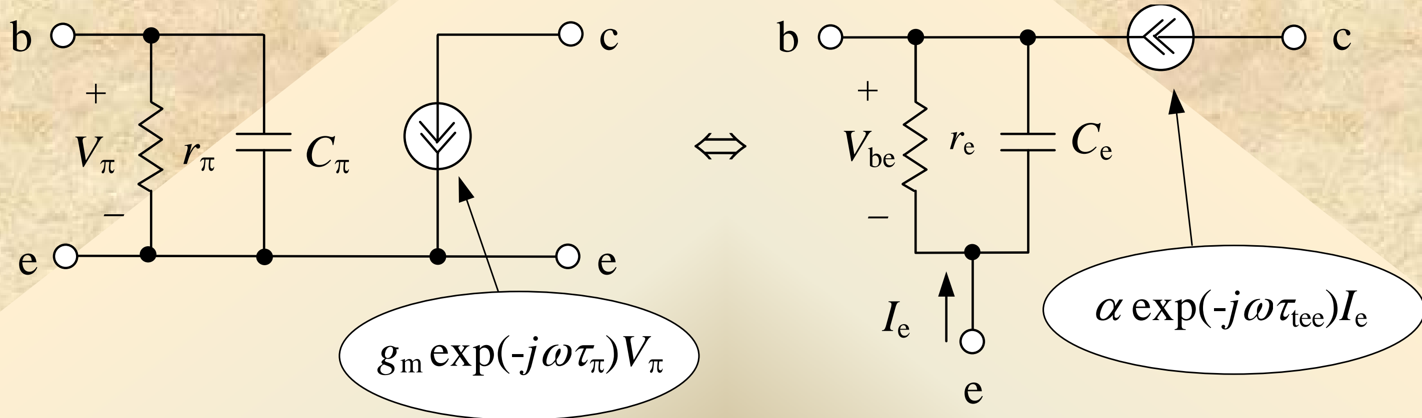
- intrinsic dynamic resistance r_e and charging capacitance C_e represent base-emitter diode p-n junction

- α is collector-to-emitter current gain

- intrinsic collector-emitter resistance r_{bc} models Early effect

1.3. BJTs and HBTs

Equivalence of intrinsic π - and T-circuit topologies



$$Y_e = \frac{I_e}{V_{be}} = \frac{1}{r_e} + j\omega C_e = \frac{1}{r_\pi} + j\omega C_\pi + g_m \exp(-j\omega\tau_\pi)$$ - equal admittances

$$\alpha \exp(-j\omega\tau_{tee}) I_e = g_m \exp(-j\omega\tau_\pi) V_\pi$$ - equal collector currents where $\alpha = \alpha_0/(1 + j\omega\tau_\alpha)$

Relationships between circuit intrinsic parameters:

$$g_m = \alpha_0 \sqrt{(1/r_e)^2 + (\omega C_e)^2} \Big/ \sqrt{1 + (\omega\tau_\alpha)^2}$$

$$\frac{1}{r_\pi} = \frac{1}{r_e} - g_m \cos(\omega\tau_\pi)$$

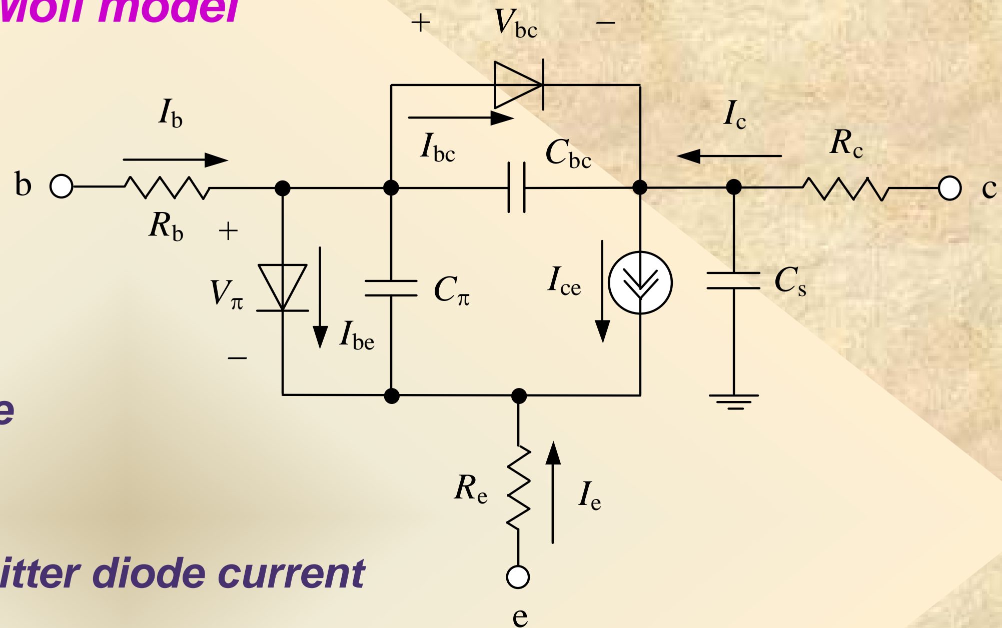
$$\tau_\pi = \tau_{tee} - \frac{1}{\omega}\left[\tan^{-1}(\omega C_e r_e) + \tan^{-1}(\omega\tau_\alpha)\right]$$

$$C_\pi = C_e - g_m \frac{\sin(\omega\tau_\pi)}{\omega}$$

1.3. BJTs and HBTs

Ebers-Moll model

Nonlinear I-V and C-V models



$$I_{ce} = I_{sat}\left[\exp\left(\frac{V_\pi}{V_T}\right) - \exp\left(\frac{V_{bc}}{V_T}\right)\right]$$

where $V_T = \dfrac{kT}{q}$ **- thermal voltage**

$$I_{be} = \frac{I_{sat}}{\beta_F}\left[\exp\left(\frac{V_\pi}{V_T}\right) - 1\right]$$ **- base-emitter diode current**

where β_F - forward current gain

$$I_{bc} = \frac{I_{sat}}{\beta_R}\left[\exp\left(\frac{V_{bc}}{V_T}\right) - 1\right]$$

- base-collector diode current

where β_R - reverse current gain

$$C_{be} = \tau_F \frac{dI_{be}}{dV_\pi} + C_{jeo}\left(1 - \frac{V_\pi}{\varphi_e}\right)^{-m_e}$$ **- base-emitter diode capacitance**

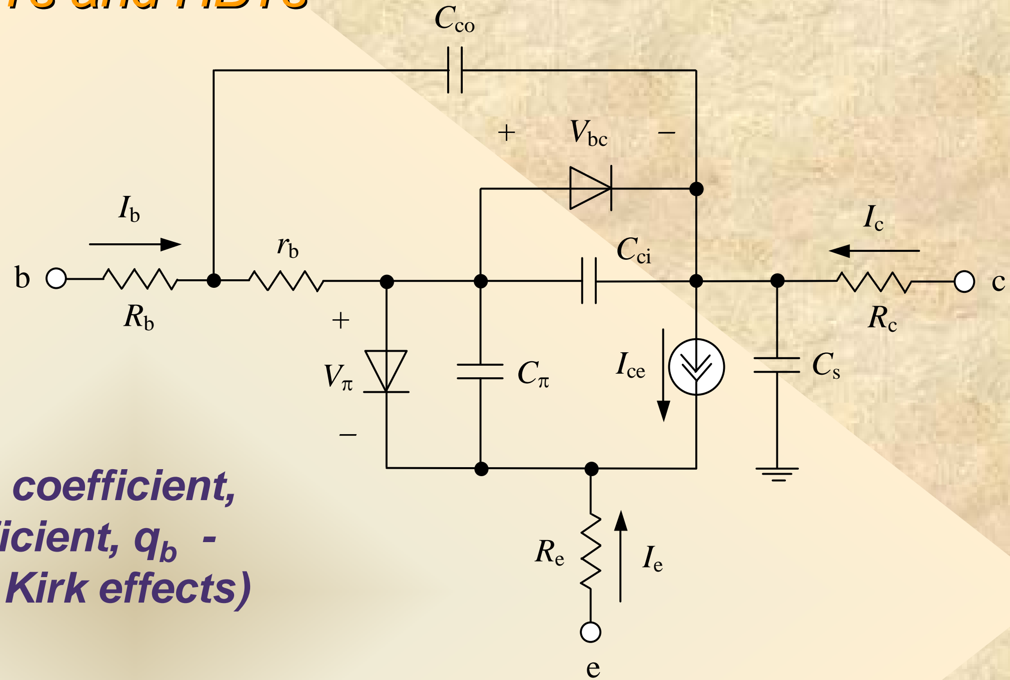
$$C_{bc} = \tau_R \frac{dI_{bc}}{dV_{bc}} + C_{jco}\left(1 - \frac{V_{bc}}{\varphi_c}\right)^{-m_c}$$ **- base-collector diode capacitance**

where τ_F - forward transit time, τ_R - reverse transit time, m_e and m_c - grading factors

1.3. BJTs and HBTs

Gummel-Poon model

Nonlinear I-V model



$$I_{ce} = \frac{I_{ss}}{q_b}\left[\exp\left(\frac{V_\pi}{n_F V_T}\right) - \exp\left(\frac{V_{bc}}{n_R V_T}\right)\right]$$

where n_F - forward current emission coefficient, n_R - reverse current emission coefficient, q_b - variable model parameter (Early and Kirk effects)

$$I_{be} = \frac{I_{sat}(0)}{\beta_{FM}(0)}\left[\exp\left(\frac{V_\pi}{n_F V_T}\right) - 1\right] + C_2 I_{sat}(0)\left[\exp\left(\frac{V_\pi}{n_{EL} V_T}\right) - 1\right]$$

- base-emitter diode current

$$I_{bc} = \frac{I_{sat}(0)}{\beta_{RM}(0)}\left[\exp\left(\frac{V_{bc}}{n_R V_T}\right) - 1\right] + C_4 I_{sat}(0)\left[\exp\left(\frac{V_{bc}}{n_{CL} V_T}\right) - 1\right]$$

- base-collector diode current

where C_2, C_4, n_{EL}, n_{CL} - model parameters responsible for low-current effects

Gummel-Poon model

Base resistance model

$$r_b = r_{bm} + 3(r_{b0} - r_{bm})\frac{\tan z - z}{z \tan^2 z}$$

where z - current-dependent model parameter

Model advantages:

- base-width modulation (Early effect)

- variation of forward current gain β_F with collector current (Kirk effect)

- better approximation of distributed structure of base-collector junction (base resistance between two capacitances)

- variation of base resistance with base current

Nonlinear C-V models

$$C_\pi = \frac{d}{dV_\pi}\left(\tau_{FF}\frac{I_{cc}}{q_b}\right) + C_{jeo}\left(1 - \frac{V_\pi}{\varphi_e}\right)^{-m_e}$$

- base-emitter diode capacitance, τ_{FF} - current-dependent transit time

$$C_{ci} = \tau_R \frac{dI_{bc}}{dV_{bc}} + k_c C_{jco}\left(1 - \frac{V_{bc}}{\varphi_c}\right)^{-m_c}$$

- base-collector diode capacitance

$$C_{co} = C_{jco}(1 - k_c)\left(1 - \frac{V_{bco}}{\varphi_c}\right)^{-m_c}$$

- junction capacitance, k_c - fraction of base-collector capacitance connected to base resistance