LECTURE 4. HIGH-EFFICIENCY POWER AMPLIFIER DESIGN

4.1. Overdriven Class B

4.2. Class F circuit design

4.3. Inverse Class F

4.4. Class E with shunt capacitance

4.5. Class E with parallel circuit

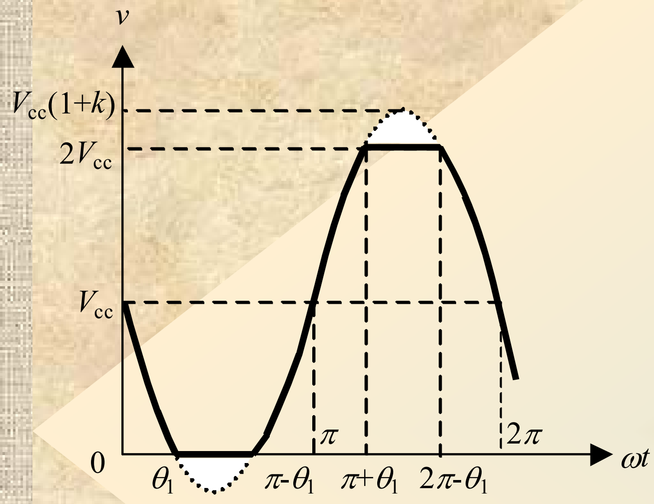
4.6. Class E with transmission lines

4.7. Broadband Class E circuit design

4.8. Practical high efficiency RF and microwave power amplifiers

4.1. Overdriven Class B

In overdriven Class B, voltage and current waveforms have increased amplitudes with the same peak values as in conventional Class B



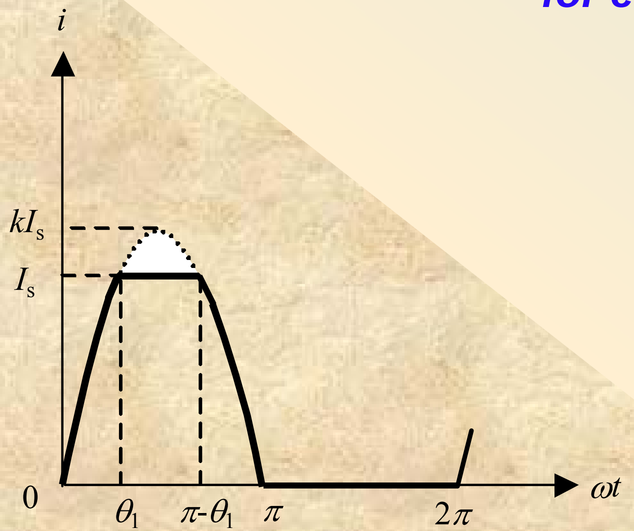
for DC voltage: $$V_0 = V_{cc}$$

for fundamental voltage : $$V_1 = \frac{2V_{cc}}{\pi}\left(\frac{\theta_1}{\sin\theta_1} + \cos\theta_1\right)$$

for odd voltage components, n = 3, 5, … :

$$V_n = \frac{2V_{cc}}{\pi}\left[\frac{\sin(\theta_1 - n\theta_1)}{(1-n)\sin\theta_1} - \frac{\sin(\theta_1 + n\theta_1)}{(1+n)\sin\theta_1} + \frac{2\cos n\theta_1}{n}\right]$$

for even voltage components, n = 2, 4, … : $$V_n = 0$$



for DC current: $$I_0 = \frac{I_s}{\pi}\left(\frac{\pi}{2} - \theta_1 + \tan\frac{\theta_1}{2}\right)$$

for fundamental current: $$I_1 = \frac{I_s}{\pi}\left(\frac{\theta_1}{\sin\theta_1} + \cos\theta_1\right)$$

for odd current components, n = 3, 5, … :

$$I_n = \frac{I_s}{\pi}\left[\frac{\sin(\theta_1 - n\theta_1)}{(1-n)\sin\theta_1} - \frac{\sin(\theta_1 + n\theta_1)}{(1+n)\sin\theta_1} + \frac{2\cos n\theta_1}{n}\right]$$

4.1. Overdriven Class B

$$P_1 = \frac{V_1 I_1}{2} = \frac{V_{cc} I_s}{\pi^2}\left(\frac{\theta_1}{\sin\theta_1} + \cos\theta_1\right)^2$$ ***- fundamental output power***

$$P_0 = V_0 I_0 = \frac{V_{cc} I_s}{\pi}\left(\frac{\pi}{2} - \theta_1 + \tan\frac{\theta_1}{2}\right)$$ ***- DC output power***

Out-of-band impedances :

$$Z_n = \frac{2V_{cc}}{I_s} = R_L, \qquad \text{for odd } n$$

$$Z_n = 0, \qquad \text{for even } n$$

where R_L is load resistance

Collector efficiency :

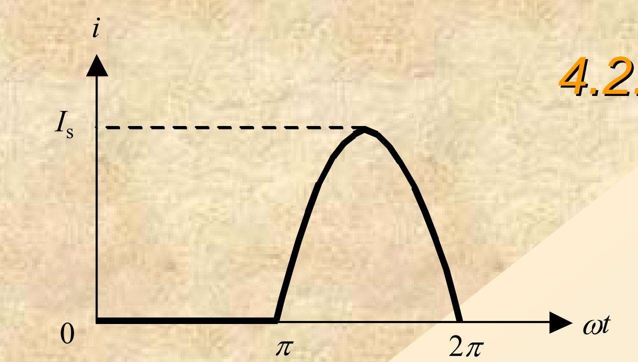
$$\eta = \frac{P_1}{P_0} = \frac{1}{\pi}\frac{\left(\frac{\theta_1}{\sin\theta_1} + \cos\theta_1\right)^2}{\frac{\pi}{2} - \theta_1 + \tan\frac{\theta_1}{2}}$$

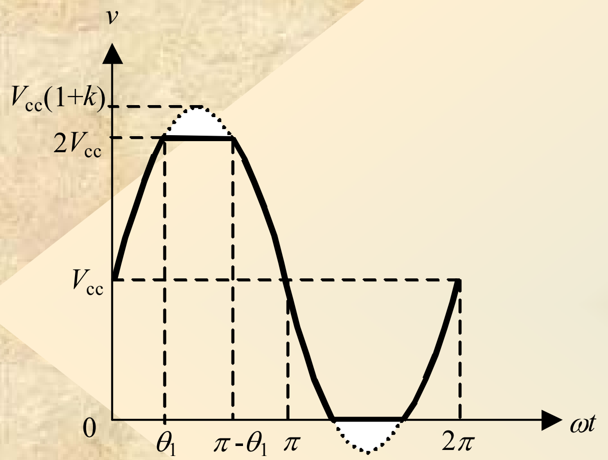
For $$\lim_{\theta_1\to 0}\frac{\theta_1}{\sin\theta_1} = \lim_{\theta_1\to 0}\frac{\theta_1'}{\sin'\theta_1} = \lim_{\theta_1\to 0}\frac{1}{\cos\theta_1} = 1 \quad \Rightarrow \quad \eta = \frac{8}{\pi^2} = 81\%$$

- maximum collector efficiency for square voltage and current waveforms

Analyzing η on extremum gives η = 88.6% for optimum angle θ_1 = 32.4°

4.2. Class F circuit design





$$I_1 = \frac{I_s}{2}$$ - *fundamental current component*

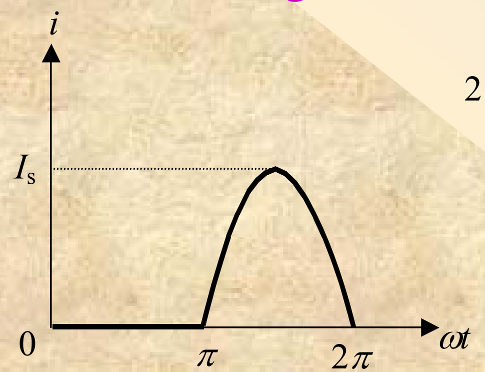
$$V_1 = \frac{4V_{cc}}{\pi}$$ - *fundamental voltage component when $\theta_1 \rightarrow 0$*

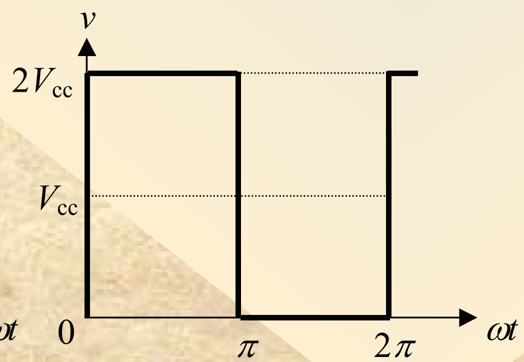
$$P_1 = \frac{V_{cc}I_s}{\pi}$$ - *fundamental output power*

$$P_0 = \frac{V_{cc}I_s}{\pi}$$ - *DC output power*

$$\eta = \frac{P_1}{P_0} = 100\%$$ - *collector efficiency*

Ideal voltage and current waveforms:

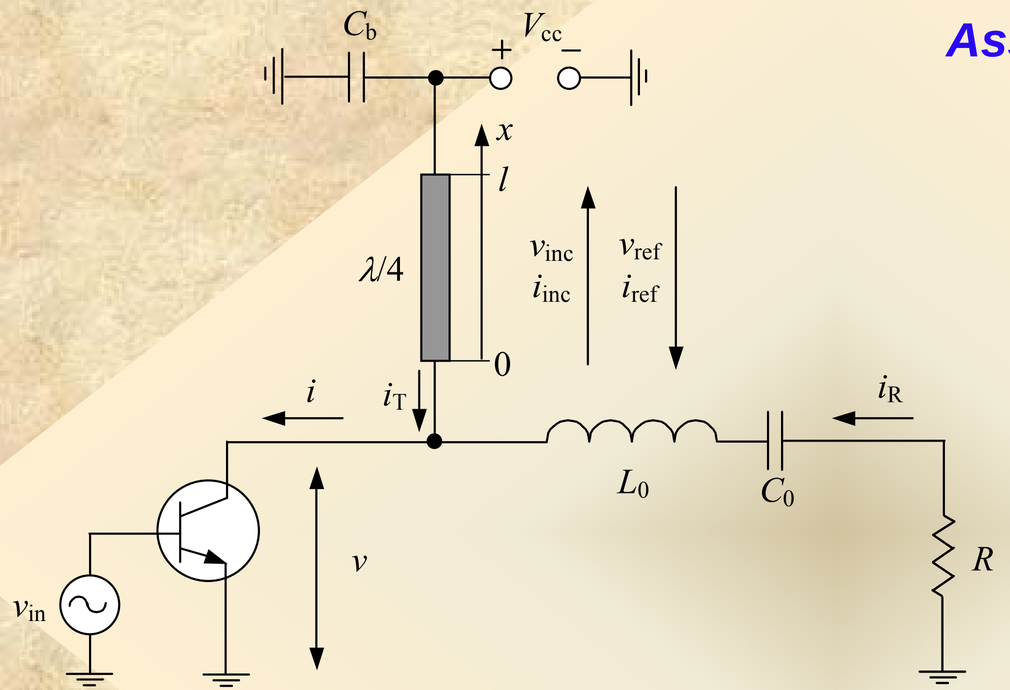




Harmonic impedance conditions:

$$\begin{cases} Z_1 = R_L = \dfrac{8}{\pi}\dfrac{V_{cc}}{I_s} \\ Z_n = 0 \quad \text{for even } n \\ Z_n = \infty \quad \text{for odd } n \end{cases}$$

4.2. Class F circuit design: quarterwave transmisssion line



Assumptions for transistor:

- ***ideal switch: no parasitic elements***
- ***half period is on, half period is off: 50% duty cycle***

Assumptions for load:

- ***purely sinusoidal current: ideal L_0C_0-circuit tuned at fundamental***

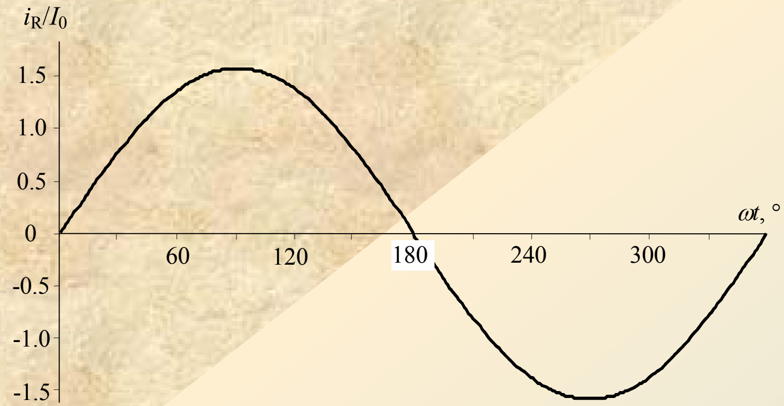
$i(\omega t) = I_R \sin\omega t$ *- load current*

$v(\omega t) = 2V_{cc} - v(\omega t + \pi)$ *- collector voltage*

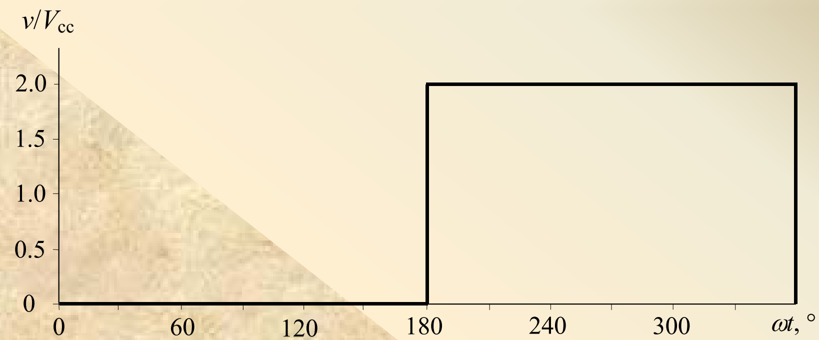
$i_T(\omega t) = i_T(\omega t + \pi) = I_R \left|\sin\omega t\right|$ *- transmission-line current*

$i(\omega t) = I_R(\sin\omega t + \left|\sin\omega t\right|)$ *- collector current*

4.2. Class F circuit design: quarterwave transmission line

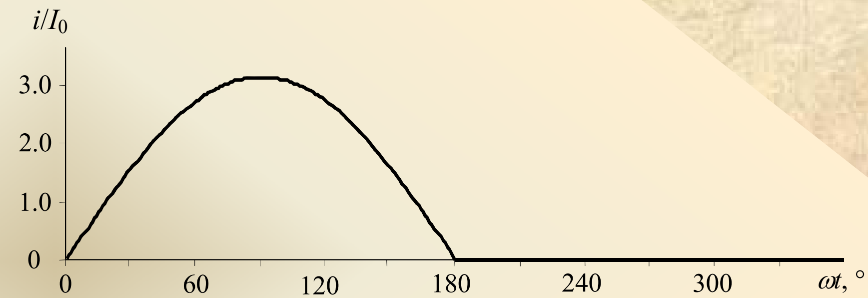


sinusoidal load current

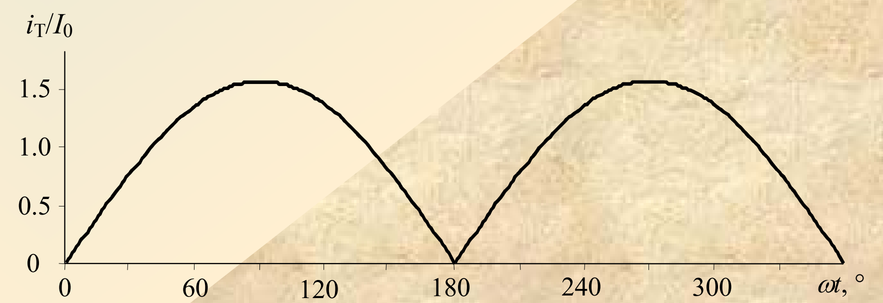


rectangular collector voltage

collector current consisting of fundamental and even harmonics



transmission-line current consisting of even harmonics



4.2. Class F circuit design

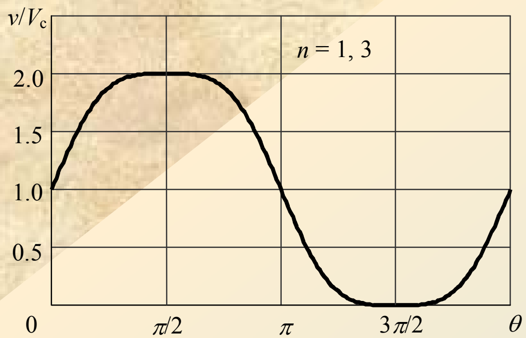
For maximally flat waveforms:

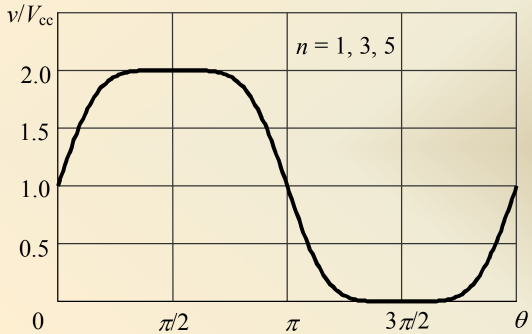
collector voltage

optimum values:

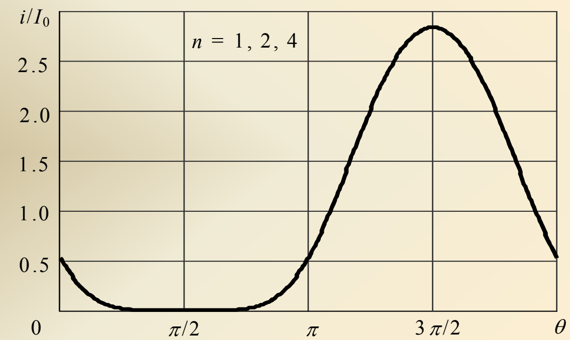
$$V_1 = \frac{9}{8} V_{cc}$$

$$V_3 = \frac{1}{8} V_{cc}$$





collector current



optimum values:

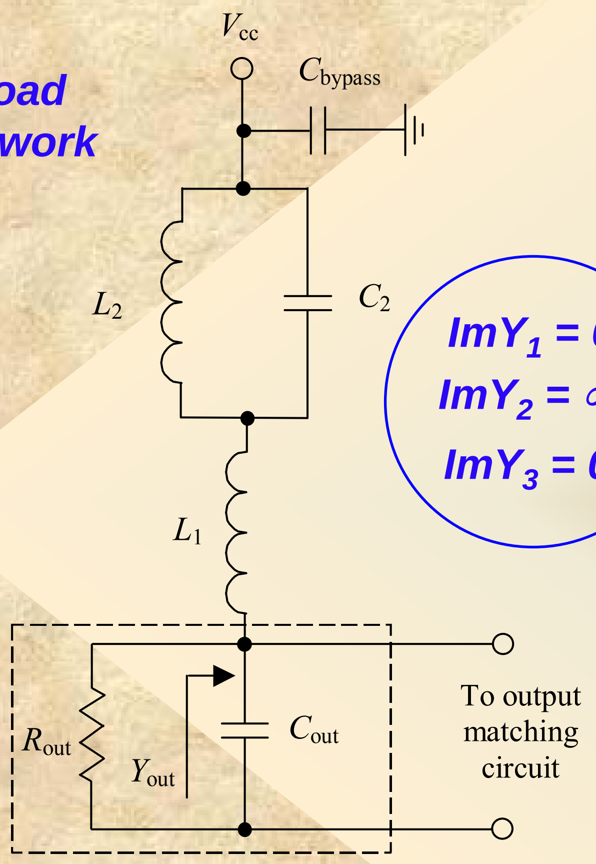
$$I_1 = \frac{4}{3} I_0$$

$$I_2 = \frac{1}{3} I_0$$

Current harmonic components	Voltage harmonic components				
	1	1, 3	1, 3, 5	1, 3, 5, 7	1, 3, 5, …, ∞
1	1/2 =0.500	9/16 = 0.563	75/128 = 0.586	1225/2048 = 0.598	2/π = 0.637
1, 2	2/3 = 0.667	3/4 = 0.750	25/32 = 0.781	1225/1536 = 0.798	8/3π = 0.849
1, 2, 4	32/45 = 0.711	4/5 = 0.800	5/6 = 0.833	245/288 = 0.851	128/45π = 0.905
1, 2, 4, 6	128/175 = 0.731	144/175 = 0.823	6/7 = 0.857	7/8 = 0.875	512/175π = 0.931
1, 2, 4,…, ∞	π/4 = 0.785	9π/32 = 0.884	75π/256 = 0.920	1225π/4096 = 0.940	1 = 1.000

4.2. Class F circuit design: second current and third voltage harmonic peaking

Load network



$ImY_1 = 0$

$ImY_2 = \infty$

$ImY_3 = 0$

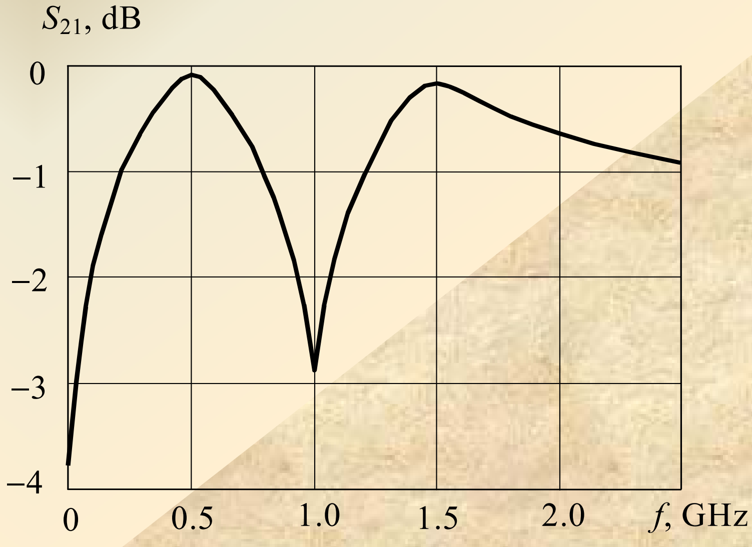
Output susceptance:

$$\mathrm{Im}(Y_{out}) = j\omega C_{out} - j\frac{1-\omega^2 L_2 C_2}{\omega L_1 \left(1-\omega^2 L_2 C_2\right) + \omega L_2}$$

Three harmonic impedance conditions:

$$\begin{cases} \left(1-\omega_0^2 L_1 C_{out}\right)\left(1-\omega_0^2 L_2 C_2\right) - \omega_0^2 L_2 C_{out} = 0, \\ L_1\left(1-4\omega_0^2 L_2 C_2\right) + L_2 = 0, \\ \left(1-9\omega_0^2 L_1 C_{out}\right)\left(1-9\omega_0^2 L_2 C_2\right) - 9\omega_0^2 L_2 C_{out} = 0, \end{cases}$$

S_{21} simulation (f_0 = 500 MHz)

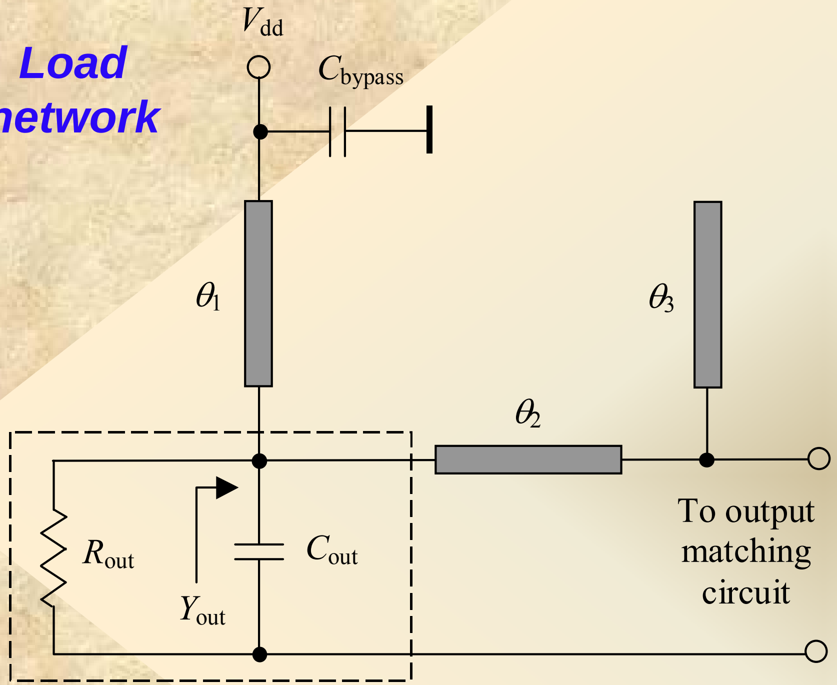


Circuit parameters

$$L_1 = \frac{1}{6\omega_o^2 C_{out}}, \quad L_2 = \frac{5}{3}L_1, \quad C_2 = \frac{12}{5}C_{out}$$

4.2. Class F circuit design: even current and third voltage harmonic peaking

Load network



Harmonic impedance conditions:

$ImY_1 = 0$

$ImY_{even} = \infty$

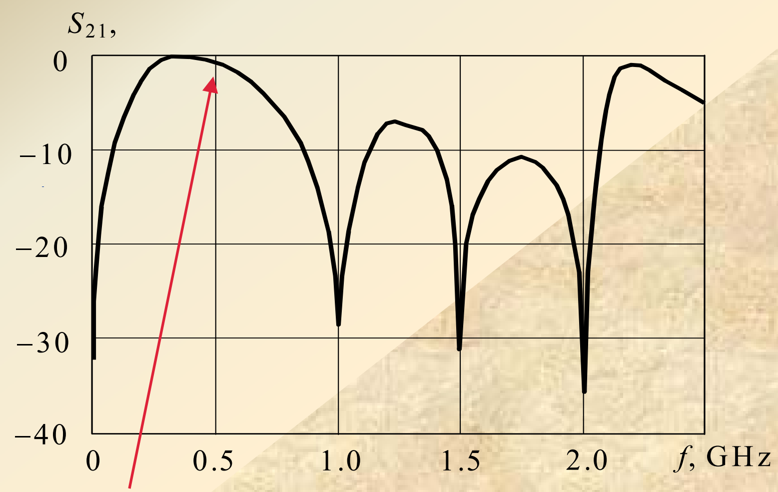
$ImY_3 = 0$

Circuit parameters:

$$\theta_1 = \frac{\pi}{2}, \quad \theta_3 = \frac{\pi}{6}$$

$$\theta_2 = \frac{1}{3}\tan^{-1}\left(\frac{1}{3Z_0\omega C_{out}}\right)$$

S_{21} simulation (f_0 = 500 MHz)

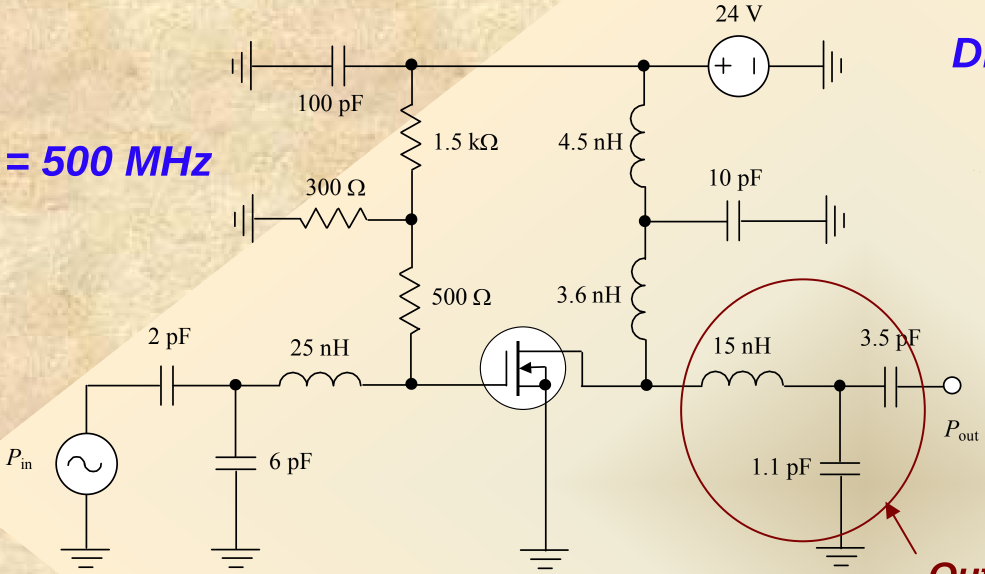


Requires additional impedance matching at fundamental

4.2. Class F circuit design

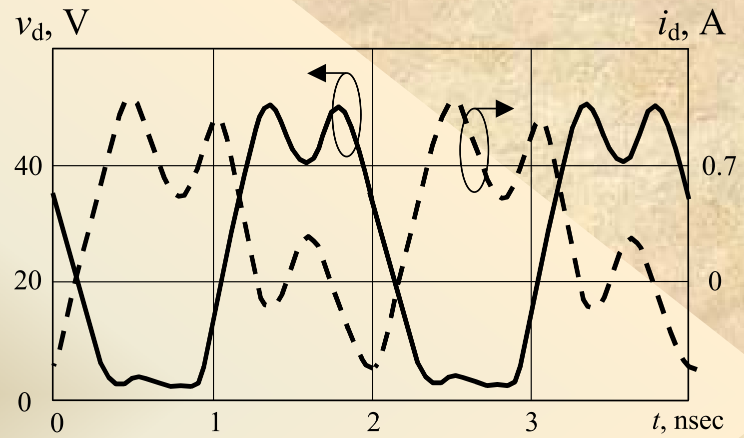
Class F power amplifier with lumped elements

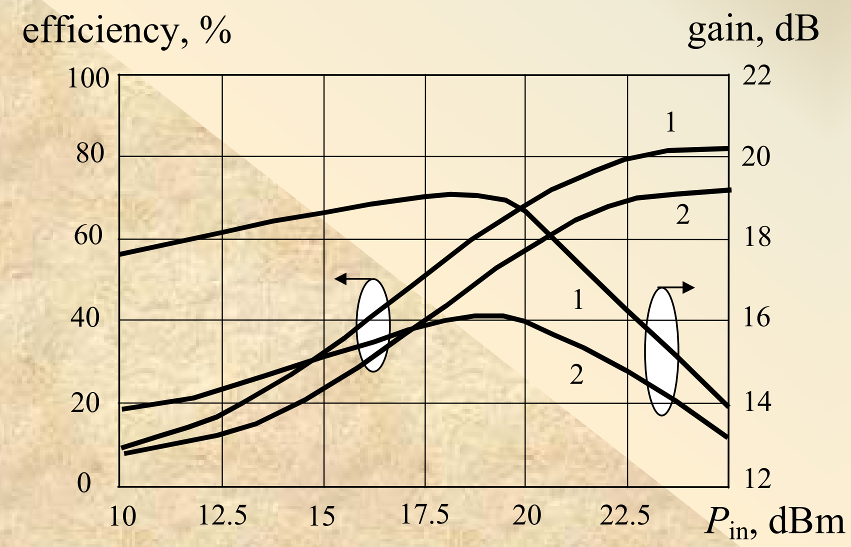
f_0 = 500 MHz



Output matching

Drain voltage and current waveforms





LDMOSFET:
gate length 1.25 um
gate width 7x1.44 mm

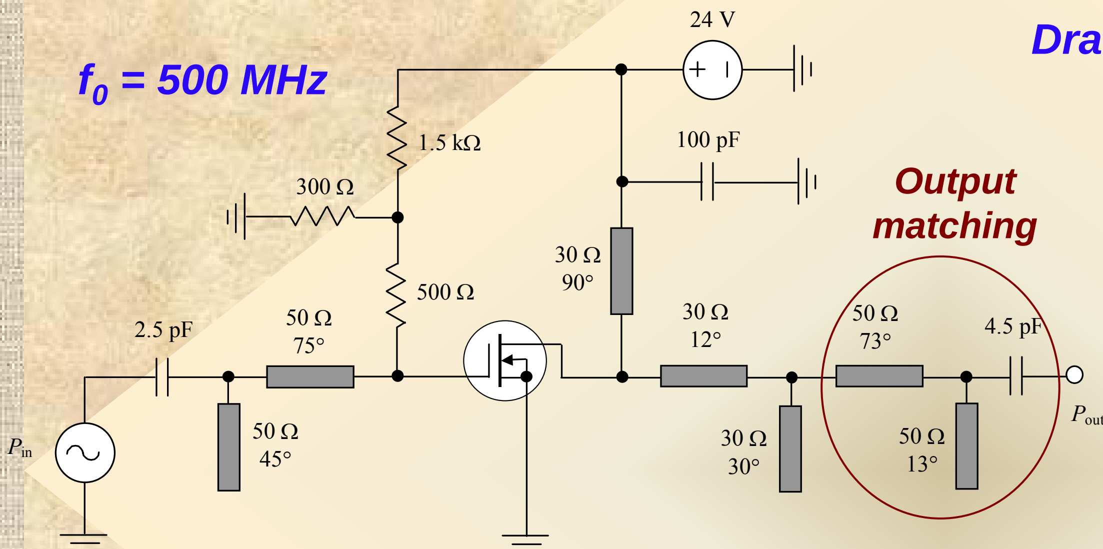
1 - inductance Q-factor = ∞
efficiency > 82%,
linear power gain > 16 dB

2 - inductance Q-factor = 30
efficiency < 71%,
linear power gain > 14 dB

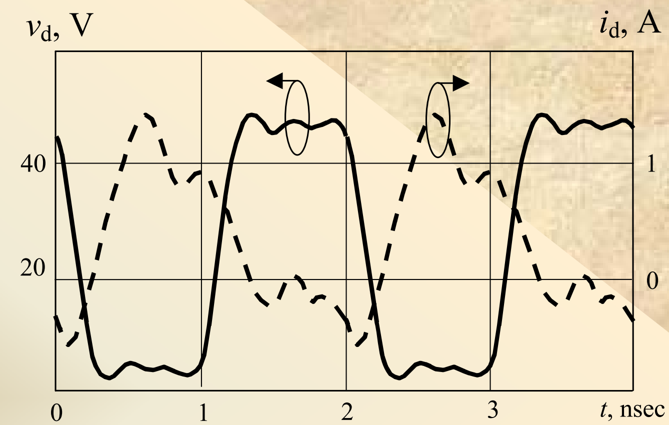
4.2. Class F circuit design

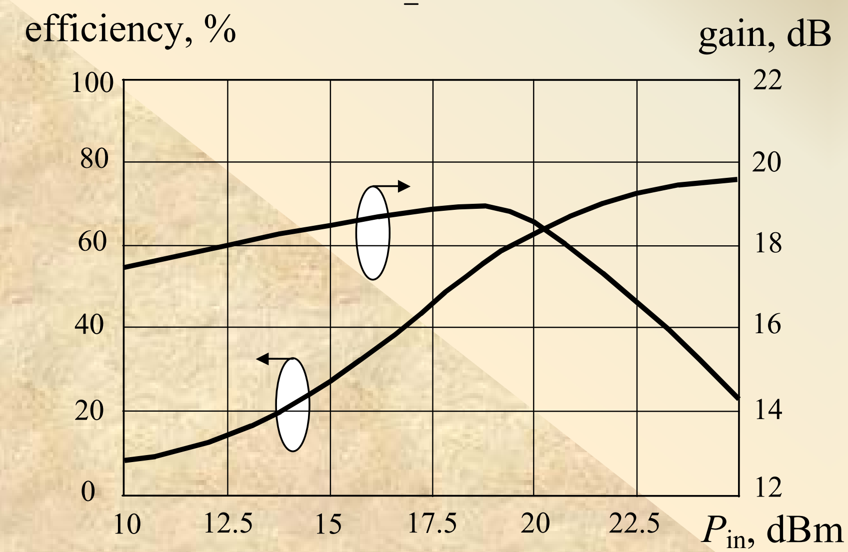
Class F power amplifier with transmission lines

f_0 = 500 MHz



Drain voltage and current waveforms





LDMOSFET:
gate length 1.25 um
gate width 7x1.44 mm

T-matching circuit for output impedance transformation

Output power - 39 dBm or 8 W

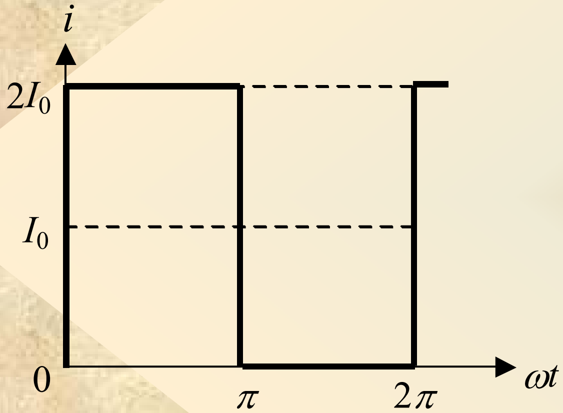
Collector efficiency - 76%

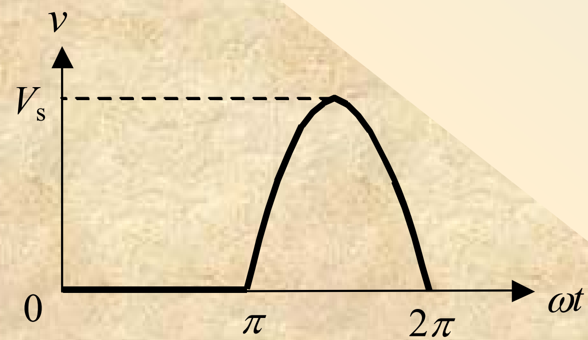
Linear power gain > 16 dB

4.3. Inverse Class F

Concept of inverse Class F mode was introduced for low voltage power amplifiers designed for monolithic applications (less collector current)

Dual to conventional Class F with mutually interchanged current and voltage waveforms





$$I_1 = \frac{4I_0}{\pi}$$ - fundamental current

$$V_1 = \frac{V_s}{2} = \frac{\pi}{2}V_{cc}$$ - fundamental voltage

$$P_1 = \frac{V_s I_0}{\pi}$$ - fundamental output power

$$P_0 = V_{cc} I_0 = \frac{V_s I_0}{\pi}$$ - DC output power

$$\eta = \frac{P_1}{P_0} = 100\%$$ - ideal collector efficiency

Harmonic impedance conditions:

$$\begin{cases} Z_1 = R_L = \dfrac{\pi}{8}\dfrac{V_s}{I_0} \\ Z_n = 0 \quad \text{for odd } n \\ Z_n = \infty \quad \text{for even } n \end{cases}$$

4.3. Inverse Class F

Optimum load resistances for different classes

Load resistance in Class B :

$$R_{\mathrm{L}}^{(\mathrm{B})} = \frac{V_{\mathrm{cc}}}{I_1}$$

Load resistance in Class F :

$$R_{\mathrm{L}}^{(\mathrm{F})} = \frac{4}{\pi}\frac{V_{\mathrm{cc}}}{I_1} = \frac{4}{\pi} R_{\mathrm{L}}^{(\mathrm{B})}$$

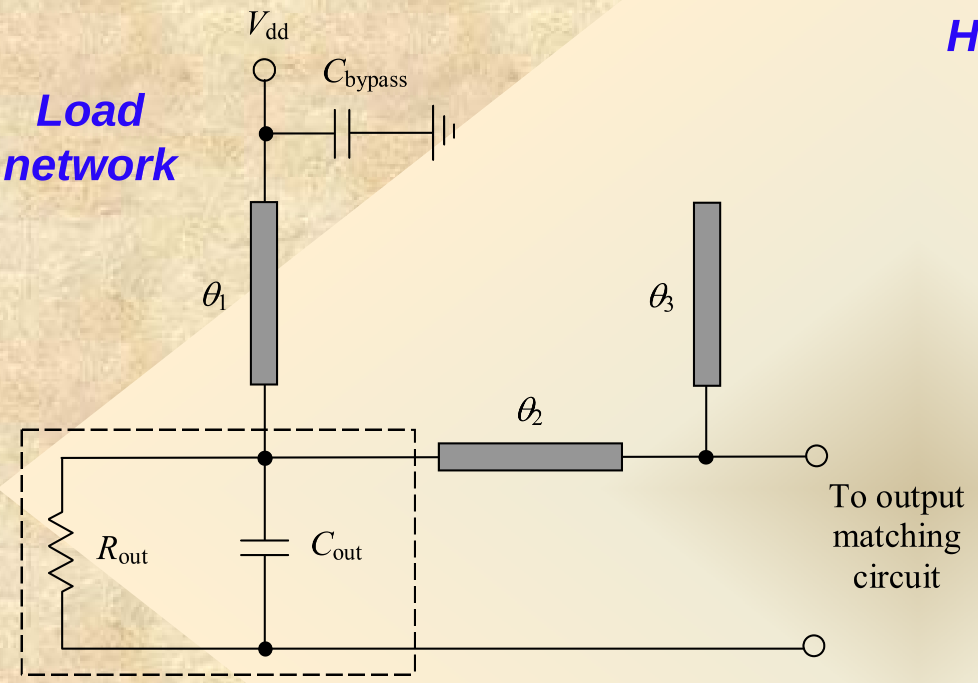
Load resistance in inverse Class F :

$$R_{\mathrm{L}}^{(\mathrm{invF})} = \frac{\pi}{2}\frac{V_{\mathrm{cc}}}{I_1} = \frac{\pi^2}{8} R_{\mathrm{L}}^{(\mathrm{F})} = \frac{\pi}{2} R_{\mathrm{L}}^{(\mathrm{B})}$$

Load resistance in inverse Class F is the highest (1.6 times larger than in Class B) → ***Less impedance transformation ratio and easier matching procedure***

4.3. Inverse Class F: second current and third voltage harmonic peaking

Load network



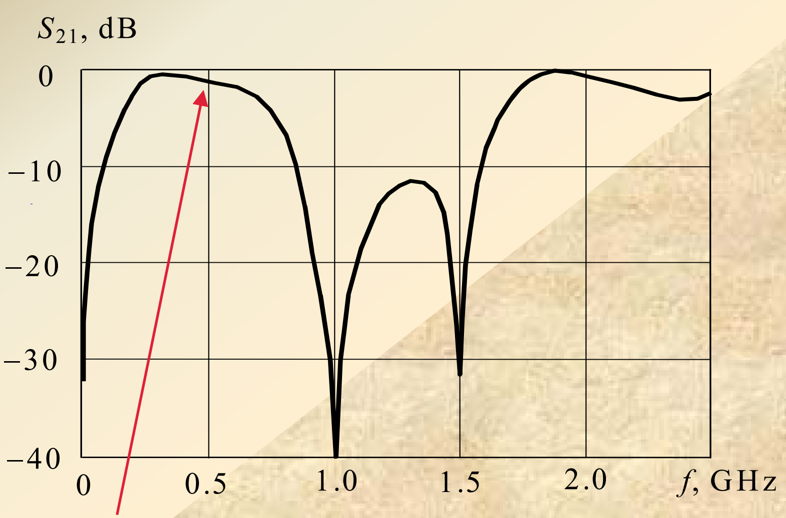
Harmonic impedance conditions:

$ImY_1 = 0$

$ImY_2 = 0$

$ImY_3 = \infty$

S_{21} simulation (f_0 = 500 MHz)



Circuit parameters:

$$\theta_1 = \frac{\pi}{3}, \qquad \theta_3 = \frac{\pi}{4}$$

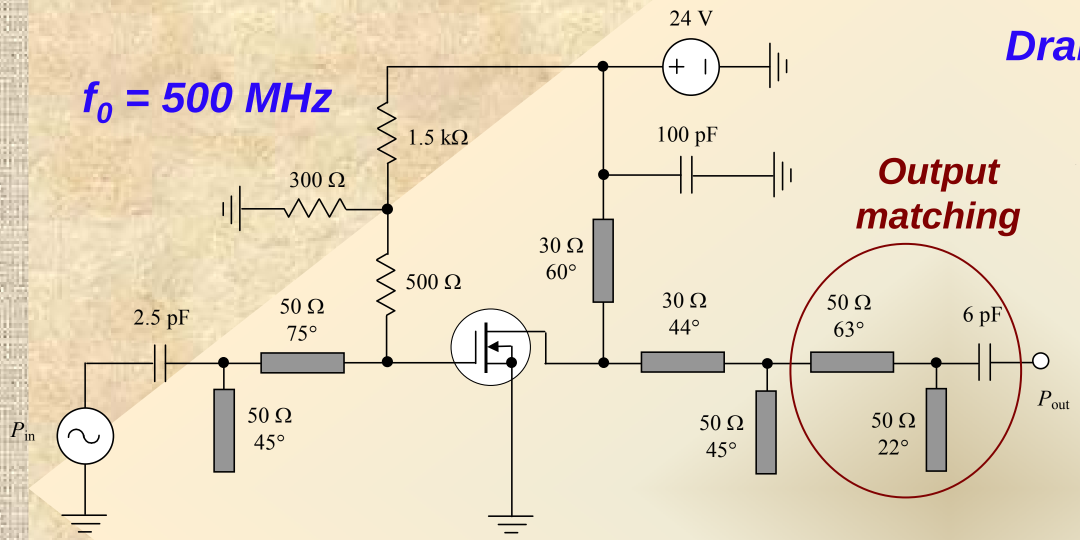
$$\theta_2 = \frac{1}{2}\tan^{-1}\left[\left(2Z_0\omega C_{out} - \frac{1}{\sqrt{3}}\right)^{-1}\right]$$

Requires additional impedance matching at fundamental

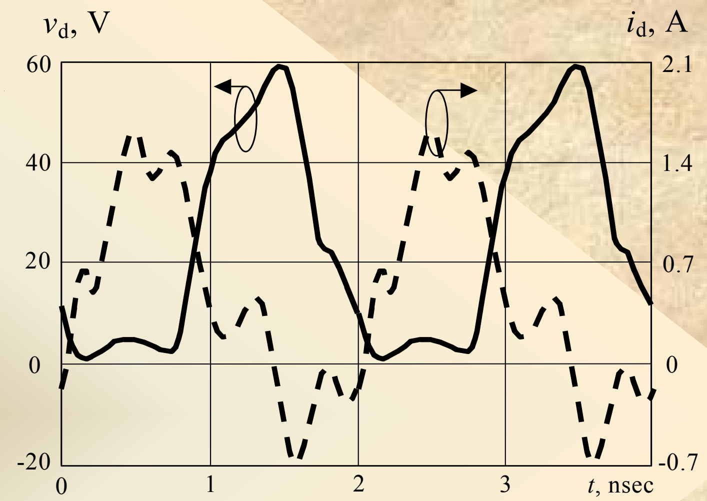
4.3. Inverse Class F

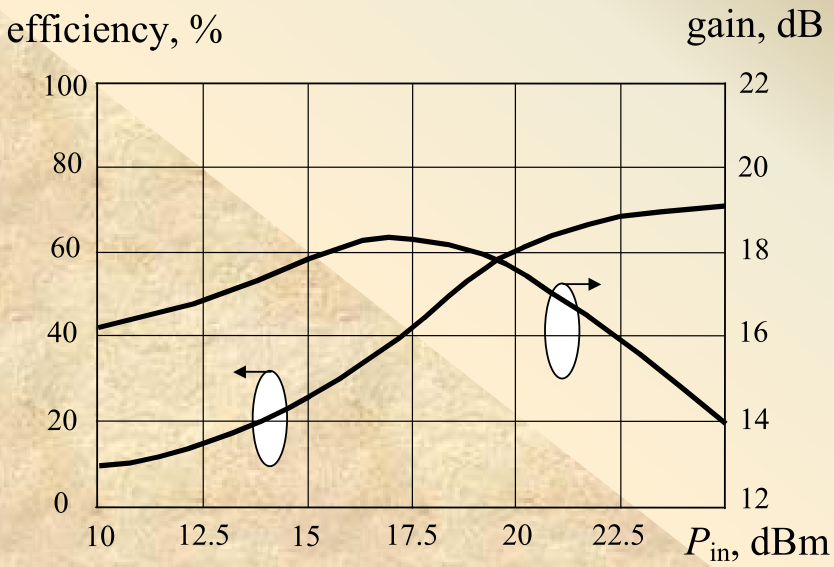
Inverse Class F power amplifier with transmission lines

f_0 = 500 MHz



Drain voltage and current waveforms





LDMOSFET:
gate length 1.25 um
gate width 7x1.44 mm

T-matching circuit for output impedance transformation

Output power - 39 dBm or 8 W

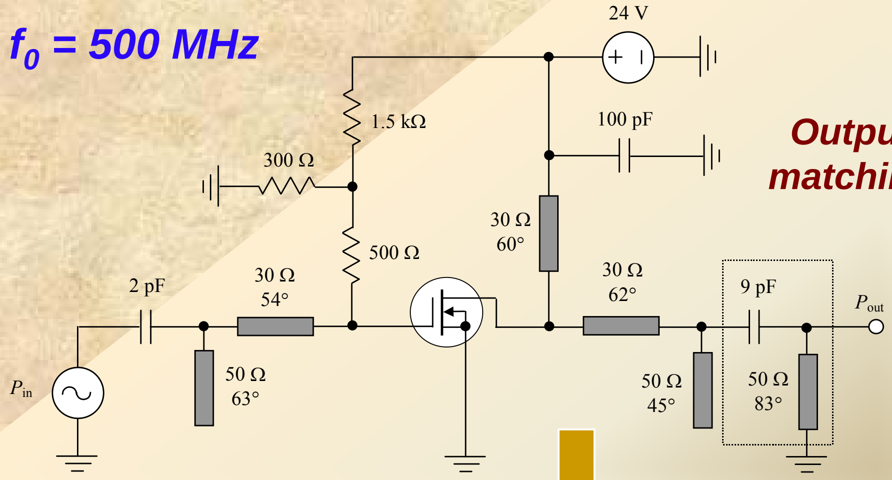
Collector efficiency - 71%

Linear power gain > 16 dB

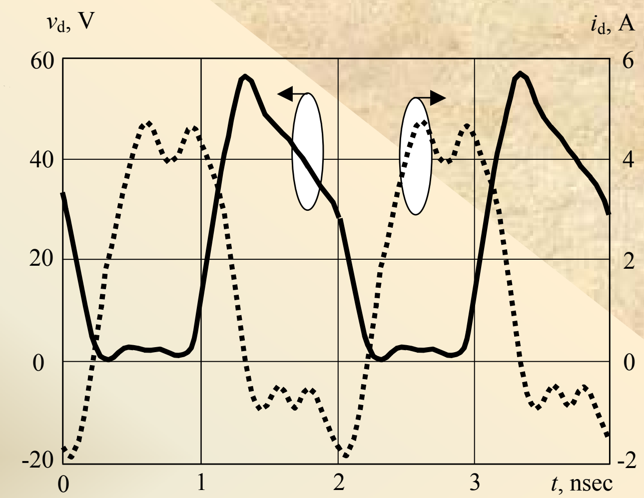
4.3. Inverse Class F

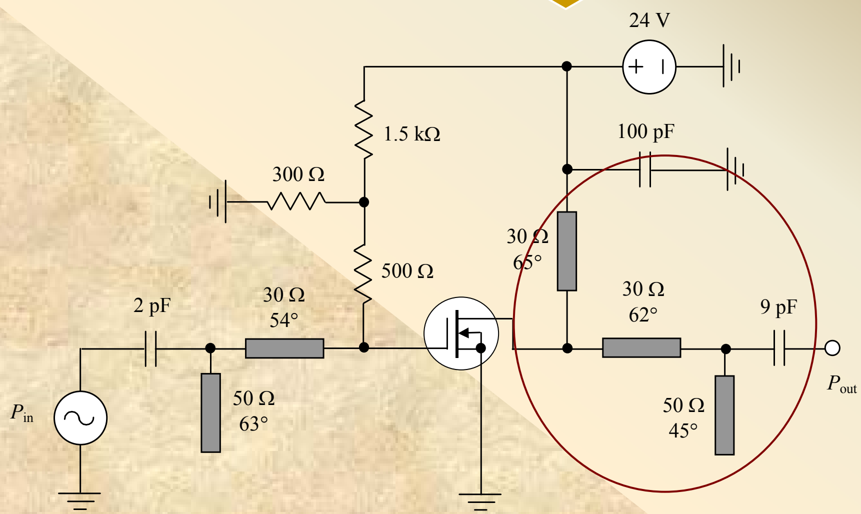
Inverse Class F power amplifier with transmission lines

f_0 = 500 MHz

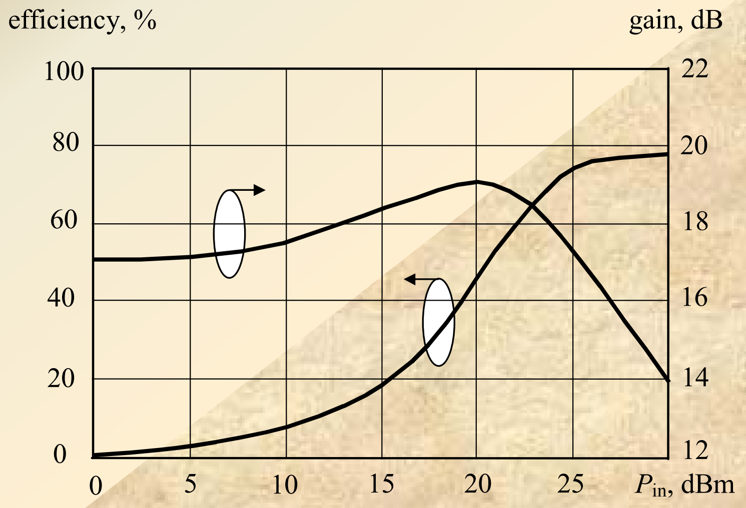


Output matching

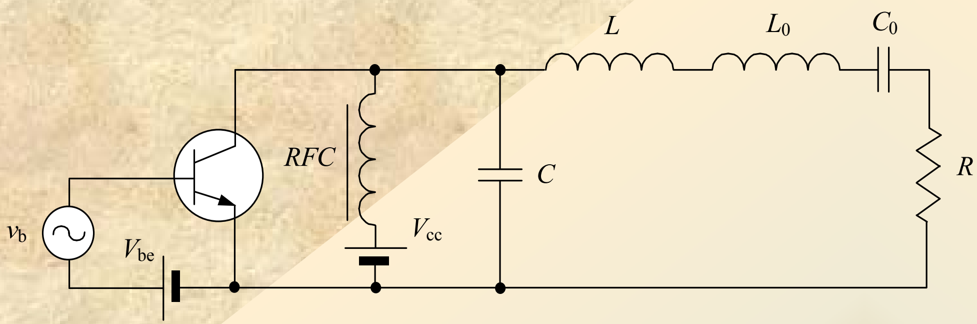




Load network with output matching



4.4. Class E with shunt capacitance



In Class E power amplifiers, transistor operates as on-to-off switch and ideal shapes of current and voltage waveforms do not overlap simultaneously resulting in 100% efficiency

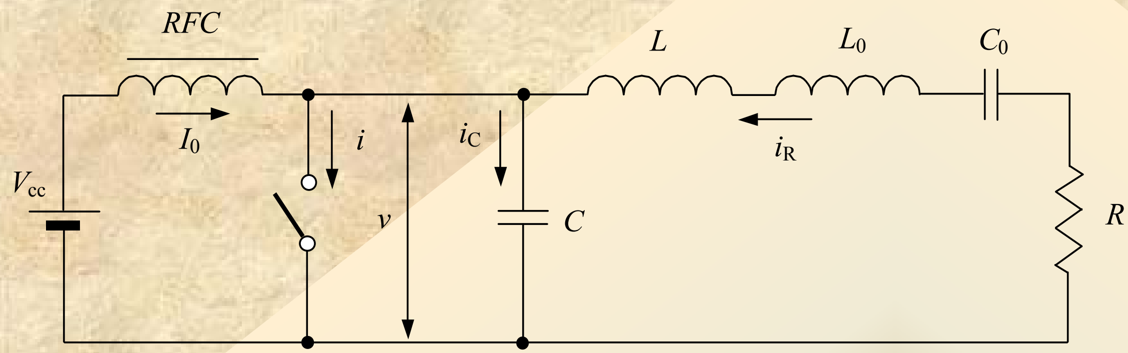
Unlike Class F power amplifiers analyzed in frequency domain as their voltage and current waveforms contain either in-phase or out-of-phase harmonics, Class E power amplifiers are analyzed in time domain as their current and voltage waveforms contain harmonics having specified different phase delays depending on load network configuration

Basic circuit of Class E power amplifier with shunt capacitance consists of series inductance L, capacitor C shunting transistor, series fundamentally tuned L_0C_0 resonant circuit, RF choke to supply DC current and load R

Shunt capacitor C can represent intrinsic device output capacitance and external circuit capacitance

Active device is considered as ideal switch to provide instantaneous device switching between its on-state and off-state operation conditions

4.4. Class E with shunt capacitance



Optimum voltage conditions across switch:

$$v(\omega t)\big|_{\omega t=2\pi} = 0$$

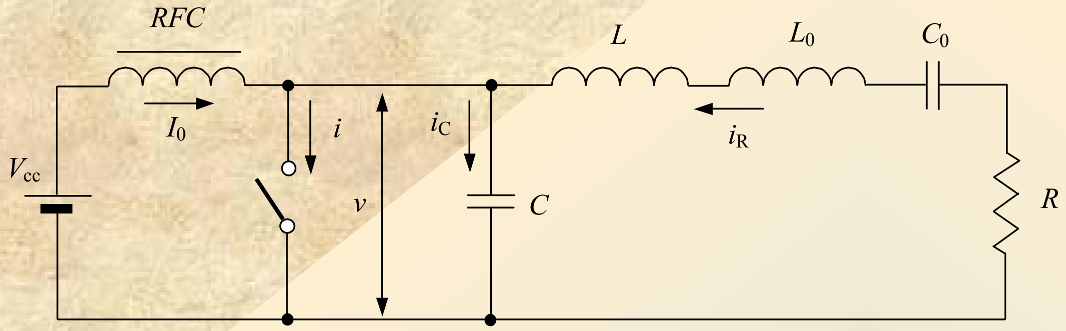
$$\left.\frac{dv(\omega t)}{d\omega t}\right|_{\omega t=2\pi} = 0$$

Idealized assumptions for analysis:

- *transistor has zero saturation voltage, zero on-resistance, infinite off-resistance and its switching action is instantaneous and lossless*
- *total shunt capacitance is assumed to be linear*
- *RF choke allows only DC current and has no resistance*
- *loaded quality factor Q_L of series fundamentally tuned resonant L_0C_0 - circuit is infinite to provide pure sinusoidal current flowing into load*
- *reactive elements in load network are lossless*
- *for optimum operation 50% duty cycle is used*

$$i_R(\omega t) = I_R \sin(\omega t + \varphi)$$ *- sinusoidal current flowing into load*

4.4. Class E with shunt capacitance



Optimum voltage conditions across switch:

$$v(\omega t)\big|_{\omega t=2\pi} = 0$$

$$\left.\frac{dv(\omega t)}{d\omega t}\right|_{\omega t=2\pi} = 0$$

$0 \le \omega t < \pi$ **- switch is on** $\Rightarrow$ $i_C(\omega t) = \omega C \dfrac{dv(\omega t)}{d\omega t} = 0$

$\Rightarrow$ $i(\omega t) = I_0 + I_R \sin(\omega t + \varphi)$ **or using initial condition** $i(0) = 0$

when $I_0 = -I_R \sin\varphi$ ➡ $$i(\omega t) = I_R\left[\sin(\omega t + \varphi) - \sin\varphi\right]$$

$\pi \le \omega t < 2\pi$ **- switch is off** $\Rightarrow$ $i(\omega t) = 0$ $\Rightarrow$ $i_C(\omega t) = I_0 + I_R \sin(\omega t + \varphi)$

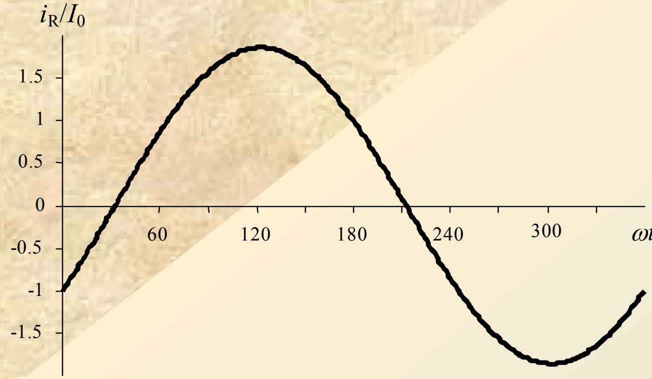
$$\Rightarrow \quad v(\omega t) = \frac{1}{\omega C}\int_{\pi}^{\omega t} i_C(\omega t)\, d\omega t = -\frac{I_R}{\omega C}\left[\cos(\omega t + \varphi) + \cos\varphi + (\omega t - \pi)\sin\varphi\right]$$

From first optimum condition: $\varphi = \tan^{-1}\left(-\dfrac{2}{\pi}\right) = -32.482^{\circ}$

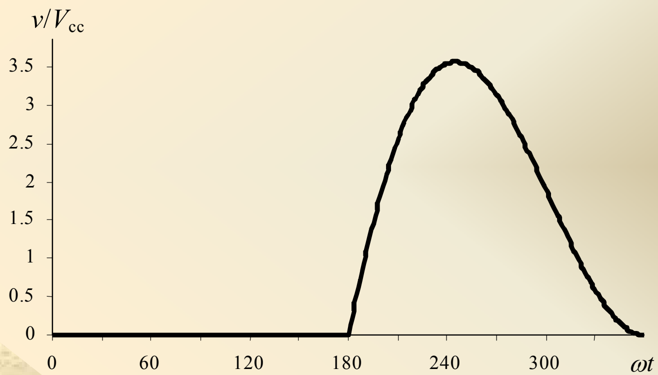
➡ $$v(\omega t) = \frac{I_0}{\omega C}\left(\omega t - \frac{3\pi}{2} - \frac{\pi}{2}\cos\omega t - \sin\omega t\right)$$

4.4. Class E with shunt capacitance

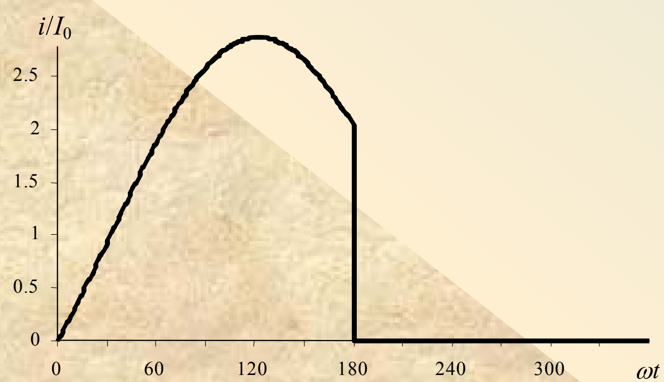
Load current



Collector voltage



Collector current



Optimum circuit parameters :

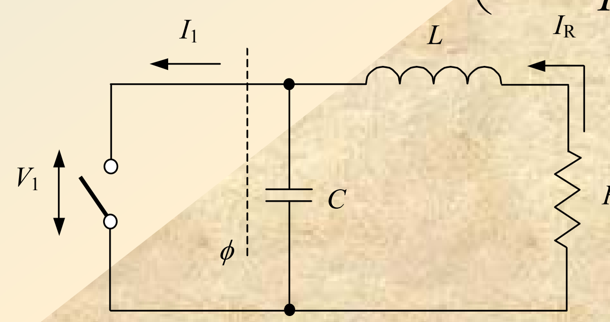
$$L = 1.1525 \frac{R}{\omega}$$ - series inductance

$$C = 0.1836 \frac{1}{\omega R}$$ - shunt capacitance

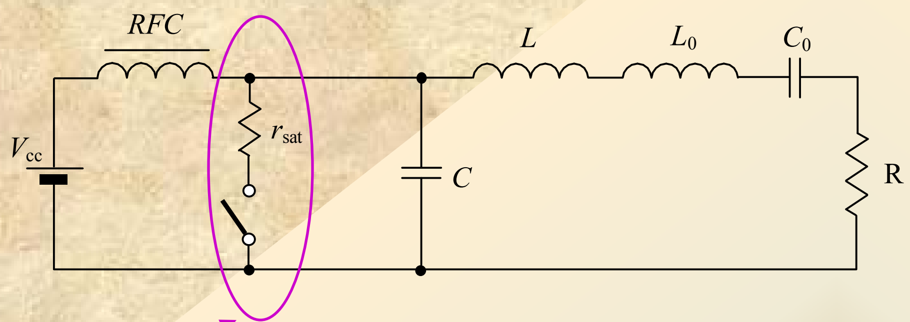
$$R = 0.5768 \frac{V_{cc}^2}{P_{out}}$$ - load resistance

Optimum phase angle at fundamental seen by switch :

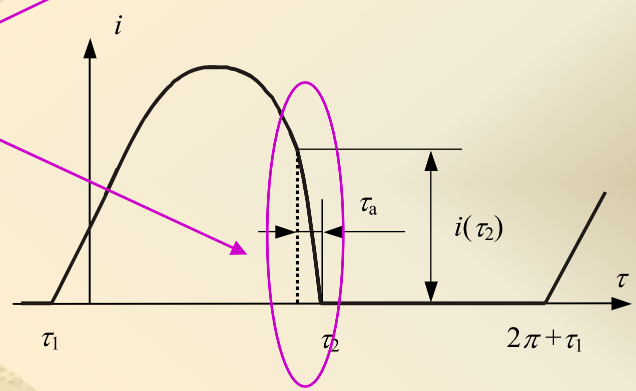
$$\phi = \tan^{-1}\left(\frac{\omega L}{R}\right) - \tan^{-1}\left(\frac{\omega CR}{1 - \frac{\omega L}{R}\omega CR}\right)$$

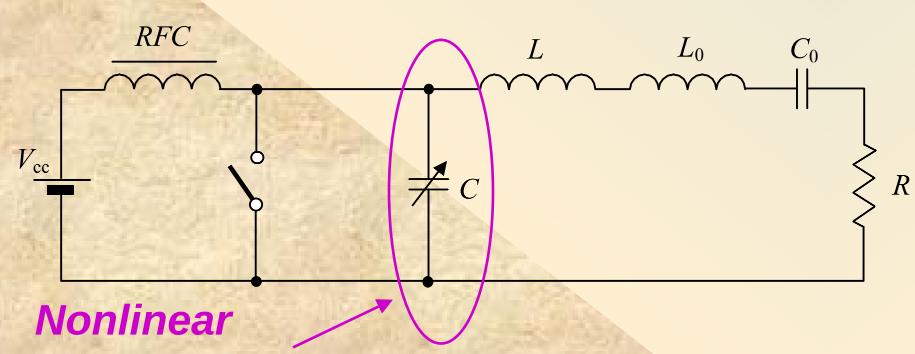


4.4. Class E with shunt capacitance



Non-ideal switch





Nonlinear capacitance

Power loss due to non-zero saturation resistance

$$P_{sat} \cong \frac{8}{3}\frac{r_{sat}P_{out}^2}{V_{cc}^2} \cong 3\frac{r_{sat}}{R}$$

Power loss due to finite switching time

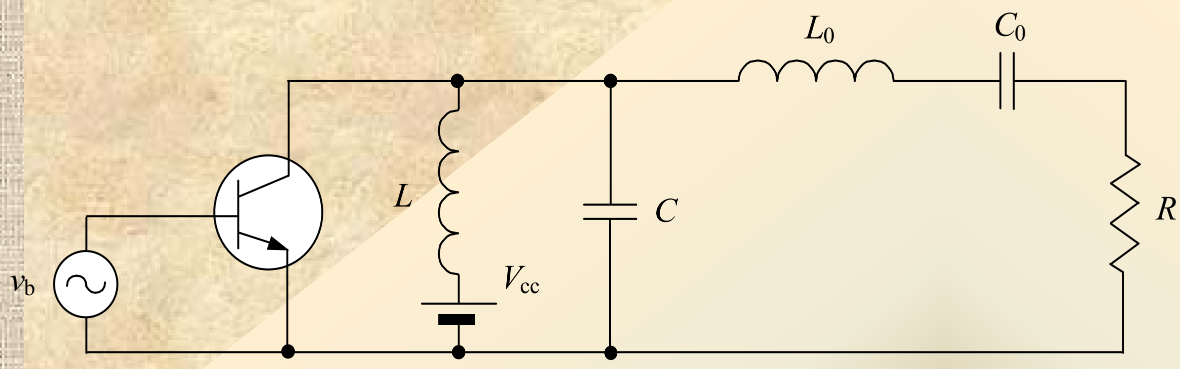
$$P_a \cong \frac{\tau_a^2}{12}$$

where $\tau_a = 0.35 \text{ or } 20°$

Only 1%

For nonlinear capacitances represented by abrupt junction collector capacitance with γ = 0.5, peak collector voltage increases by 20%

4.5. Class E with parallel circuit



Optimum voltage conditions across switch:

$$v(\omega t)\big|_{\omega t=2\pi} = 0$$

$$\left.\frac{dv(\omega t)}{d\omega t}\right|_{\omega t=2\pi} = 0$$

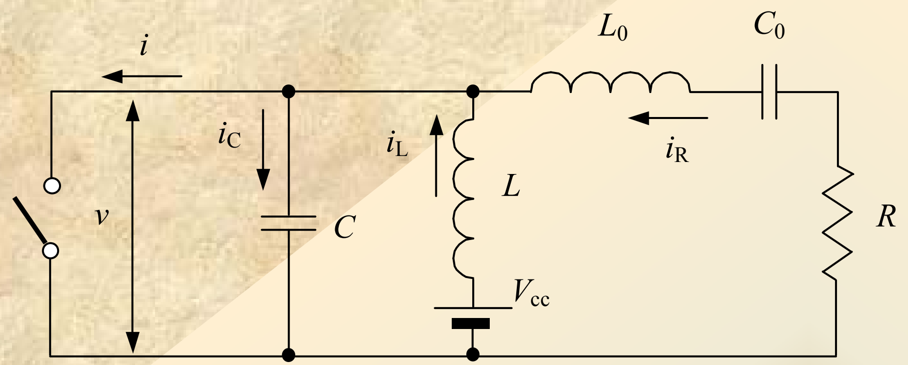
$$i_R(\omega t) = I_R \sin(\omega t + \varphi)$$ ***- sinusoidal current in load***

- ***basic circuit of Class E power amplifier with parallel circuit consists of parallel inductance L supplying also DC current, parallel capacitor C shunting transistor, series fundamentally tuned L_0C_0 resonant circuit and load R***

- ***shunt capacitor C can represent intrinsic device output capacitance and external circuit capacitance***

- ***active device is considered as ideal switch to provide instantaneous device switching between its on-state and off-state operation conditions***

4.5. Class E with parallel circuit



Optimum voltage conditions across switch:

$$v(\omega t)\big|_{\omega t = 2\pi} = 0$$

$$\left.\frac{dv(\omega t)}{d\omega t}\right|_{\omega t = 2\pi} = 0$$

$0 \le \omega t < \pi$ **- switch is on** $\Rightarrow$ $v(\omega t) = V_{cc} - v_L(\omega t) = 0$ **and** $i_C(\omega t) = \omega C \dfrac{dv(\omega t)}{d\omega t} = 0$

$$i(\omega t) = i_L(\omega t) + i_R(\omega t) = \frac{V_{cc}}{\omega L}\omega t + I_R\left[\sin(\omega t + \varphi) - \sin\varphi\right]$$

$\pi \le \omega t < 2\pi$ **- switch is off** $\Rightarrow$ $i(\omega t) = 0$ $\Rightarrow$ $i_C(\omega t) = i_L(\omega t) + i_R(\omega t)$

$$\omega C \frac{dv(\omega t)}{d(\omega t)} = \frac{1}{\omega L}\int_{\pi}^{\omega t}\left[V_{cc} - v(\omega t)\right]d(\omega t) + i_L(\pi) + I_R\sin(\omega t + \varphi)$$

under initial conditions $v(\pi) = 0$ **and** $i_L(\pi) = \dfrac{V_{cc}\pi}{\omega L} - I_R\sin\varphi$

4.5. Class E with parallel circuit

$$\omega^2 LC \frac{d^2 v(\omega t)}{d(\omega t)^2} + v(\omega t) - V_{cc} - \omega L I_R \cos(\omega t + \varphi) = 0$$

- second-order differential equation

$$\frac{v(\omega t)}{V_{cc}} = C_1 \cos(q\omega t) + C_2 \sin(q\omega t) + 1 - \frac{q^2 p}{1 - q^2} \cos(\omega t + \varphi)$$

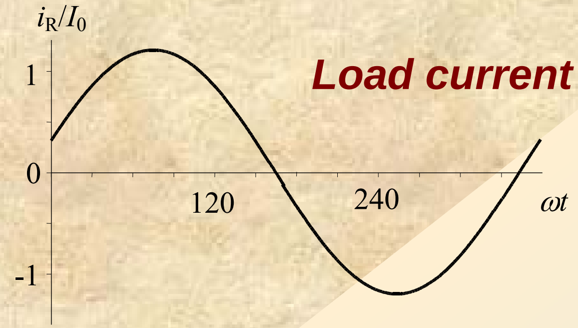
where $q = 1/\omega\sqrt{LC}, \quad p = \frac{\omega L I_R}{V_{cc}}$ ***and coefficients C_1 and C_2 are defined from initial conditions***

To define three unknown parameters q, φ and p, two optimum conditions and third equation for DC Fourier component are applied resulting to system of three algebraic equations:

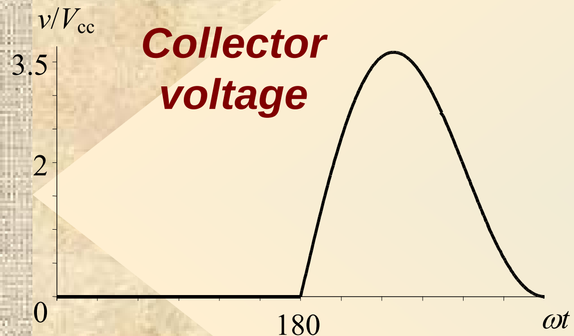
$$v(\omega t)\big|_{\omega t = 2\pi} = 0 \qquad \left.\frac{dv(\omega t)}{d\omega t}\right|_{\omega t = 2\pi} = 0 \qquad V_{cc} = \frac{1}{2\pi}\int_0^{2\pi} v(\omega t)\, d\omega t$$

$$q = 1.412 \qquad \varphi = 15.155° \qquad p = 1.21$$

4.5. Class E with parallel circuit

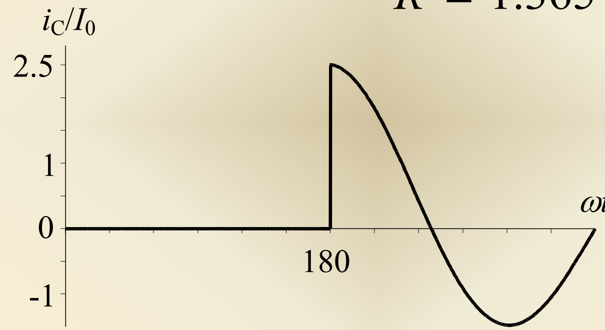


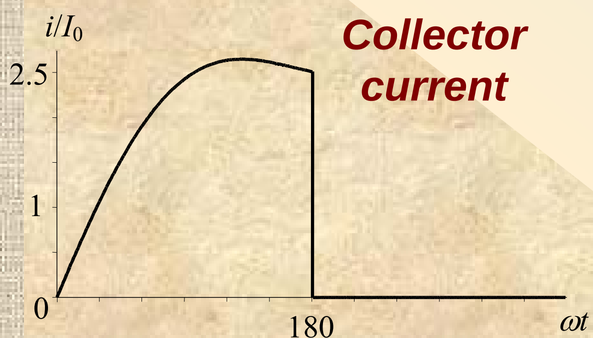
Load current



Collector voltage

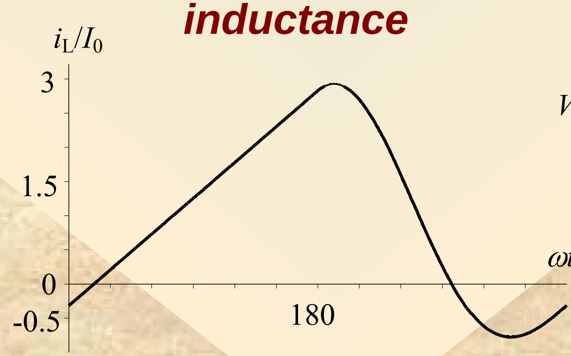
Current through capacitance





Collector current

Current through inductance



Optimum circuit parameters :

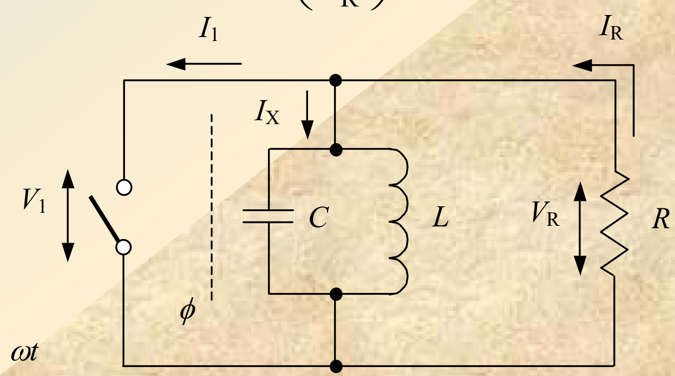
$$L = 0.732\frac{R}{\omega}$$ - parallel inductance

$$C = \frac{0.685}{\omega R}$$ - parallel capacitance

$$R = 1.365\frac{V_{cc}^2}{P_{out}}$$ - load resistance

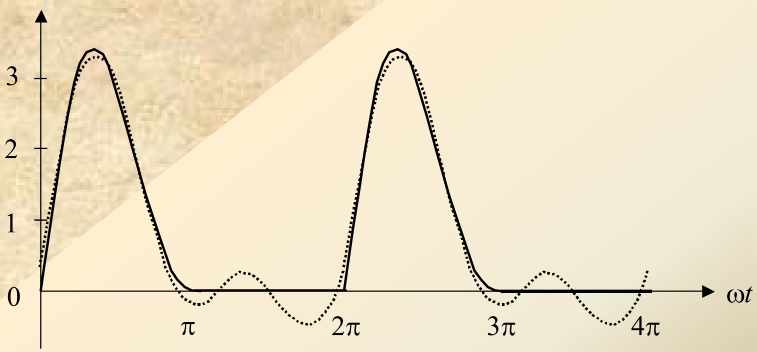
Optimum phase angle at fundamental seen by switch :

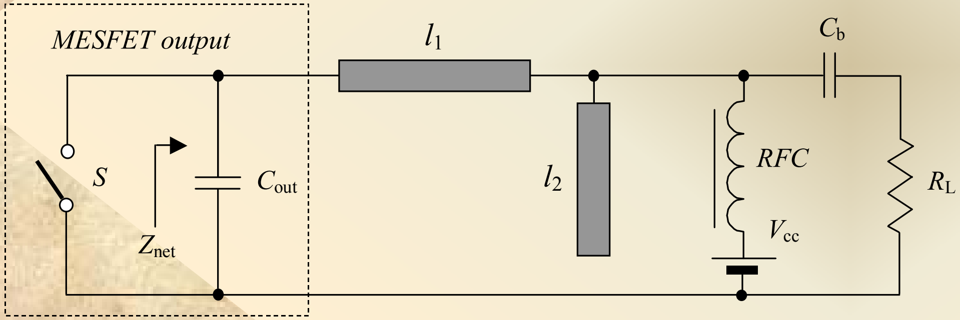
$$\phi = \tan^{-1}\left(\frac{I_X}{I_R}\right) = 34.244°$$

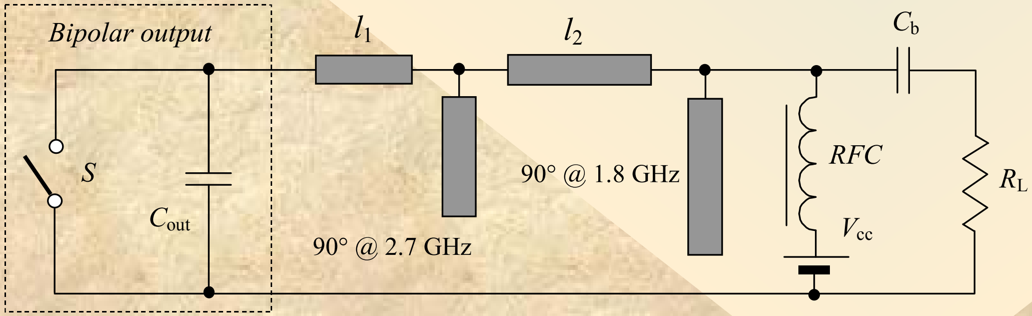


4.6. Class E with transmission lines: approximation

Two-harmonic collector voltage approximation







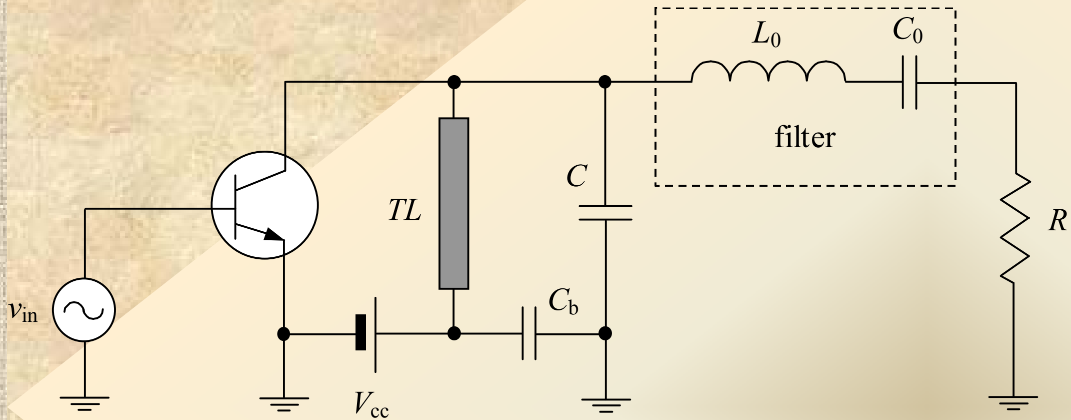
Optimum impedance at fundamental seen by device :

$$Z_{\mathrm{net1}} = R\left(1 + j\tan 49.052^{\circ}\right)$$

- ***electrical lengths of transmission lines l_1 and l_2 should be of 45° to provide open circuit seen by device at second harmonic***
- ***their characteristic impedances are chosen to provide optimum inductive impedance seen by device at fundamental***
- ***for three harmonic approximation, additional open circuit transmission line stub with 90-degree electrical length at third harmonic is required (1.5 GHz, 1.5 W, 90%)***

4.6. Class E with transmission lines: approximation

Transmission-line Class E power amplifier with parallel circuit



Optimum impedance at fundamental seen by device :

$$Z_{net1} = R / \left(1 - j\tan 34.244^{\circ}\right)$$

Parallel inductance is replaced by transmission line providing optimum inductive reactance at fundamental :

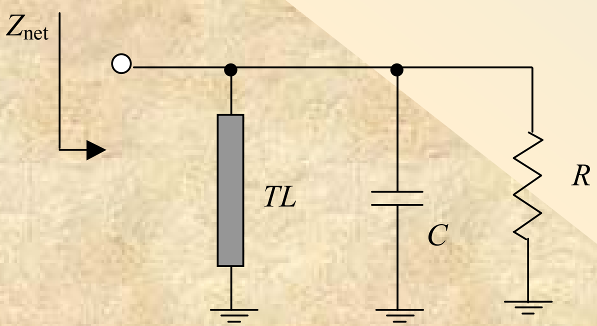
$$Z_0 \tan\theta = \omega L$$

where $L = 0.732 \dfrac{R}{\omega}$

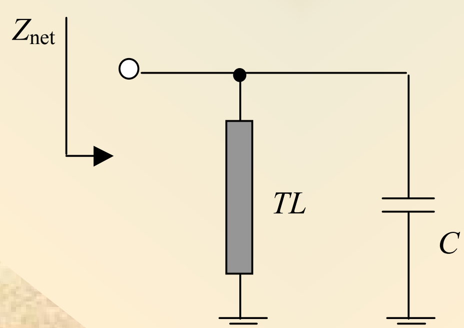
Relationship between optimum transmission line and load parameters :

$$\tan\theta = 0.732 \frac{R}{Z_0}$$

Impedance seen by device at fundamental

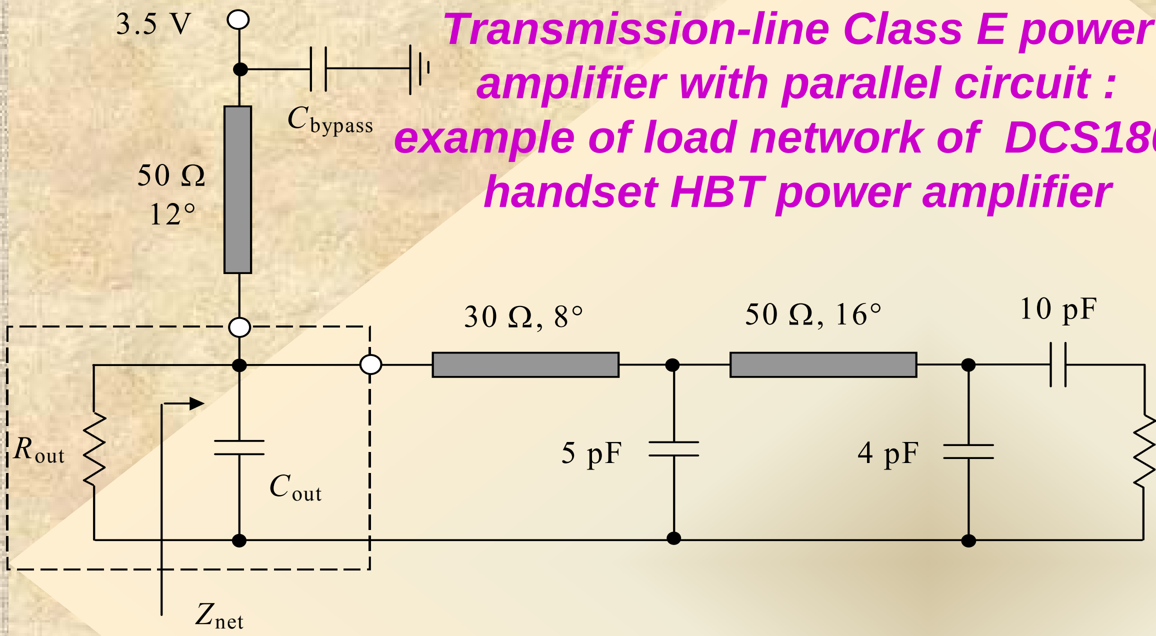


Impedance seen by device at harmonics

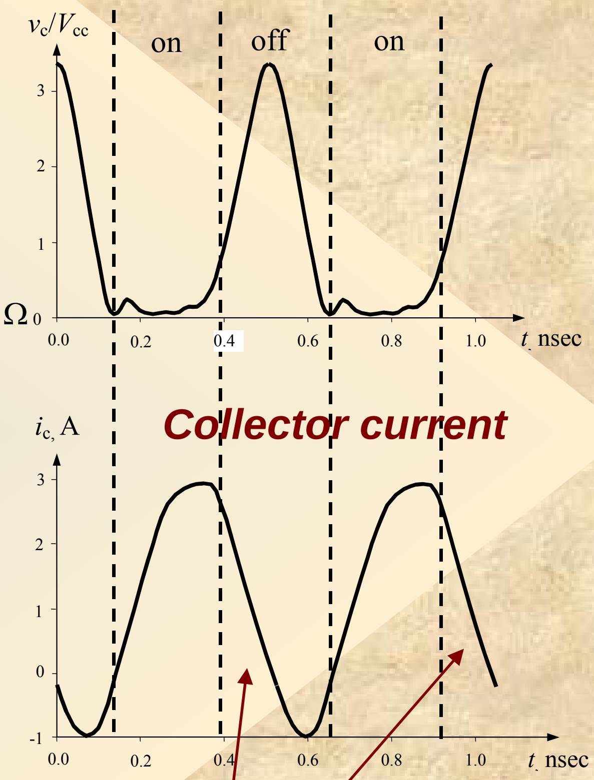


4.6. Class E with transmission lines: approximation

Transmission-line Class E power amplifier with parallel circuit : example of load network of DCS1800 handset HBT power amplifier

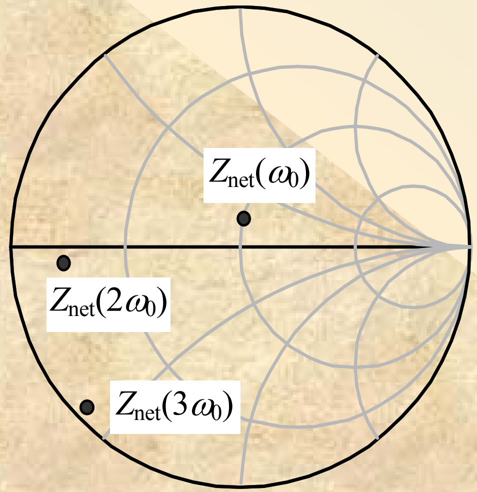


Collector voltage



Collector current

- *parameters of parallel transmission line is chosen to realize optimum inductive impedance at fundamental*



- *output matching circuit consisting of series microstrip line with two parallel capacitances should provide capacitive reactances at second and third harmonics*

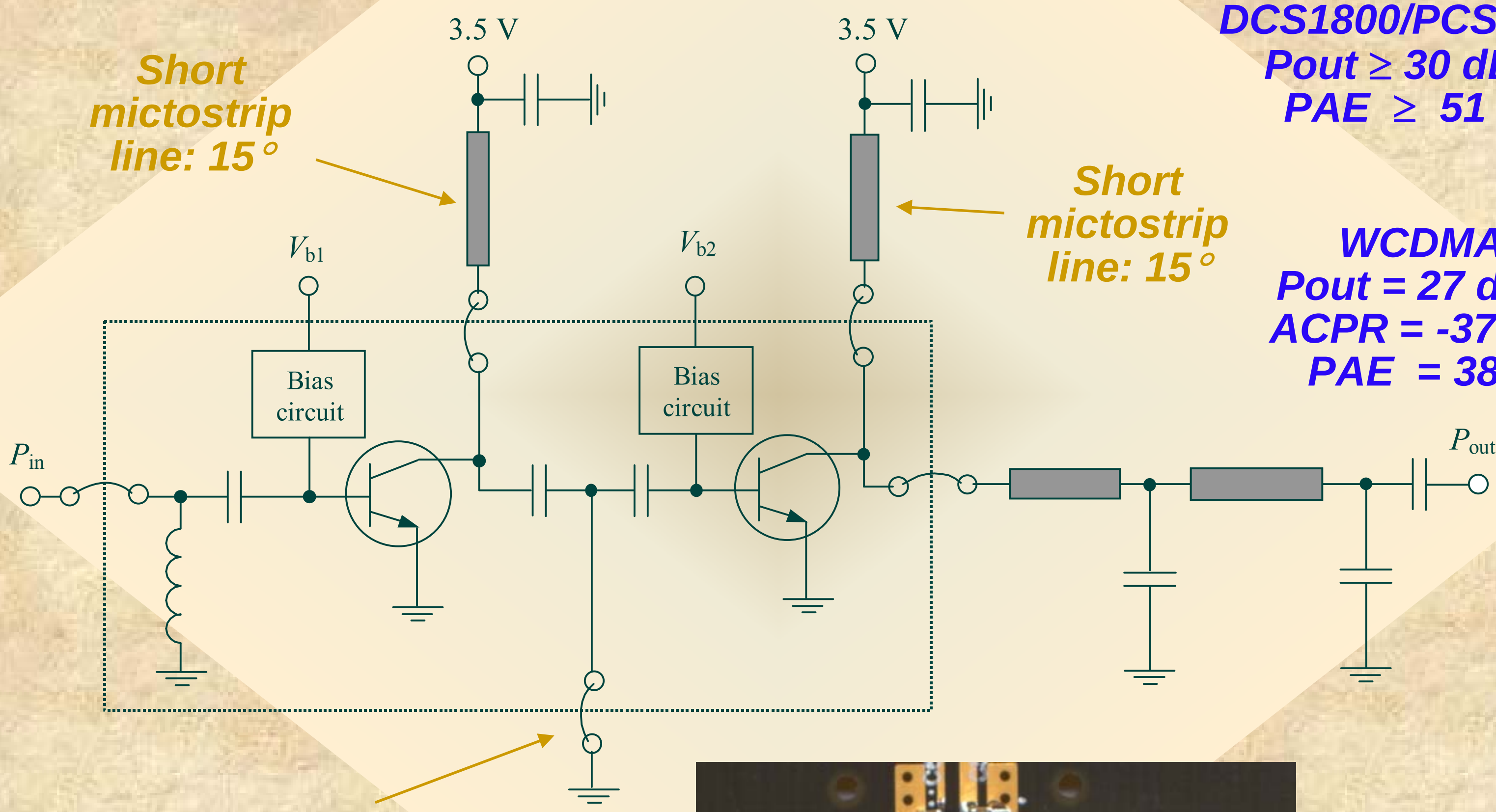
Current flowing through collector capacitance

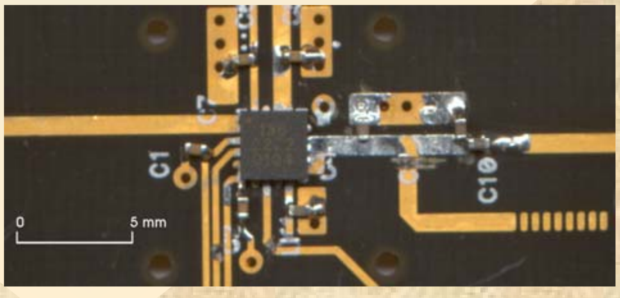
4.6. Class E with transmission lines: design example

1.71-1.98 GHz handset InGaP/GaAs HBT power amplifier: two-stage MMIC designed in 2001

DCS1800/PCS1900:
Pout ≥ 30 dBm
PAE ≥ 51 %

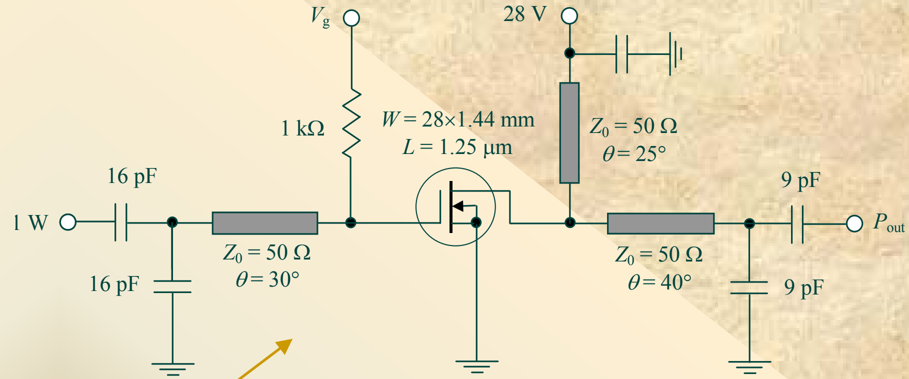
WCDMA:
Pout = 27 dBm
ACPR = -37 dBc
PAE = 38 %



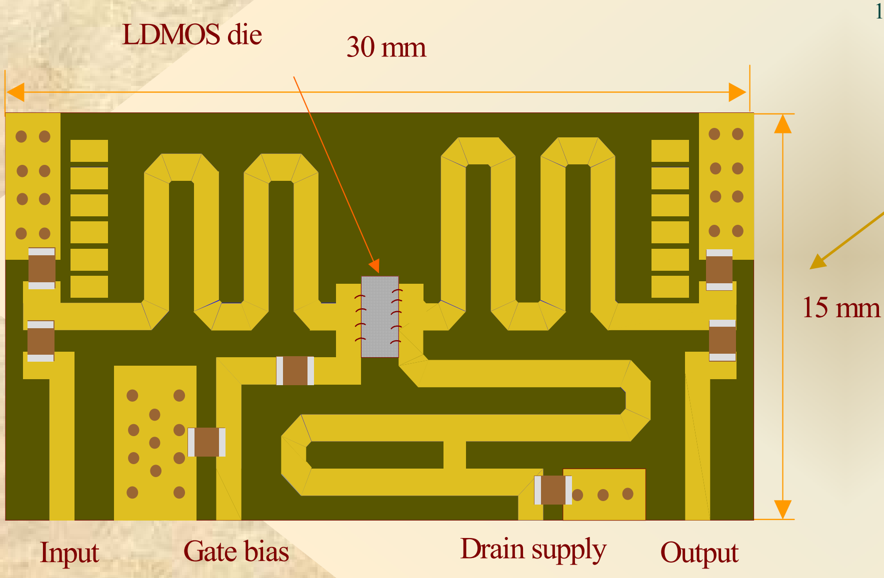


3x3mm package

4.6. Class E with transmission lines: design example



28 V single-stage LDMOSFET power amplifier module

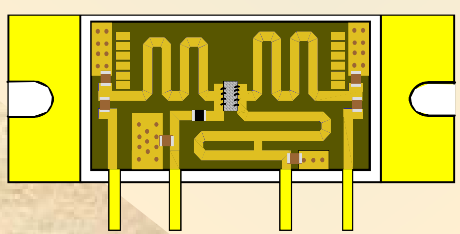


Bandwidth: 480-520 MHz

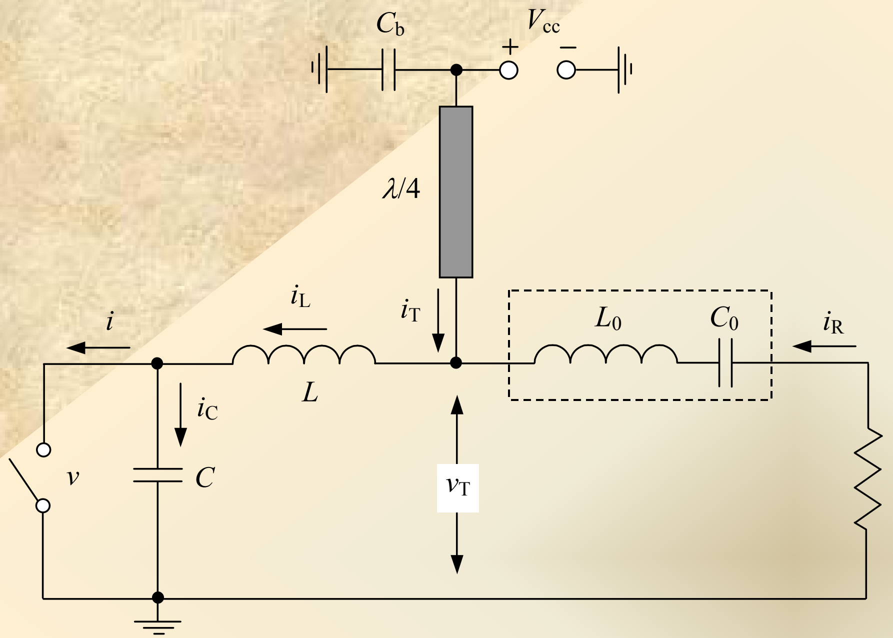
Output power: 20 W

Power gain: 15 dB

PAE: 67%



4.6. Class E with quarterwave transmission line



Optimum voltage conditions across switch:

$$v(\omega t)\Big|_{\omega t = 2\pi} = 0$$

$$\left.\frac{dv(\omega t)}{d\omega t}\right|_{\omega t = 2\pi} = 0$$

- **sinusoidal load current**
- **50% duty cycle**

$$\frac{d^2 i_C(\omega t)}{d(\omega t)^2} + \frac{q^2}{2} i_C(\omega t) + I_R \sin(\omega t + \varphi) = 0$$

- second-order differential equation

boundary conditions:

$$i_C(\omega t)\Big|_{\omega t = \pi} = 2 i_R(\pi)$$

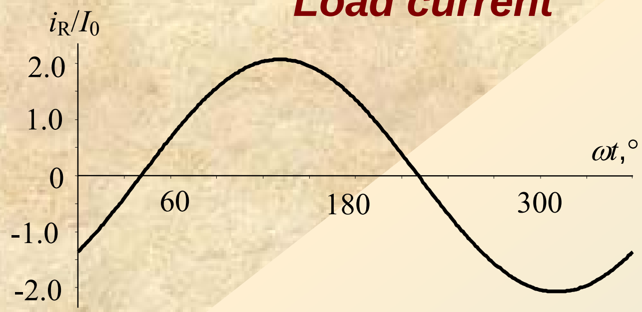
$$\left.\frac{d i_C(\omega t)}{d(\omega t)}\right|_{\omega t = \pi} = \frac{V_{cc}}{\omega L} - I_R \cos(\varphi)$$

$$p = \frac{\omega L I_R}{V_{cc}} \qquad q = 1/\omega\sqrt{LC}$$

$$q = 1.649 \quad p = 1.302 \quad \varphi = -40.8^\circ$$

4.6. Class E with quarterwave transmission line

Load current



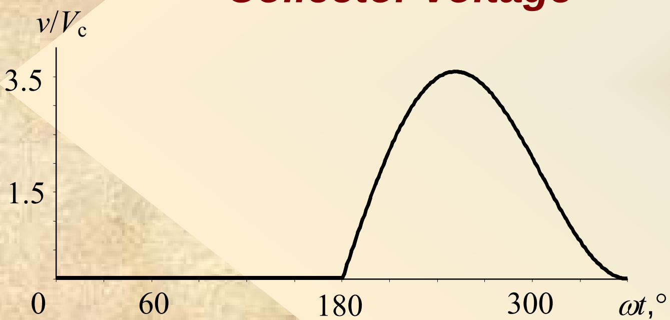
Optimum circuit parameters :

$$L = 1.349\frac{R}{\omega}$$ - series inductance

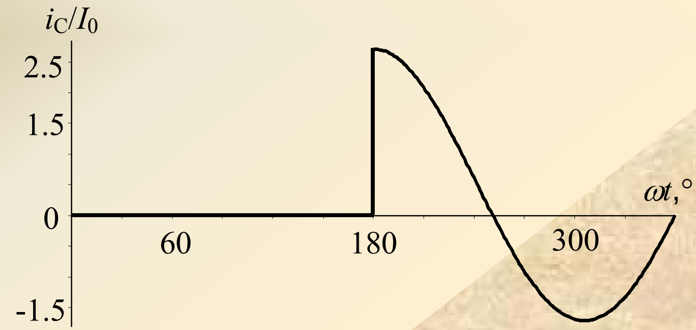
$$C = \frac{0.2725}{\omega R}$$ - shunt capacitance

$$R = 0.465\frac{V_{cc}^2}{P_{out}}$$ - load resistance

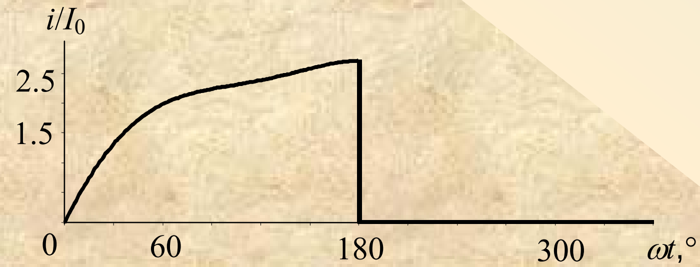
Collector voltage



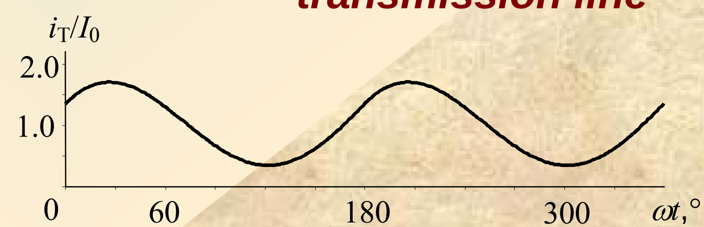
Current through capacitance



Collector current

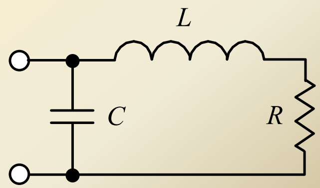
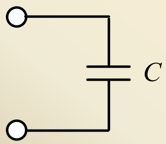
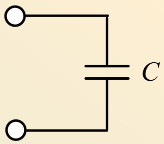
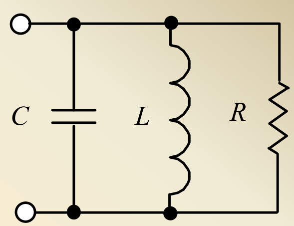
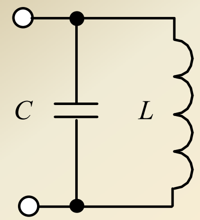
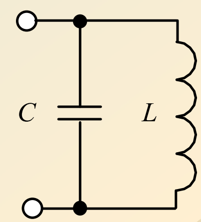
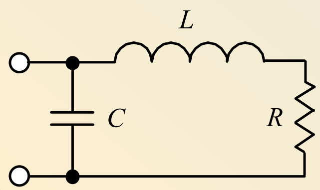
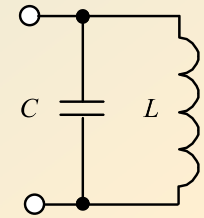
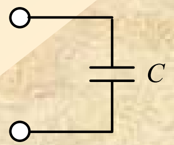


Current through transmission line



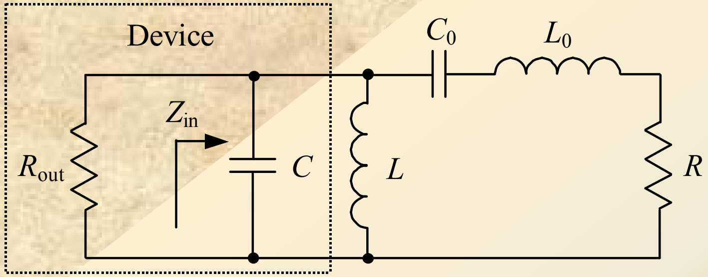
4.6. Class E with quarterwave transmission line

Optimum impedances at fundamental and harmonics for different Class E load networks

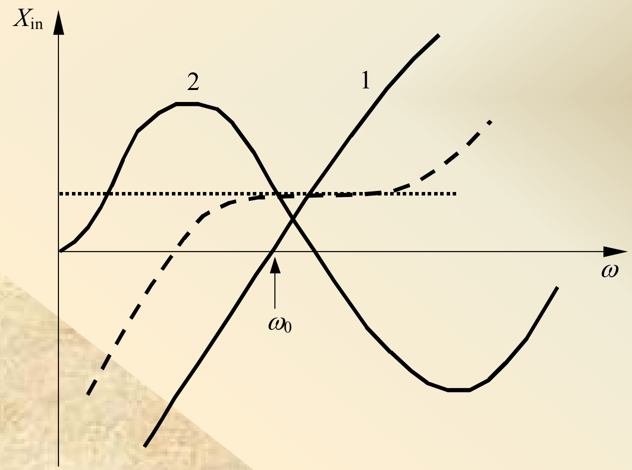
Class E load network	f_0 (fundamental)	$2nf_0$ (even harmonics)	$(2n+1)f_0$ (odd harmonics)
Class E with shunt capacitance			
Class E with parallel circuit			
Class E with quarterwave transmission line			

4.7. Broadband Class E circuit design

Reactance compensation load network



Reactance compensation principle



1 - impedance provided by series L_0C_0 resonant circuit

2 - impedance provided by parallel LC resonant circuit

- *summation of reactances with opposite slopes results in constant load phase over broad frequency range*

Input load network admittance

$$Y_{in} = \left(j\omega C + \frac{1}{j\omega L} + \frac{1}{R + j\omega' L_0} \right)$$

$$\omega' = \omega\left(1 - \frac{\omega_0^2}{\omega^2}\right) \qquad \omega_0 = 1/\sqrt{L_0 C_0}$$

To maximize bandwidth:

$$\left.\frac{d\,\mathrm{Im}\,Y_{in}(\omega)}{d\omega}\right|_{\omega=\omega_0} = 0$$

$$C + \frac{1}{\omega^2 L} - \frac{2L_0}{R^2} = 0$$

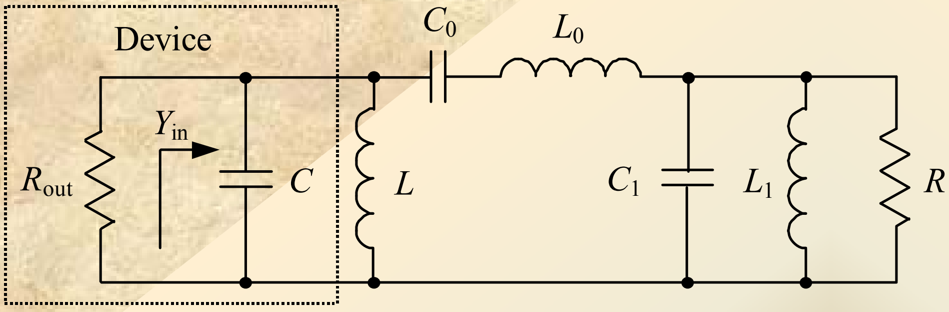
Optimum circuit parameters using equations for inductance L and capacitance C in Class E mode

$$L_0 = 1.026\frac{R}{\omega}$$

$$C_0 = 1/\omega^2 L_0$$

4.7. Broadband Class E circuit design

Double reactance compensation load network



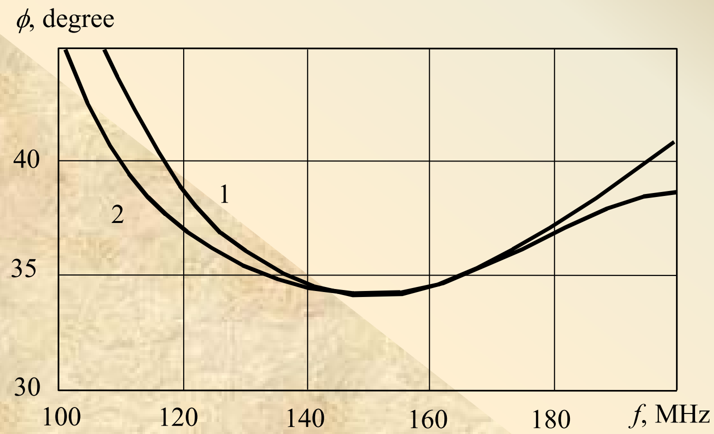
To maximize bandwidth:

$$\left.\frac{dB}{d\omega}\right|_{\omega=\omega_0} = \left.\frac{d^3B}{d\omega^3}\right|_{\omega=\omega_0} = 0$$

$$C + \frac{1}{\omega^2 L} - 2\frac{C_1R^2 - L_0}{R^2} = 0$$

$$\frac{1}{\omega^2 L} + \frac{C_1R^2 - L_0}{R^2} - 8\omega^2 L_0\left[C_1^2 + \frac{\left(C_1R^2 - L_0\right)\left(L_0 - 2C_1R^2\right)}{R^4}\right] = 0$$

Load network phase angle



Optimum circuit parameters using equations for inductance L and capacitance C in Class E mode

$$L_0 = \frac{R}{\omega}\frac{2}{\sqrt{5} - 1} \qquad C_0 = \frac{1}{\omega^2 L_0}$$

$$C_1 = \frac{L_0}{R^2}\frac{3 - \sqrt{5}}{2} \qquad L_1 = \frac{1}{\omega^2 C_1}$$

1 - single reactance compensation load network

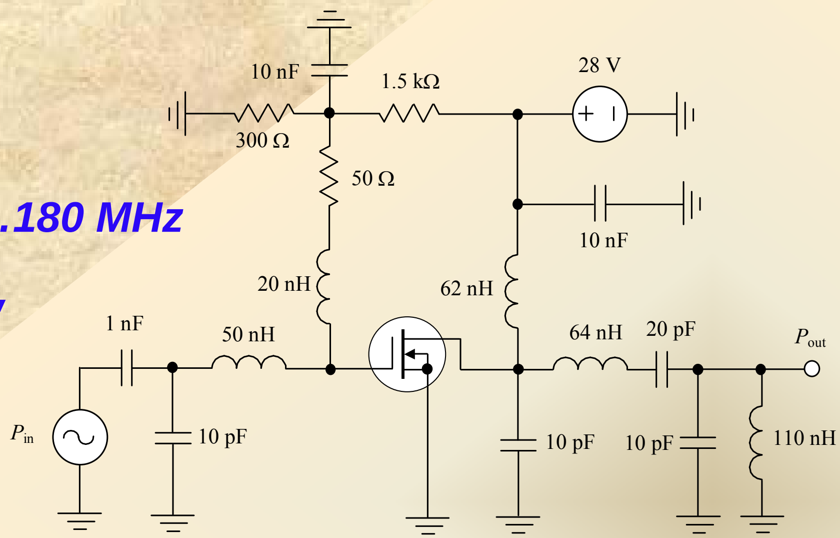
2 - double reactance compensation load network

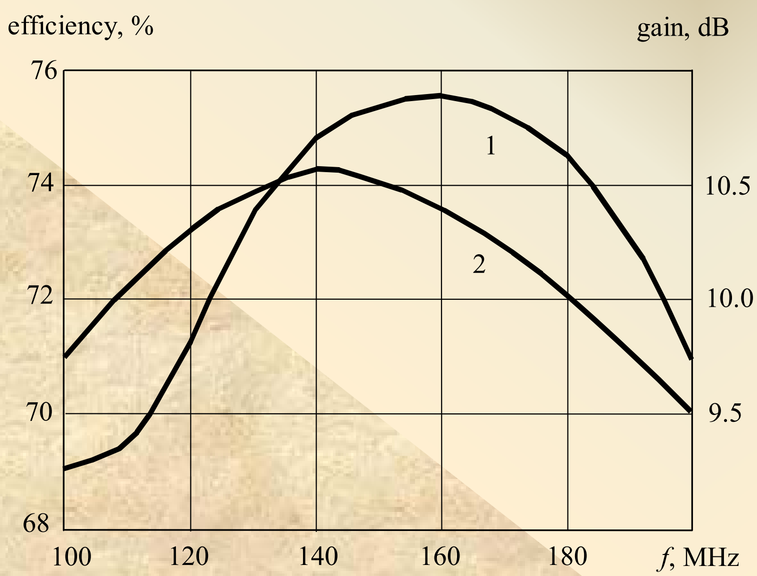
4.7. Broadband Class E circuit design

Broadband Class E power amplifier with double reactance compensation

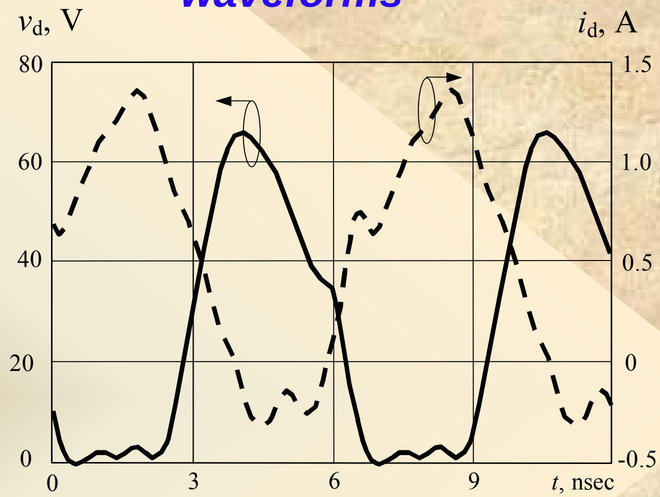
f_0 = 120…180 MHz

P_{in} = 1 W





Drain voltage and current waveforms



LDMOSFET:
gate length 1.25 um
gate width 7x1.44 mm

1 - drain efficiency > 71%

2 - power gain > 9.5 dB

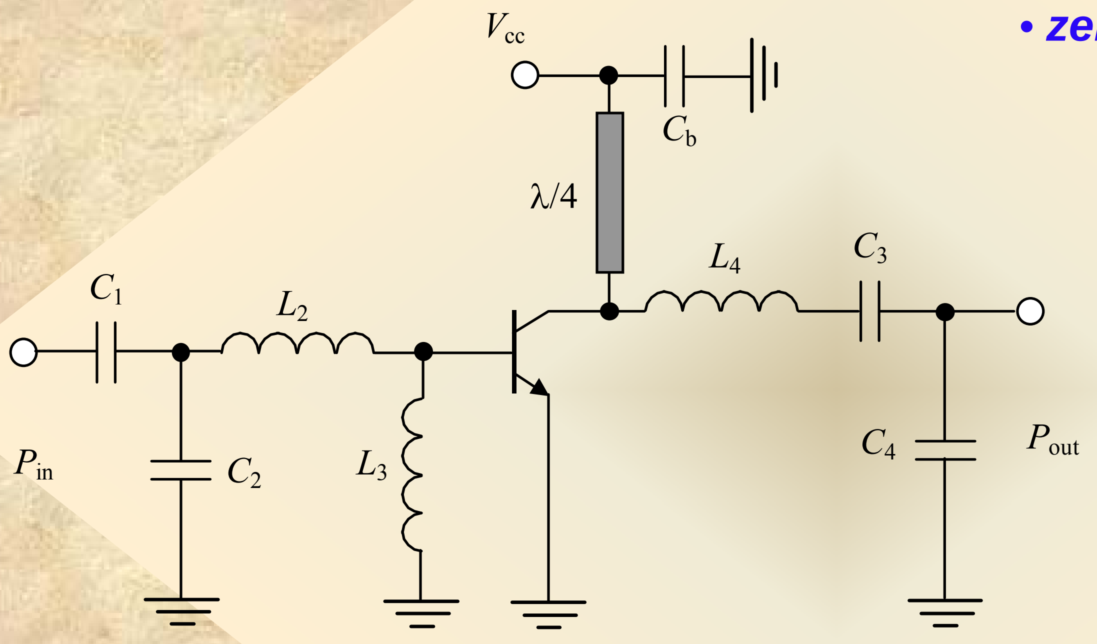
Input power - 1 W

Input VSWR < 1.4

Gain flatness ≤ ± 0.3

4.8. Practical high efficiency RF and microwave power amplifiers

Typical bipolar RF Class F power amplifier

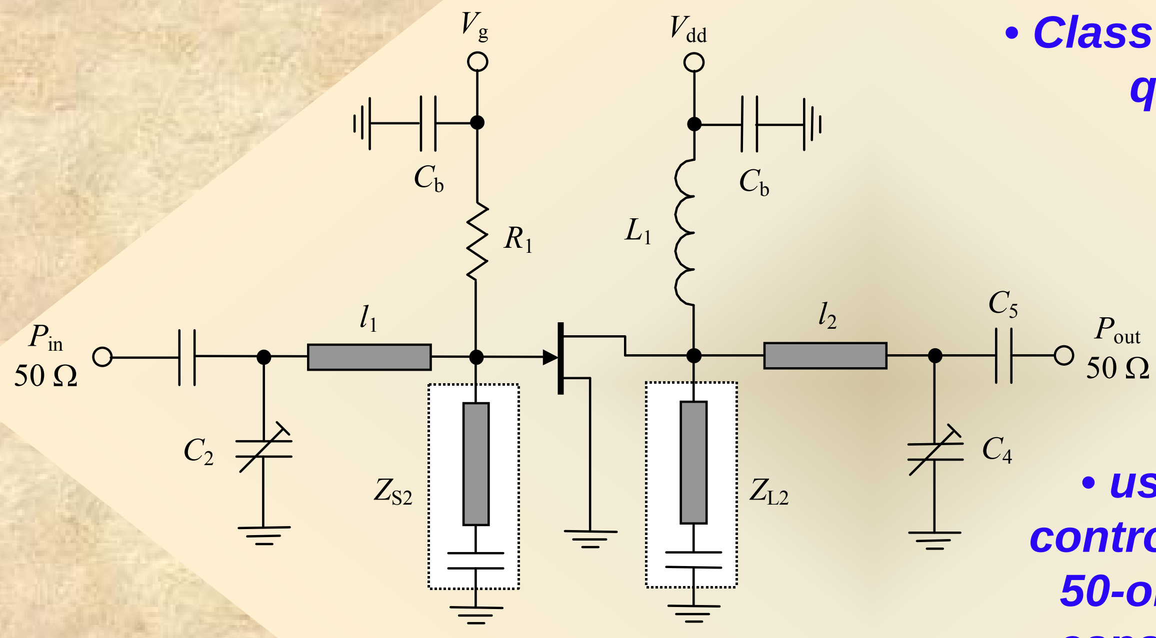


- ***zero-volt Class C biasing using RF choke***
- ***T-type input and output matching circuits with parallel capacitance***
- ***quarterwave transmission line in collector to suppress even harmonics***
- ***high-Q series LC circuit to provide high impedance conditions for harmonics***

Up to 90% collector efficiency for 10 W at 250 MHz

4.8. Practical high efficiency RF and microwave power amplifiers

Harmonic controlled MESFET microwave Class F power amplifier



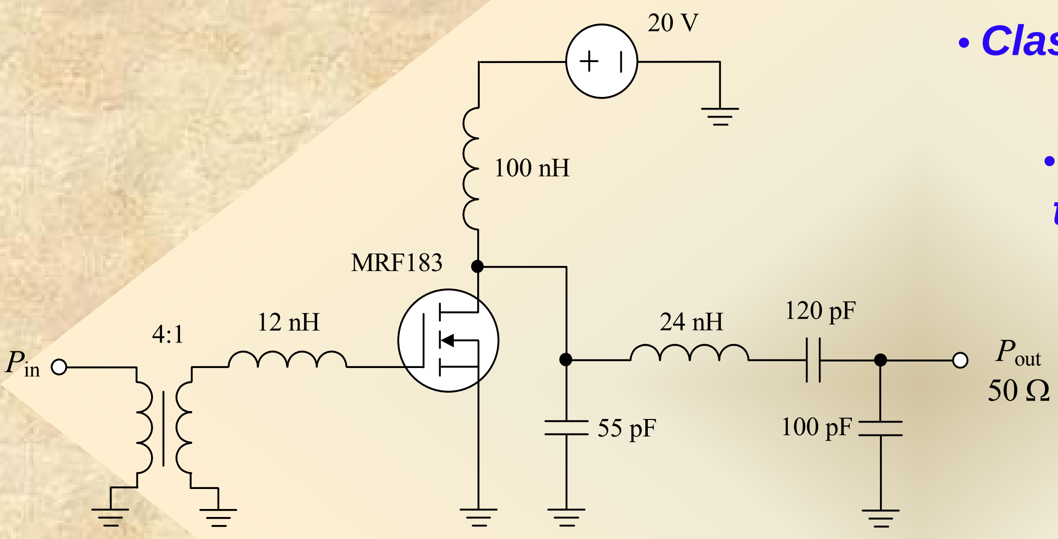
- *Class AB biasing with small quiescent current*
- *T-type input and output matching circuits with parallel capacitance*
- *using second harmonic controlled circuits with series 50-ohm microstrip line and capacitance each at device input and output*

Input second-harmonic termination circuit is required to provide input quasi-square voltage waveform minimizing device switching time

74% power-added efficiency for 1.4 W at 930 MHz

4.8. Practical high efficiency RF and microwave power amplifiers

High power LDMOSFET RF Class E power amplifier

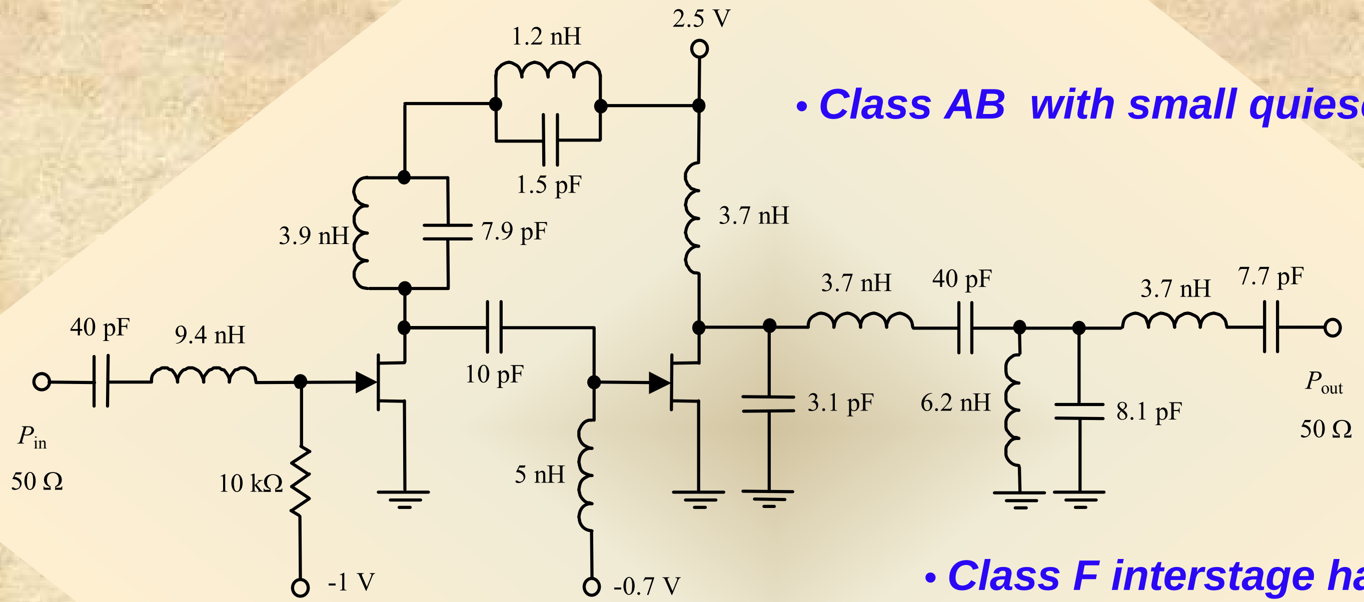


- Class B with zero quiescent current
- series inductance and ferrite 4:1 transformer is required to match device input impedance
- L-type output transformer to match optimum 1.5-ohm output impedance to 50-ohm load
- quality factor of resonant circuit was chosen to be sufficiently low (~5) to provide some frequency bandwidth operation and to reduce sensitivity to resonant circuit parameters
- required value of Class E shunt capacitance is provided by device intrinsic 38-pF capacitance and external 55-pF capacitance

70% drain efficiency for 54 W at 144 MHz

4.8. Practical high efficiency RF and microwave power amplifiers

Low voltage fully integrated MESFET Class E power amplifier



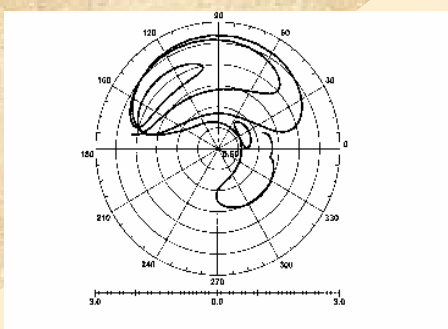
- *Class AB with small quiescent current*
- *Class F interstage harmonic controlled circuit using two LC resonant circuits tuned on fundamental and third harmonic to approximate square-wave driving signal*
- *Class E load network with optimum series inductance and shunt capacitance*
- *T-type output matching circuit for impedance transformation to 50-ohm load*

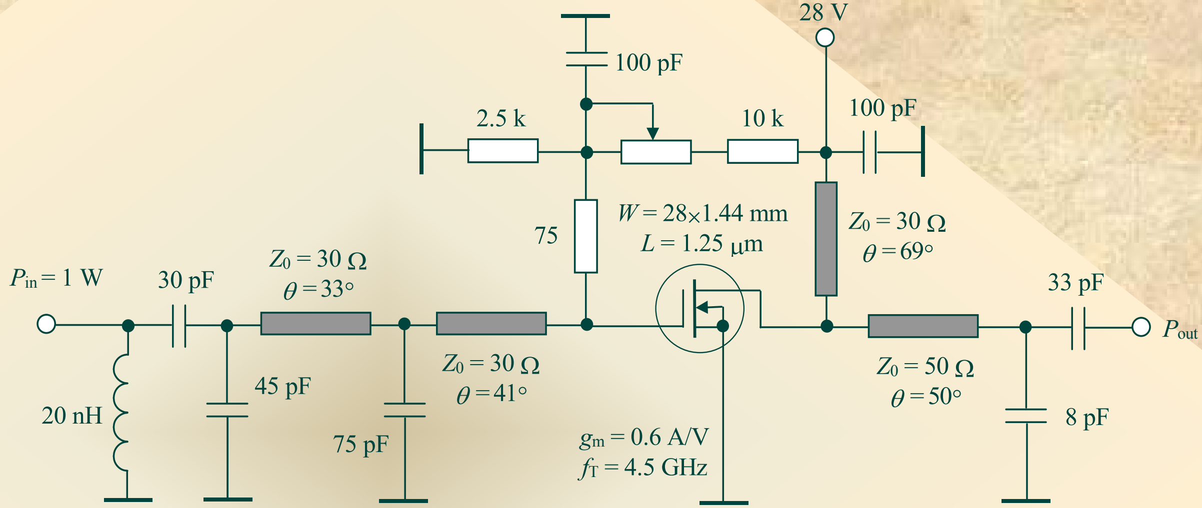
50% power-added efficiency for 24 dBm within 800-870 MHz

4.8. Practical high efficiency RF and microwave power amplifiers

225-400 MHz 28 V 20 W LDMOSFET Class AB power amplifier: simulations

Stability

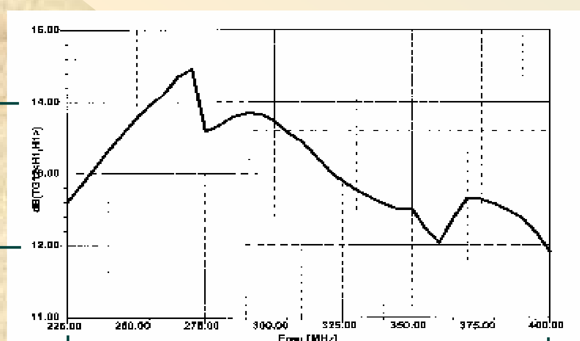




Power gain

14 dB

12 dB



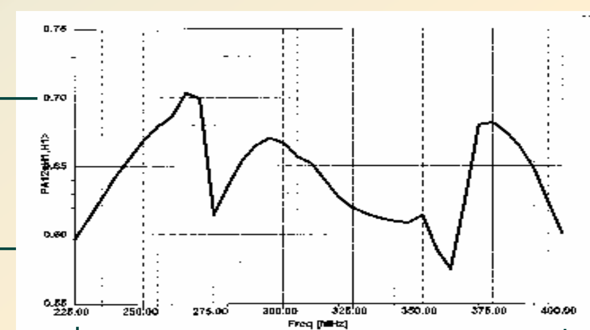
225 MHz

400 MHz

Power-added efficiency

70%

60%



225 MHz

400 MHz